CHAPTER 4

Characterization and Modeling of Planes and Laminates

4.1 Introduction

Planes with dielectric layer separation, also called the power-bus, serve several purposes in PDNs: they carry dc current from source to load, they connect bypass capacitors horizontally to active devices, and many times they also provide a return path for signals. The nature and depth of modeling and characterization depends on our interests and (ultimate) goals. If we are worried about the dc voltage drop on a high-current but otherwise well-filtered supply rail, our main focus may be limited to the equivalent dc resistance and voltage-drop profile. For lower current multi-GB IO rails the dc voltage drop may matter less, but we may need to characterize and model the high-frequency return-path function of the plane over a wide frequency band. If our task is to characterize the material properties of the conductive planes and dielectric laminates, we may not care much for the practical limitations of connecting geometry in the real usage, but we might want to model and capture the pure material properties as accurately as possible. Finally, if our focus is electromagnetic compatibility, we probably need to characterize primarily the high-frequency resonance peaks.

There are several commercial tools available to simulate PDN planes (see Chapter 2). Tools which use the finite difference time domain (FDTD) method (see, e.g., [1]) solve for the structure's response in the time domain, and obtain the frequency domain response by translating the result with fast Fourier transform. FDTD solutions are known to have time-efficient execution for large problems, but the translation to the frequency domain is limited by the equidistant time-sample requirement of the transformations. Equidistant time samples result in a linear scale in the frequency domain. PDNs may require characterization in the frequency domain over several decades of frequency. The linear scale either ignores low-frequency details or requires an unrealistically large number of points, many of which at the high end of the frequency range are not needed. This is because PDN components necessarily come in a limited range of quality factor (Q), which is more readily suited for logarithmic description.

While FDTD does not lend itself to simple implementation by the end user, analytical plane models based on the cavity resonances (see, e.g., [2]) are easy to program in spreadsheet programs or MATLAB for rectangular shapes; solutions based on the *Partial Element Equivalent Circuit* (PEEC) (see, e.g., [3]) are easy to program in SPICE.

4.2 Analytical Plane Models

For parallel plane pairs separated by a uniform dielectric material, analytical impedance expressions are available describing the self- and transfer impedances between rectangular ports. Analytical expressions are available for simple plane shapes, such as rectangular, triangular, or circular. Of these options, the rectangular shape is the most widely used, both directly and as a building block, to construct irregular plane shapes.

4.2.1 Analytical Models for Rectangular Plane Shapes

The parameters are defined in Figure 4.1. Figure 4.1(a) shows a top view of the plane structure, defining the size of the rectangular plane shape as w_x by w_y. There are two ports on the plane pair. Port i is at coordinates (x_i, y_i), and port j is at coordinates (x_j, y_j). Figure 4.1(b) defines the vertical geometry and the material properties. We assume a uniform plane spacing of h and a uniform relative dielectric constant of ε_r. The upper and lower planes have thicknesses of t_u and t_l, and conductivities of σ_u and σ_l, respectively.

In PCBs with regular lamination processes, as well as in organic packages, the two planes separated by a dielectric layer may represent either a core, or a prepreg with the planes belonging to cores above and below. If located on the same core, the nominal plane thicknesses and conductivities are probably, but not necessarily, the same. If located on different cores, or if a build-up process is used to create the PCB or package, the two plane layers may be nominally different. One of the planes may be of copper with regular thickness, such as 18 μm (0.5 oz) or 35 μm (1 oz), while the other plane could be a 70-μm (2 oz) or 140-μm (4 oz) copper plane or a similarly thick aluminum layer for heat-spreader purposes and to help to distribute large currents.

4.2.1.1 Lossless Cavity Model

If we assume that the plane separation, h, is small compared to any wavelength of interest, the field can be considered to be constant along the z-axis; this results in a

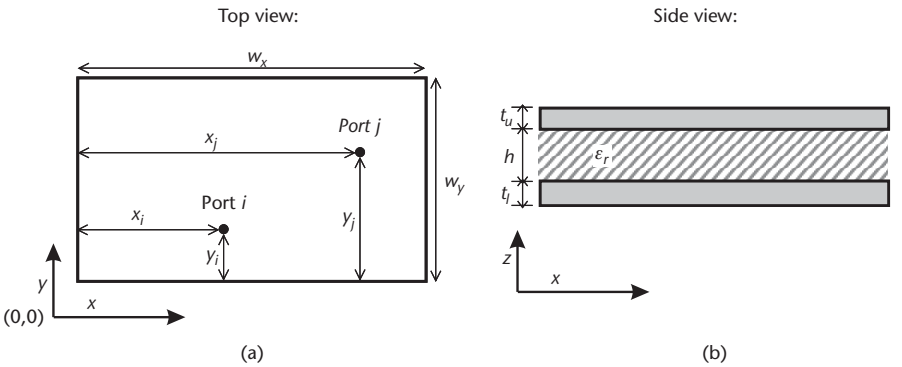


Figure 4.1 Rectangular parallel plane pair, separated by a uniform layer of dielectric material. Part (a) shows the top view and (b) defines the vertical geometry. Not to scale.

2D waveguide cavity with open boundaries. Waves traveling horizontally between the planes experience full reflection at the open boundaries; this reflection gives rise to a 2D series of modal resonances at frequencies where the w_x or w_y dimension equals integer multiples of the half wavelength. This structure has been analyzed for planar array antennas [4], for planar microwave circuits [5], and more recently for PDN applications.

In Figure 4.1, the generic transfer impedance between ports *i* and *j* for a lossless structure is given by:

$$Z_{ij}(\omega) = j\omega\mu h \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{\chi_{mn}^2}{w_x w_y \left(k_{xm}^2 + k_{yn}^2 - k^2\right)} f\left(x_i, y_i, x_j, y_j\right) \tag{4.1}$$

where

$$\begin{aligned} f\left(x_i, y_i, x_j y_j\right) = {} & \cos\left(\frac{m\pi x_i}{w_x}\right)\mathrm{sinc}\left(\frac{m\pi t_{xi}}{2w_x}\right)\cos\left(\frac{n\pi y_i}{w_y}\right)\mathrm{sinc}\left(\frac{n\pi t_{yi}}{2w_y}\right)\cdot \\ & \cos\left(\frac{m\pi x_j}{w_x}\right)\mathrm{sinc}\left(\frac{m\pi t_{xj}}{w_x}\right)\cos\left(\frac{n\pi y_j}{w_y}\right)\mathrm{sinc}\left(\frac{n\pi t_{yj}}{2w_y}\right) \end{aligned} \tag{4.2}$$

$$k = \omega\sqrt{\varepsilon\mu} = \omega\sqrt{\varepsilon_r\varepsilon_0\mu_0} = \sqrt{\varepsilon_r}\,\frac{\omega}{c} \tag{4.3}$$

$\omega = 2\pi f$ is the angular frequency;
μ is the permeability of dielectric ($\mu = \mu_0 = 4\pi 10^{-7}$);
c is the speed of light.

$$k_{xm}^2 = \left(\frac{m\pi}{w_x}\right)^2,\ k_{yn}^2 = \left(\frac{n\pi}{w_y}\right)^2$$

$\chi_{mn} = 1$ for $m = 0$ and $n = 0$; $\sqrt{2}$ for $m = 0$ or $n = 0$; 2 for $m \neq 0, n \neq 0$

(x_i, y_i), (x_j, y_j) are the coordinates of the ports;
(t_{xi}, t_{yi}), (t_{xj}, t_{yj}) are the port dimensions.

The analytical expression of (4.1) can be solved for any pair of arbitrarily located points on the planes, either self-impedance or transfer impedance, and is well suited for programming in spreadsheets with macro capabilities to evaluate the summations.

If the port dimensions are much smaller than the smallest wavelength of interest, the *sinc* functions disappear in (4.2) leaving the four *cosine* terms. Furthermore, if the two ports are at the same location such that the self-impedance of the plane is measured, then (4.2) simplifies to:

$$f\left(x_{ij}, y_{ij}\right) = \cos\left(\frac{m\pi x_{ij}}{w_x}\right)^2 \cos\left(\frac{n\pi y_{ij}}{w_y}\right)^2 \tag{4.4}$$

Though not limited by finite spatial granularity, as it is the case with SPICE-grid plane models, the analytical expression has a double infinite series, which for practical calculations must be truncated. This means that instead of being infinite, we have to use finite $n = N$ and $m = M$ limits. Figure 4.2 illustrates the effect of truncation with the simulated impedance of a plane pair of 25.4 × 25.4 cm (10 × 10 inch) size, 50-μm (2-mil) plane separation and dielectric constant of 4.0. The self-impedance was computed at one of the corners.

There are two major trends to observe as we change the summation limits in (4.1). As it was detailed for instance in [6, 7], at low frequencies, the impedance minima converge very slowly; at high frequencies, after the last impedance peak in the summation, the impedance drops monotonically, as opposed to a rising function that we would expect from the inductive behavior. Since the summation is based on poles, the impedance maxima included in the summation of a low-loss structure are captured properly, regardless of the summation limits. To ensure sufficient frequency coverage for the peaks, the N and M summation limits have to be chosen such that the highest included modal peak is safely above the highest frequency of interest. With $n = N$ and $m = M$ summation limits along the n and m variables, the frequencies of the last captured modal resonances are:

$$f_N = \frac{N}{2a}\frac{c}{\sqrt{\varepsilon_r}}, \quad f_M = \frac{M}{2b}\frac{c}{\sqrt{\varepsilon_r}} \tag{4.5}$$

While peaks automatically provide good convergence, the convergence around the minima is very slow. This is the most critical at the first impedance minimum of the self-impedance profile, because it usually reaches milliohm values in a low-loss PCB or package structure. Figure 4.3 shows the convergence with two plots using the same plane pair that was used for Figure 4.2. Figure 4.3(a) plots the simulated impedance magnitude, enlarged around the first minimum. Figure 4.3(b) plots the extracted frequencies of the impedance minimum from each trace. The summation limit was varied from $N = M = 1$ to $N = M = 20$ in increments of one.

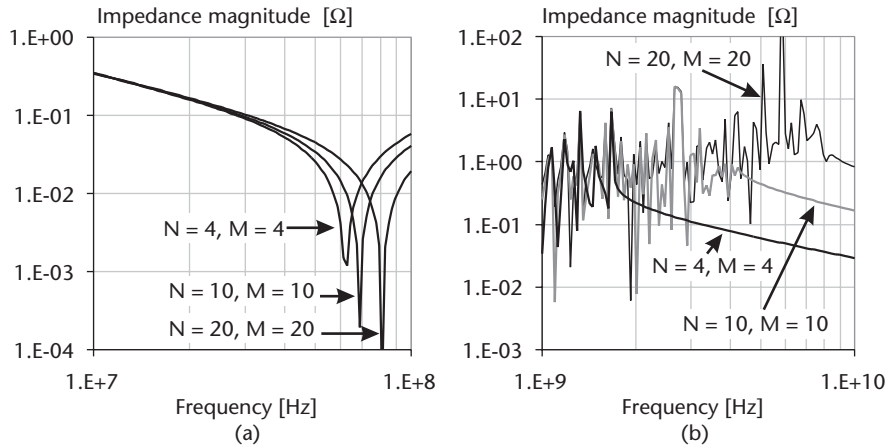


Figure 4.2 Self-impedance magnitude at the corner of a lossless square plane pair: (a) low-frequency response and (b) high-frequency response.

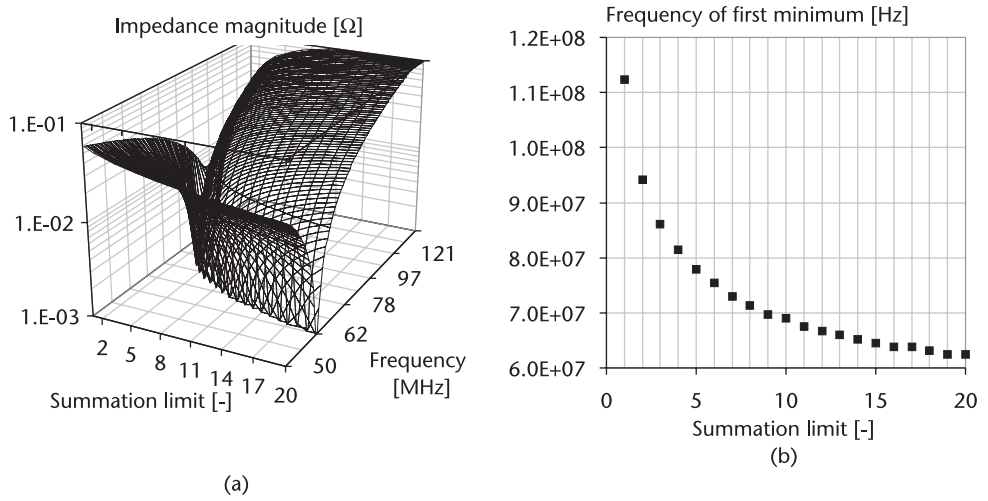


Figure 4.3 Convergence of the first impedance minimum as a function of summation limit: (a) plots the simulated impedance magnitude and (b) plots the minimum-impedance frequency points.

For laminates with a plane separations much larger than the thickness of either of the conductive layers, t_u or t_l, the lossless assumption yields fairly good agreement with measured data. Figure 4.4 compares the measured self-impedance magnitudes at a corner of a square parallel plane pair with simulated data using (4.1). The plane pair was square, with $w_x = w_y = 25.4$ cm (10 inches) and $h = 0.79$ mm (31 mils). The bare two-sided FR4 laminate had 35-μm (1 oz) copper on either side, and it was measured in several sizes: while the measurement test points were attached to one of its corners, the laminate sheet was repeatedly cut into four equal-size sections. First, the laminate was measured as is with its full size. Second, the sheet was cut into four squares of $w_x = w_y = 12.7$ cm (5 inches). Third, one of the smaller squares was fur-

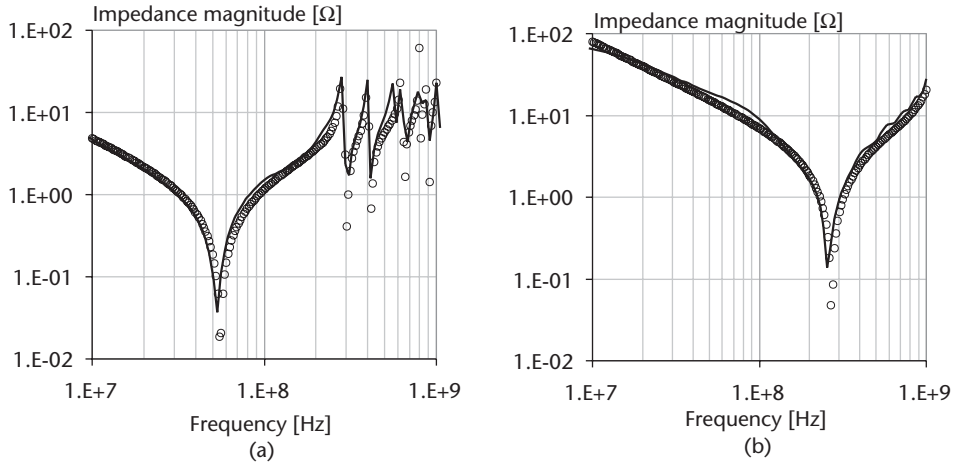


Figure 4.4 Comparison of measured self-impedance at a corner of a square pair of planes to simulated self-impedance using (4.1). Continuous lines: measured data. Small circles: simulated data. Plane separation is $h = 0.79$ mm (31 mils). (a) Plane size is $w_x = w_y = 25.4$ cm (10 inches). (b) Plane size is 6.35 cm (2.5 inches).

ther cut into four equal sections of $w_x = w_y = 6.35$ cm (2.5 inches). Figure 4.4 shows the correlation between measured and simulated self impedances for the (a) full-size and (b) smallest-size squares.

Besides the slow convergence around the minima, another drawback of the analytical solution based on (4.1) is the dual summation. One option to reduce the complexity of the calculations is to make use of the natural symmetry of the rectangular plane shape. By appropriately partitioning the planes, the responses for even and odd modes can be calculated, leading to an overall reduction in computation time [8]. A second possibility to reduce the computational complexity is to model the plane pair as a section of a rectangular waveguide so that one direction is automatically accounted for instead of using a summation. By applying magnetic walls along the opposite sides of length w_y, and applying open termination at the other two sides, the boundary conditions can be captured by a Green's function [9].

Finally, another major limitation of (4.1) is that the analytical expression assumes the structure is lossless. Plane pairs in real PCB exhibit many different types of losses, of which conductive losses and dielectric losses are generally the most prominent loss mechanisms. Several investigators have modified (4.1) to include conductive and dielectric losses. In the following sections, several different lossy formulations are discussed.

4.2.1.2 Light-Losses Cavity Model

One approach to capture losses is to modify the real wave number, k, with a complex wave number given by [4]:

$$k = \beta - j\alpha = k' - jk'' \tag{4.6}$$

where $k' = k$ from (4.3), and

$$k'' = \omega\sqrt{\varepsilon_r \varepsilon_0 \mu_0}\left(\frac{\tan\_\delta}{2} + \frac{\delta}{2h}\right) \tag{4.7}$$

where tan_δ is the loss tangent of the dielectric material, and δ is the skin depth at the frequency of interest, given by:

$$\delta = \sqrt{\frac{1}{\pi f \sigma \mu}} \tag{4.8}$$

The model assumes that there is small dissipation (i.e., $k' >> k''$).

This model accounts for the attenuation but neglects any changes to the phase constant β caused by the nonideal conductor and dielectric substrate. For this reason, strictly speaking, the solution is not causal [10]. The overall attenuation constant, α, is calculated by summing the dielectric loss and conductive loss.

4.2.1.3 Modified Cavity Model Using the Complex Propagation Constant

A second approach to capture losses is to substitute the complex propagation constant for the real wave number, k, in (4.3) [11]. The per-unit-length transmission line parameters are obtained using a lumped-element model of a radial transmission line. The effect of the imperfect dielectric substrate is represented by the shunt conductance, G_d, and the conductive losses are represented by the series impedance, Z_{cu}. The modified cavity model expression and accompanying formula for the propagation constant are

$$Z_{ij}(\omega) = j\omega\mu h \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{\chi_{mn}^{2}}{w_x w_y \left(k_{xm}^2 + k_{yn}^2 + \gamma^2\right)} f\left(x_i, y_i, x_j, y_j\right) \tag{4.9}$$

where

$$\gamma = \sqrt{\left(Z_{cu} + j\omega L\right)\left(G_d + j\omega C\right)} = j\omega\sqrt{\varepsilon\mu}\sqrt{\left(1 - \frac{j(1+j)\delta}{h}\right)\left(1 - j\tan\_\delta\right)} \tag{4.10}$$

4.2.1.4 Equivalent Circuit-Based Cavity Model

A third approach to include losses takes the dual infinite series of (4.1) and transforms it into an equivalent circuit [12]. By using parallel resonant circuits and ideal transformers, the transfer impedance between port i and port j is:

$$Z_{ij}(\omega) = \sum_{n=1}^{\infty}\sum_{m=1}^{\infty} \frac{\chi_{mn}^{2}}{\frac{1}{j\omega L_{mn}} + j\omega C_{mn} + G_{mn}} f\left(x_i, y_i x_j, y_j\right) + \frac{1}{j\omega C_{00} + G_{00}} \tag{4.11}$$

where

$$C_{00} = \frac{\varepsilon_0 \varepsilon_r w_x w_y}{h}, \quad G_{00} = C_{00}\omega\left(\tan\_\delta + \frac{\sqrt{\frac{2}{\omega\mu\sigma}}}{h}\right) \tag{4.12}$$

$$f_{mn} = \frac{\sqrt{\left(\frac{m}{w_x}\right)^2 + \left(\frac{n}{w_y}\right)^2}}{2\sqrt{\varepsilon_0 \varepsilon_r \mu}} \tag{4.13}$$

$$L_{mn} = \frac{h}{\omega_{mn}^2 w_x w_y \varepsilon_0 \varepsilon_r}, \quad C_{mn} = \varepsilon_0 \varepsilon_r \frac{ab}{s}, \quad G_{mn} = C_{mn}\omega_{mn}\left(\tan\_\delta + \frac{\sqrt{\frac{2}{\omega_{mn}\mu\sigma}}}{h}\right) \tag{4.14}$$

The static capacitance of the plane pair is separated (i.e., $m = 0$, $n = 0$) from the higher-order modes in (4.11). Each mode of the structure can be represented as a resonant circuit with the resonant frequency equal to (4.13). The equivalent circuit of (4.11) through (4.14) is shown in Figure 4.5 for two ports.

4.2.1.5 Transmission Plane Model

Finally, a fourth approach for including losses in the cavity model was described in [10]. In this approach, partial differential equations are derived in the frequency domain for the parallel plane structure. This yields expressions for the distributed admittance, $Y(\omega)$, and impedance, $Z(\omega)$, of the plane pair which are then substituted into (4.1). The modified cavity model expression and accompanying formula are

$$Z_{ij}(\omega) = Z(\omega)\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{\chi_{mn}^{2}}{w_x w_y\left(k_{xm}^2 + k_{yn}^2 + Z(\omega)Y(\omega)\right)} f\left(x_i, y_i, x_j, y_j\right) \tag{4.15}$$

where

$$Z(\omega) = j\omega L + Z_s(w), \quad Y(w) = \frac{1}{h}\left(j\omega\varepsilon_0\varepsilon_r(\omega) + \sigma\right) \tag{4.16}$$

$$L = \mu h, \quad Z_s = \frac{2k_m}{\sigma}\cot(k_m t), \quad k_m = (1-j)\frac{1}{\delta} \tag{4.17}$$

t is the thickness of the top and bottom metal planes.

In (4.16), σ is a bulk conductivity of dielectric and is zero for FR4-type dielectrics. It was included in the derivation because some PDN dielectric materials actually may have nonzero conductivity to suppress noise.

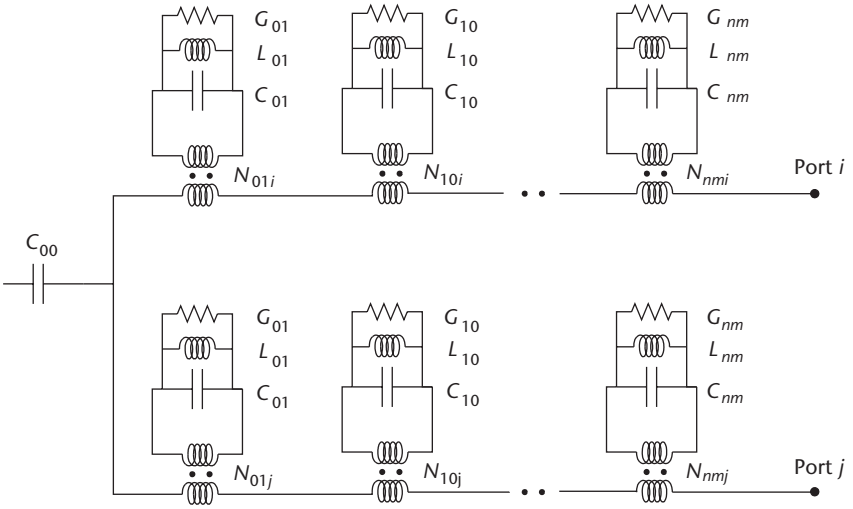


Figure 4.5 Equivalent circuit of the plane transfer impedance based on a cavity resonance model for two ports and $n \times m$ modes.

In this formulation, the complex, relative dielectric constant, $\varepsilon_r(\omega)$, included in (4.16), is defined over a broadband frequency range to ensure that (4.15) is causal. The Debye model is used to capture the frequency dependence of the complex dielectric constant and is included here for reference

$$\varepsilon_r(f) = \varepsilon_r(\infty) + \varepsilon_{rd} F_d(f) \tag{4.18}$$

where

$$F_d(f) = \frac{1}{(m_2 - m_1)\ln(10)} \ln\left[\frac{10^{m2} + jf}{10^{m1} + jf}\right] \tag{4.19}$$

$$\varepsilon_{rd} = -\frac{\tan\delta(f_0)\varepsilon_r(f_0)(m_2 - m_1)\ln(10)}{\mathrm{Im}(\theta)} \tag{4.20}$$

$$\varepsilon_r(\infty) = \varepsilon_r(f_0)\left(1 + \tan\_\delta(f_0)\frac{\mathrm{Re}(\theta)}{\mathrm{Im}(\theta)}\right), \quad \theta = \ln\left[\frac{10^{m2} + jf_0}{10^{m1} + jf_0}\right] \tag{4.21}$$

To employ this model the dielectric constant and loss tangent only need be defined at one frequency point, f_0; $m1$ and $m2$ are the parameters that define the linear portion of real part of the dielectric constant. The imaginary part of the dielectric constant (and thus loss tangent, too) will be linear in a narrower range, inside the $m1$ and $m2$ limits.

4.2.1.6 Cavity Model Simulations

To examine the accuracy of the four different lossy plane impedance formulations introduced above, the plane pair structure shown in Figure 2.1 was simulated. The m and n summation limits were set to 80 for all the simulations. The formulas were coded into MATLAB and the results postprocessed and plotted in Excel. Figure 4.6 plots the four lossy impedance expressions alongside measurement data of the test structure.

The different formulations produce similar results which are fairly well correlated to measurement although with some magnitude offset and frequency offset at higher frequencies. The transmission plane model, Figure 4.6(d), shows very little phase offset due to the inclusion of the frequency dependent dielectric constant in the model.

Plotting the low-frequency behavior, however, reveals several major differences among the formulations. Figure 4.7(a) plots the low frequency behavior of the *lossless* plane expression along side measurement data. Below the series resonances frequency, both impedance plots show a capacitive slope dictated by the static capacitance of the plane pair.

Figure 4.7(b) plots the four lossy plane expressions alongside the lossless plane expression. All but the transmission plane model show differing degrees of low-frequency roll off compared to the lossless case. The low-frequency roll off is due to the onset of skin effects (i.e., the skin depth approaches the thickness of the metal planes). Mathematically, the low-frequency response of these expressions can be

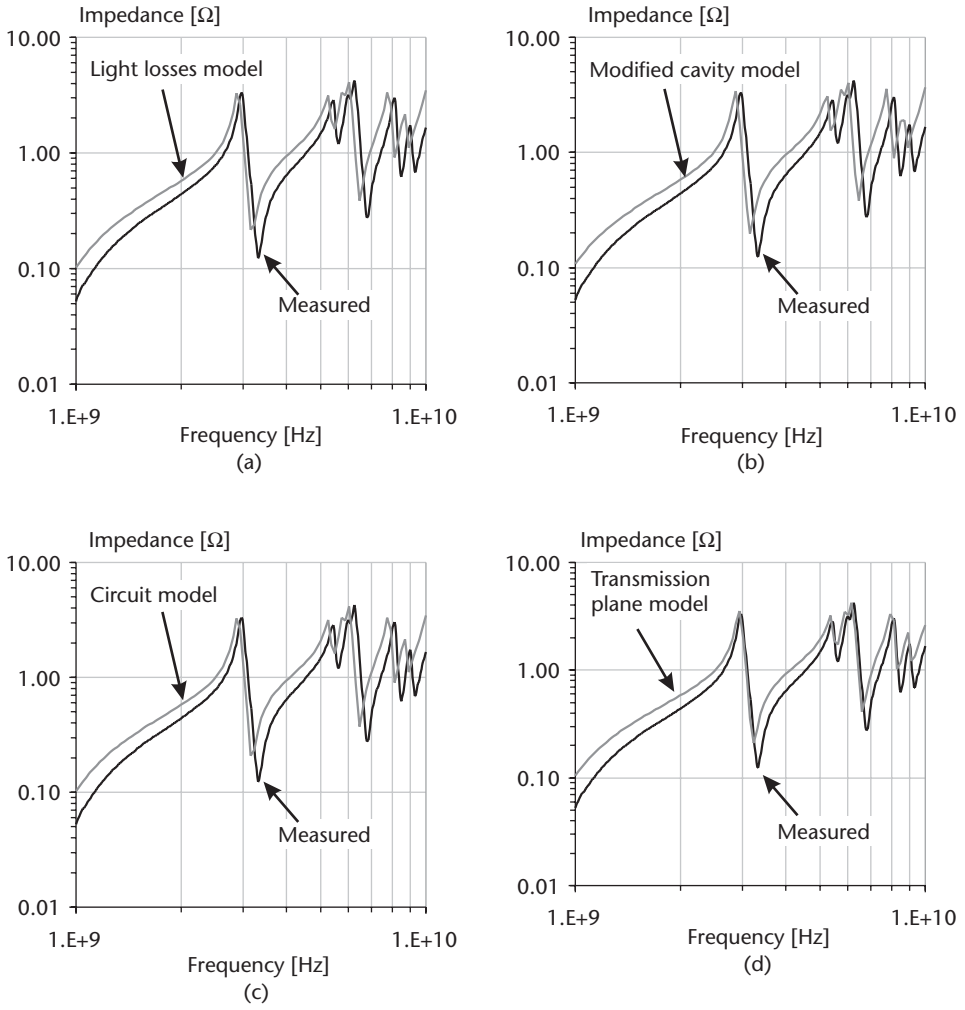


Figure 4.6 Measurement data for the test structure shown in Figure 2.1, plotted alongside the following four lossy impedance expressions: (a) light losses model, (b) modified cavity model, (c) circuit model, and (d) transmission plane model.

understood by examining the $m = 0$, $n = 0$ mode, which should capture the static capacitance of the plane pair. Substituting $m = 0$, $n = 0$ in the lossless case (4.1), the low-frequency impedance of the plane pair is

$$Z_{ij}(\omega) = -j\frac{h}{\omega w_x w_y \varepsilon_0 \varepsilon_r} = \frac{1}{j\omega C_{00}} \tag{4.22}$$

This is the impedance of a lumped capacitor, C_{00}, representing the static capacitance of the plane pair. On the other hand, substituting $m = 0$, $n = 0$ into the modified plane impedance expression which assumes light losses (4.6) through (4.7) yields:

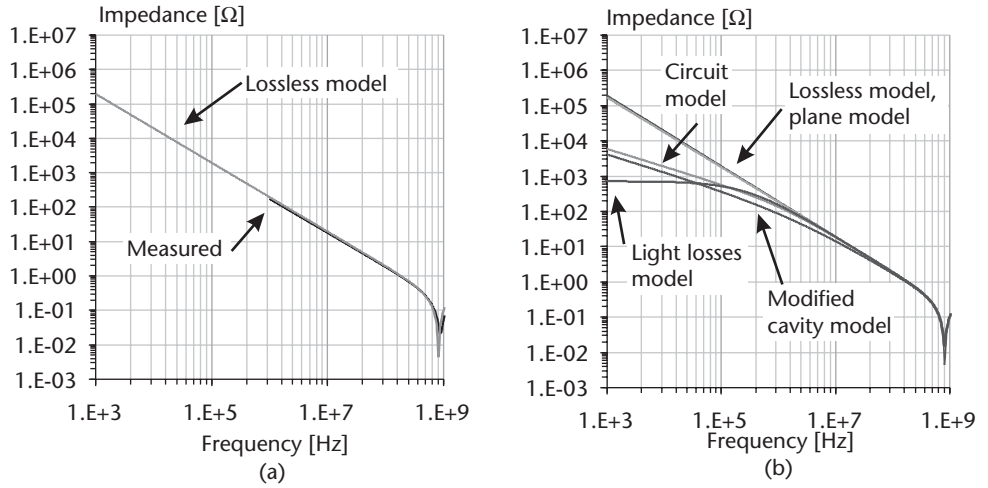


Figure 4.7 Measurement data for the strucutre shown in Figure 2.1, plotted alongside the (a) lossless model and (b) the four lossy models, together with the lossless model. The low-frequency roll off observed in (b) occurs at different frequencies for the different models.

$$Z_{ij}(\omega) = -j\frac{h}{w_x w_y h\varepsilon_0\varepsilon_r\left(1-j\left(\frac{\tan\_\delta}{2}+\frac{\delta}{2h}\right)\right)^2} = \frac{1}{j\omega C_{00}\left(1-j\left(\frac{\tan\_\delta}{2}+\frac{\delta}{2h}\right)\right)^2} \tag{4.23}$$

Equation (4.23) shows that the impedance can only be approximated by (4.22) if the dielectric thickness is much thicker than the skin depth and assuming light dielectric losses. The same requirement holds true for the modified plane impedance expression which uses the complex propagation constant, (4.9):

$$\begin{aligned} Z_{if}(\omega) &= -j\frac{h}{w_x w_y h\varepsilon_0\varepsilon_r\left(1-\frac{j(1+j)\delta}{h}\right)(1-j\tan\_\delta)} \\ &= \frac{1}{j\omega C_{00}\left(1-\frac{j(1+j)\delta}{h}\right)(1-j\tan\_\delta)} \end{aligned} \tag{4.24}$$

The low-frequency impedance of the equivalent circuit based model, which can be found by substituting (4.12) into (4.11) and solving for the $m = 0$, $n = 0$ mode, places a similar requirement on the plane thickness and dielectric loss:

$$Z_{ij}(\omega) = \frac{1}{j\omega C_{00}+G_{00}} = \frac{1}{\omega C_{00}\left(j+\left(\tan\_\delta+\frac{\delta}{h}\right)\right)} \tag{4.25}$$

Finally, the $m = 0$, $n = 0$ mode of the transmission plane model can be evaluated by substituting (4.16) into (4.15):

$$Z_{ij}(\omega)\frac{1}{w_x w_y Y(\omega)} = \frac{1}{j\omega C_{00}} \tag{4.26}$$

This is the only lossy, plane-impedance expression of the four discussed above which yields the same result obtained from the lossless plane impedance expression, (4.22); so it places no apparent limitation at low frequencies on the dielectric thickness or loss tangent. From (4.23) through (4.25), the low-frequency accuracy of the other lossy plane impedance expressions above are a function of the skin depth and dielectric loss. In Figure 4.7(b) the impedance frequency deviates from the linear capacitive slope when the skin depth approaches the thickness of the dielectric.

Simulations were performed to examine the accuracy limitations of the four lossy impedance expressions. In the first simulation, the dielectric loss tangent, tan_δ, was swept from 0.001 to 0.2, while the conductivity was set to a very large value (10^{25}), approximating a perfect conductor. By using a large conductivity, the skin depth will be smaller than the metal thickness at low frequencies so the impact of loss tangent on the impedance expressions can be examined. The dielectric constant, ε_r, was set to an arbitrary value of 4.1 for these simulations. Note that for the transmission plane model, the loss tangent and dielectric constant were set to these values at 1 MHz only; at other frequency points, the parameters vary according to the Debye model to capture the frequency dependence of the loss tangent and dielectric constant. For each value of tan_δ, all four expressions were evaluated and the loss tangent value was extracted as a function of frequency from the impedance. Specifically, the loss tangent was obtained from the phase of the impedance as follows

$$\tan\_\delta = \tan\big(\theta(\omega)\big) \tag{4.27}$$

where $\theta(\omega)$ is in radians. The loss tangent was extracted as a function of frequency. The upper frequency limit was chosen such that it was much less than the series resonance frequency, where the loss tangent can be reliably extracted from the impedance. *If* the four expressions placed no limitations on the value of the loss tangent and the expressions were causal, the extracted loss tangent values would match the simulated values across the range of extraction frequencies.

Figure 4.8 plots the percentage difference in the extracted loss tangent value over a range of extraction frequencies and loss tangent values for all four expressions. The light losses formula, in Figure 4.8(a), shows the highest overall difference in the extracted loss tangent value due to the explicit assumption about losses in this formulation (i.e., $k' >> k''$). For loss tangent values less than or equal to 20%, the difference is better than 1%. Figure 4.8(b) and Figure 4.8(c) show that the difference in the extracted loss tangent is negligible over a wide range of loss tangent values. Notice that, for these two plots, the error is increasing as the loss tangent decreases; although the conductivity is high, the δ/h term in the denominator starts to influence the extraction of loss tangent as tan_δ is made progressively smaller. With higher loss tangent values, at higher extraction frequencies, Figure 4.8(b) and Figure 4.8(c) show less difference in the extracted loss tangent value, as the influence of the δ/h term becomes negligible. Finally, Figure 4.8(d) plots the difference in the extracted loss tangent using the transmission plane model; this model shows the

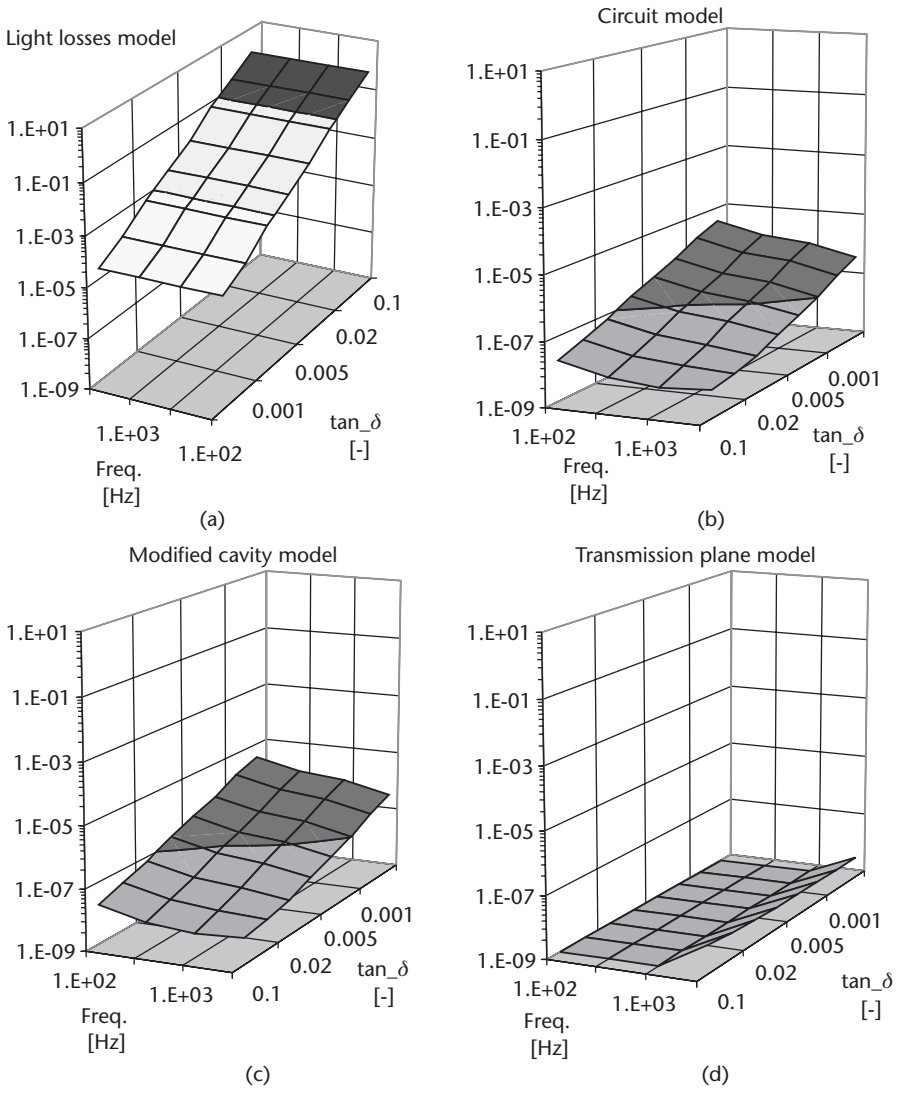


Figure 4.8 Surface plots of the percentage difference in the extracted loss tangent across a range of extraction frequencies and loss tangent values using the (a) light losses model, (b) circuit model, (c) modified cavity model, and (d) the transmission plane model.

lowest overall difference in the extracted loss tangent of the four lossy plane expressions.

In the second batch of simulations, the dielectric loss tangent was fixed to a low value (0.0001) to approximate a lossless dielectric, while the conductivity was swept over a large range. In particular, the base copper conductivity (5.8×10^7) was multiplied by 1, 10^3, 10^6, 10^{12}, and 10^{18}. The large range of conductivity values was chosen to evaluate the limits of the expressions not (necessarily) to represent practical values. By using a low dielectric loss, the impact of the metal conductivity on the impedance expressions can be examined. The dielectric constant, ε_r, was set to an arbitrary value of 4.1 for these simulations. As before, the dielectric constant and

loss tangent were only fixed to these values at 1 MHz for the transmission plane model. At each conductivity multiplier, all four expressions were evaluated and the loss tangent and dielectric constant was extracted as a function of frequency from the impedance. The dielectric constant was obtained directly from the imaginary portion of the impedance as follows

$$\varepsilon_r(\omega) = -\frac{h}{\omega\left(\mathrm{Im}\left(Z(\omega)\right) - \omega L\right)\varepsilon_0 w_x w_y} \tag{4.28}$$

where L is the inductance of the plane at the series resonance. If the four expressions placed no limitations on the conductor losses and the expressions were causal, we expect the extracted loss tangent and dielectric constant values to match the simulated values across the range of extraction frequencies.

Figure 4.9 plots the difference in the extracted dielectric loss using the four different impedance formulations. Figures 4.9(a) through 4.9(c) show a sharply increasing difference in the extracted dielectric loss as the conductivity is reduced. Also, there is a slight increase in the difference with decreasing frequency. Both of these trends are due to skin effects; only at very high conductivities and/or at high frequencies do we find skin effects be minimized. For the base copper conductivity (i.e., multiplier of 1), the error in the extracted loss tangent is very significant due to skin effects. Figure 4.9(d) plots the difference in the extracted loss tangent using the transmission plane model. This model shows the lowest overall difference in the extracted loss tangent of the expressions. The increase at the lowest conductivity values is quite moderate (0.01%).

Figure 4.10 plots the difference in the extracted dielectric constant using the four different impedance formulations. Figures 4.10(a) through 4.10(c) show very significant differences in the extracted dielectric constant as the conductivity is reduced due to skin effects. Figure 4.10(d) plots the difference in the extracted dielectric constant using the transmission plane model. This model shows no dependence of the dielectric constant on the copper conductivity.

Finally, we present a simple work-around for avoiding the roll-off at low-frequencies due to skin effects observed in most of the lossy impedance expressions. For example, (4.23) shows that the low-frequency roll off becomes significant when the skin depth is approximately equal to or greater than the dielectric thickness, h. If we substitute the following modified expression for the skin depth, δ_{mod}, then we can "clip" the skin depth at low frequencies, thereby avoiding the roll-off while still maintaining the proper skin effect behavior at high frequencies:

$$\delta_{\mathrm{mod}} = \frac{1}{\frac{1}{\delta} + \frac{1}{t}} \tag{4.29}$$

where t is the thickness of the upper and lower planes. As an example, δ_{mod} was substituted into the modified plane impedance expression, which assumes light losses (4.6) through (4.7). Figure 4.11 plots the plane impedance for the structure shown in Figure 2.1 using the light-losses cavity model and using the modified light losses cavity model, which uses (4.29). The inclusion of (4.29) is observed to remove the

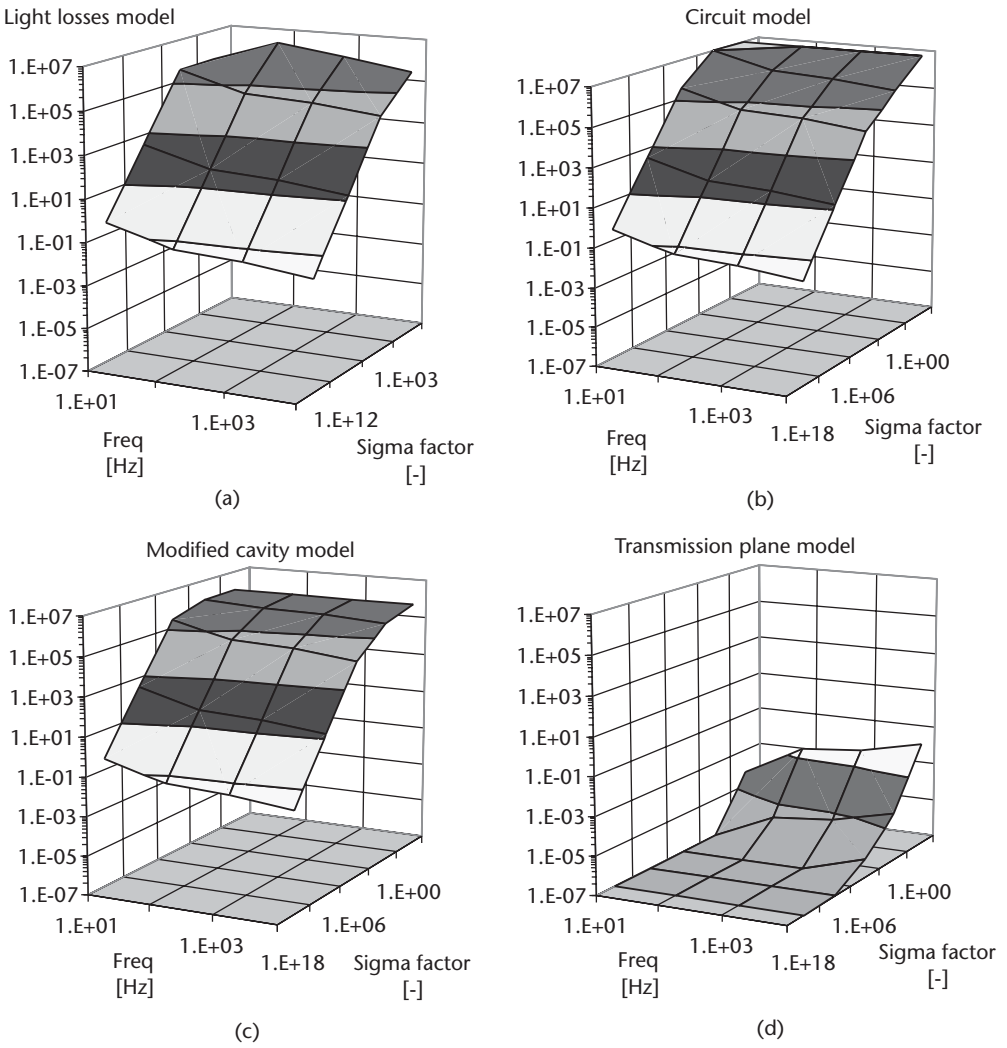


Figure 4.9 Surface plots of the percentage difference in the extracted dielectric loss across a range of extraction frequencies and copper conductivity values using (a) the light losses model, (b) circuit model, (c) modified cavity model, and (d) the transmission plane model. The *sigma factor* is a multiplicative constant applied to base copper conductivity.

low-frequency roll-off due to skin effects. Of course, the limitation on the light losses are not removed by this technique. However, as we observed from the error plots, inaccuracy due to dielectric losses only start being significant at very high tan_δ values.

4.2.2 Analytical Plane Models for Arbitrary Plane Shapes

The analytical plane models are based on the cavity modal resonances; in their original forms as shown above, they are all limited to rectangular plane shapes. The analytical models can still be applied to irregular-shape power-ground plane pairs by using the segmentation method [13, 14]. First we approximate the irregular plane

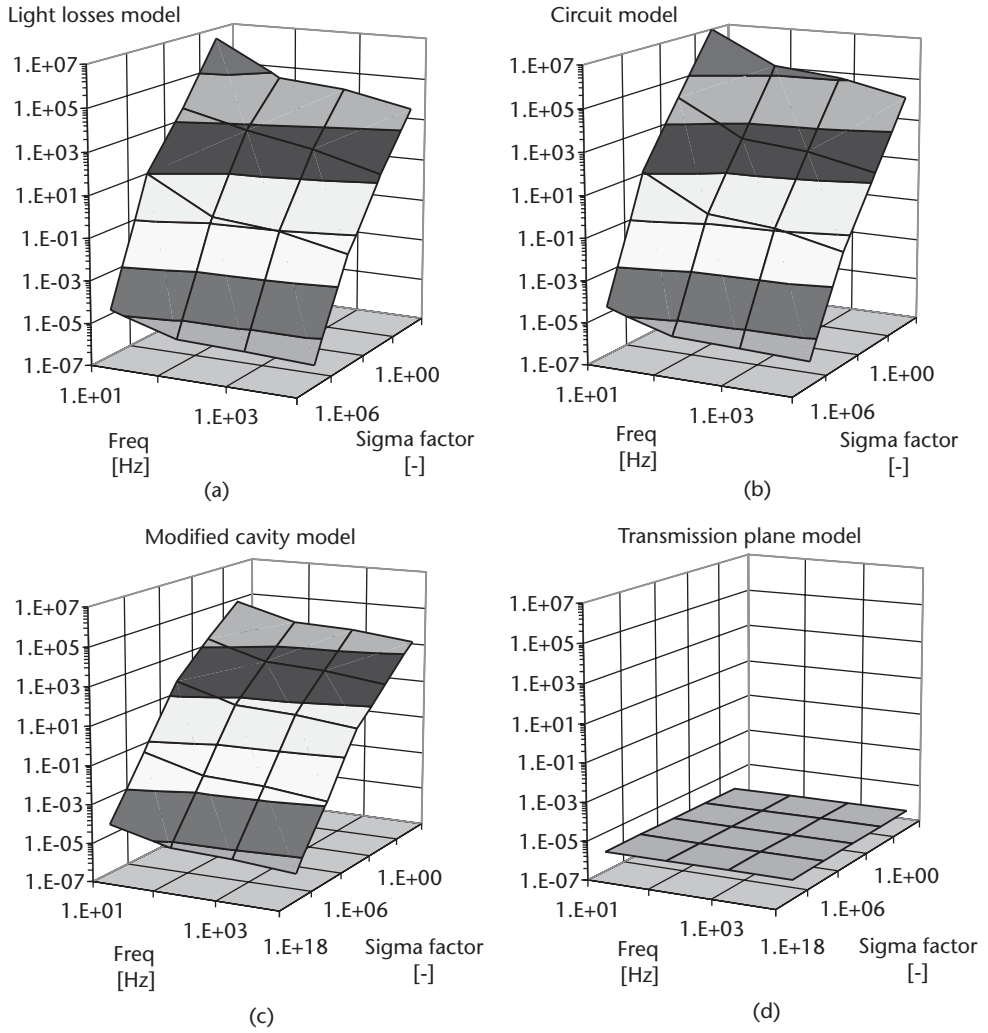


Figure 4.10 Surface plots of the percentage difference in the extracted dielectric constant across a range of extraction frequencies and copper conductivity values using the (a) light losses model, (b) circuit model, (c) modified cavity model, and (d) the transmission plane model. The *sigma factor* is a multiplicative constant applied to base copper conductivity.

shape with the sum of a series of rectangular shapes; these shapes approximate the irregular plane shape with sufficient accuracy. Second, we assign temporary ports along the sides of neighboring rectangular shapes. By enforcing the continuity of voltages and currents at the temporary ports, the impedance matrix of the combined rectangles can be obtained. The process is illustrated with a simple L shape, which is decomposed into two rectangles, as shown in Figure 4.12.

The illustration is based on the fact that along the marked line we can decompose the L shape into two rectangles, marked as α and β on the right. The sum of the two shapes make up the original shape, marked γ. Furthermore, we assume that before the cut, there are p and q ports in segments α and β, respectively. After the cut, two matching sets of temporary ports are added along the cut line to the two segments. To get sufficient accuracy from the segmentation method, the temporary

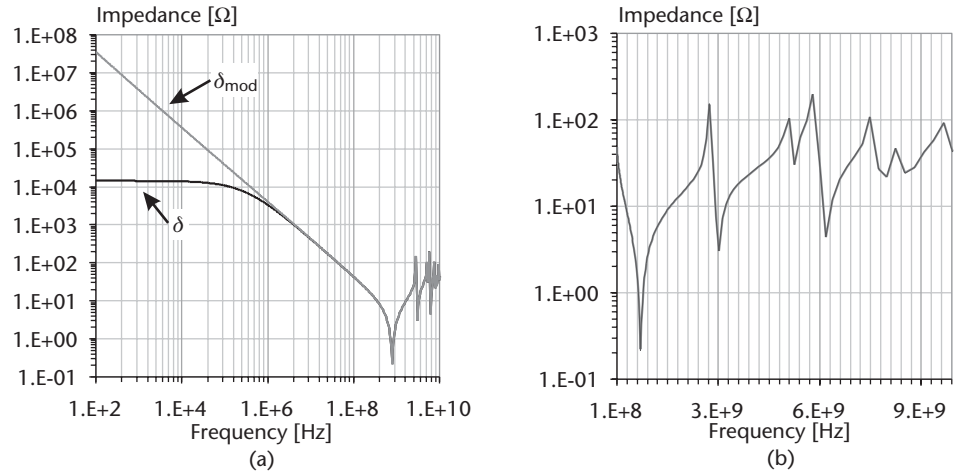


Figure 4.11 Impedance profile obtained using the light losses cavity model with and without (4.29). Part (b) is an enlarged view of (a) showing that the two approaches yield identical high frequency results.

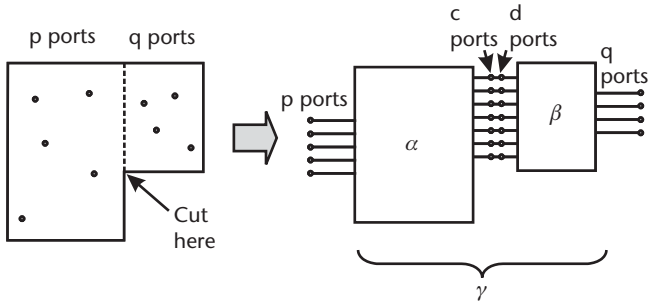


Figure 4.12 Illustration of the segmentation method to calculate the impedance matrix of irregular plane shapes.

ports have to be assigned with a spacing much less than the shortest wavelength of interest; these temporary ports are marked as *c ports* and *d ports* on the figure. The impedance matrices for α, β and γ can be partitioned into sub matrices corresponding to the c, d, p, and q sets of ports:

$$Z_\alpha = \begin{bmatrix} Z_{pp\alpha} & Z_{pc} \\ Z_{cp} & Z_{cc} \end{bmatrix}, \quad Z_\beta = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq\beta} \end{bmatrix}, \quad Z_\gamma = \begin{bmatrix} Z_{pp\chi} & Z_{pq} \\ Z_{qp} & Z_{pp\gamma} \end{bmatrix} \tag{4.30}$$

At the temporary ports, voltages and currents must equal on the two sides. From this condition we get:

$$Z_\gamma = \begin{bmatrix} Z_{pp\alpha} - Z_{pc} Z'_{dp} & Z_{pc} Z'_{dq} \\ Z_{qd} Z'_{dp} & Z_{qq\beta} - Z_{qd} Z'_{dq} \end{bmatrix} \tag{4.31}$$

where

$$Z'_{dp} = \left[Z_{cc} + Z_{dd}\right]^{-1} Z_{cp}, \quad Z'_{dq} = \left[Z_{cc} + Z_{dd}\right]^{-1} Z_{dq} \tag{4.32}$$

Once the impedance matrix for the entire plane shape is available, the matrix size can be reduced by eliminating the entries corresponding to the temporary ports.

4.3 Transmission-Line Models

Although transmission-line models are better suited for rectangular plane shapes, the approach can be extended to handle irregularly shaped planes using adaptive gridding or transmission matrix models.

4.3.1 Transmission-Line Grid Models for Rectangular Plane Shapes

As shown in Figure 4.13, rectangular plane shapes can be discretized by overlaying a square or rectangular grid, which divides the planes into unit cells [15–17]. The unit cells can be square; this will result in a different number of cells along the two axes for a rectangular plane. Alternately, the same number of cells can be used along both axes; this method retains the aspect ratio of the planes in the unit cell.

Each cell is then substituted with an equivalent circuit; this circuit represents the transmission-line behavior along the unit cell's sides or along their center lines. Figure 4.14 shows the two fundamental options in terms of assigning transmission lines to unit cells. When transmission lines are assigned to the borders of the unit cells, the resulting SPICE grid is closed, with no floating nodes. The transmission lines along the periphery, however, represent only half of the area compared to transmission lines inside the grid. It is easy to compensate for this by adjusting the parameters of the lines along the periphery.

When the transmission lines are assigned to the center lines of the unit cells, all of the transmission-line segments horizontally or vertically will have the same parameters, but now we encounter different problems: segments facing the plane edges will create open nodes, and portions of the original plane area along the edges will not be covered. These can be corrected for by applying dummy elements at the open ends to eliminate floating nodes and correcting for the uncovered plane area.

There are several possible options to model the transmission behavior in the unit cells. Some of the options are shown in Figure 4.15. Discrete RLGC circuits with fixed parameters can be used in either time or frequency-domain SPICE simulations; but, except for the lossless case, the model is not causal. Causal frequency-dependent RLGC parameters can be approximated with more complex subcircuits; each

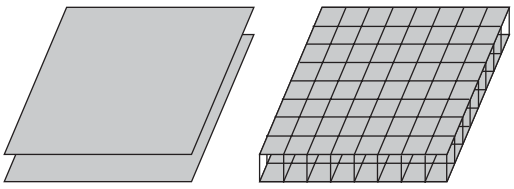


Figure 4.13 Discretization of a rectangular plane pair into unit cells.

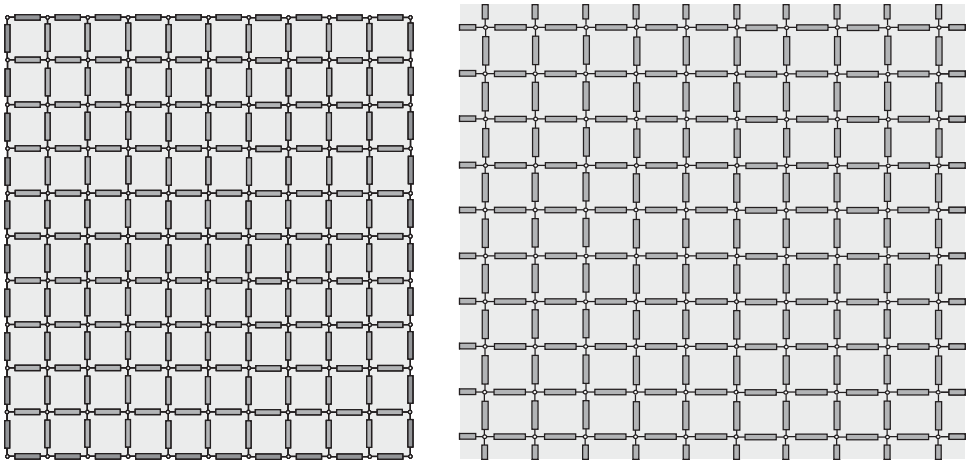


Figure 4.14 Mapping unit cells to transmission lines.

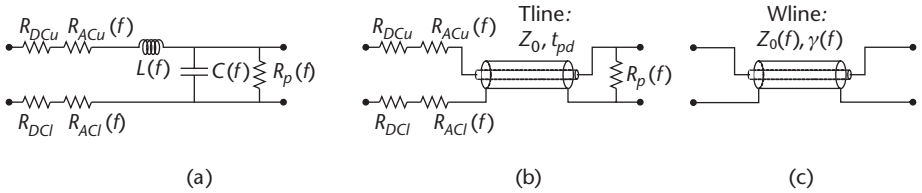


Figure 4.15 Circuit representation options for the unit cell transmission lines: (a) discrete RLGC circuit elements, (b) T line with external components, and (c) lossy W-element.

element is still frequency independent, but this approximation may significantly increase the number of nodes and the run time. For ac simulations only, frequency-dependent RLGC parameters can be defined. As a further option, we can use the built-in SPICE transmission line models: either the lossless T line, with optional external components to approximate losses, or the lossy W-line element. However, we have to keep in mind that by using transmission-line elements we loose the horizontal connectivity along the unit cells because the input and output potentials of the transmission-line elements are floating with respect to each other.

The transmission-line matrix model, also called the *bedspring model*, can capture arbitrary losses and different thicknesses and/or different conductivities in the upper and lower conductive planes.

To obtain the unit-cell parameters, we can start with the lossless characteristic impedance and propagation delay expressions and then add losses as perturbation. The quasi-static approximation of plane capacitance, C, calculates the plate capacitance for the cell area represented by the transmission line. The propagation delay, t_{pd}, along the length of the cell gives the second independent parameter. From the capacitance and propagation delay, the two dependent parameters, the characteristic impedance, Z_0, and the inductance, L, can be derived from the basic transmission-line equations:

$$t_{pd} = \sqrt{LC}, \quad L = \frac{t_{pd}^2}{C}, \quad Z_0 = \sqrt{\frac{L}{C}} \tag{4.33}$$

Conductive losses can be calculated separately for the upper and lower planes. The frequency-dependent resistance can be easily used in ac SPICE simulations. The model approximates the conductive loss, R, as the sum of dc resistance, R_{dc}, and skin resistance, R_{skin}, assuming a $\sqrt{f}$ frequency dependence for the skin resistance:

$$R = R_{dc} + R_{skin}, \quad R_{skin} = R_s\sqrt{f} \tag{4.34}$$

The parallel conductance, G, is the sum of the dc conductance, G_{dc}, and the dielectric loss, G_{diel}, which is assumed to have approximately linear frequency dependence.

$$G = G_{dc} + G_{diel}, \quad G_{diel} = G_d f \tag{4.35}$$

Note that (4.33) through (4.35) still do not result in causal solutions, because the frequency dependencies of L and C are not included. If necessary, causal solutions can also be included by using the causal RLGC solution described in Section 4.5.5.2.

4.3.2 Transmission-Line Grid Models for Arbitrary Plane Shapes

There are several limitations related to uniform rectangular SPICE grids applied to arbitrary power plane shapes [18]. As an example, consider the power-ground plane shape of Figure 4.16.

Figure 4.17 shows the outline of the inner plane shape with a 6.35-mm (0.25-inch) geometrically uniform square grid fitted over its envelope. The uniform

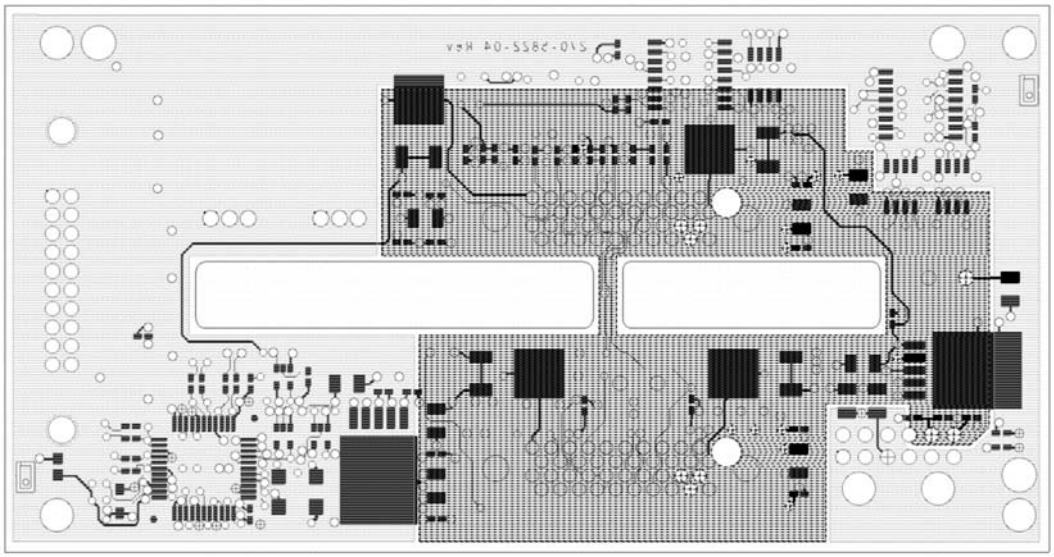


Figure 4.16 Within the outer rectangular board outline, there is an inner odd-outline plane shape with a varying degree of perforations, due to smaller and larger holes, as well as with a large cutout.

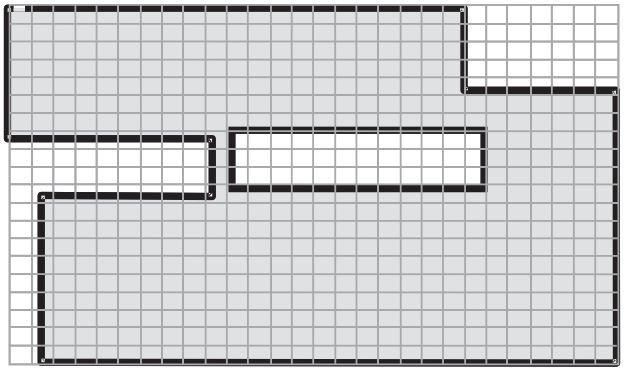


Figure 4.17 Outline of the highlighted inner plane pair shape from Figure 4.16, with a uniform square-unit-cell SPICE grid laid over it. Each side of the overlaid grid cells represents one piece of transmission line in the equivalent SPICE circuit.

grid has 28 cells horizontally and 20 cells vertically, totaling $28 \times 20 = 560$ cells and $(28 + 1) \times (20 + 1) = 609$ nodes.

Figure 4.17 shows that dependent on the actual outline and cutouts, there may be unnecessary cells and nodes in the uniform grid. In this example, out of the total of 560 cells (and 609 nodes), altogether there are 91 cells outside of the actual plane shape we want to simulate. Another problem with using uniform rectangular grids for irregular shapes is that in SPICE, run time grows sharply as the number of nodes increases. Any unnecessary nodes increase the run time without the benefit of higher resolution/accuracy. Furthermore, there may be areas where smaller grid cells may be necessary (e.g., around odd-shaped outline contours or in perforated areas); if the entire plane is meshed with the smallest grid size, the total grid number may again increase unnecessarily. Finally, modal resonances may not be captured correctly with uniform grids. One of the major roles of SPICE models of planes is to capture modal resonances so that bypass capacitors can be applied properly to smooth out the impedance profile. Modal resonance frequencies depend on the possible standing-wave pattern; that pattern is determined by the actual boundary shapes and cutouts. If it is not captured accurately, the simulated resonance frequencies are in error.

To handle complex outline shapes, results are shown below using an adaptive, variable-size cell SPICE grid. The shape is more coarsely gridded in solidly filled areas and gradually converges into a finer mesh around the shape's outline and (possible) inner cutout contours by using square unit cells. The resulting SPICE grid preserves the actual static plane-capacitance by dropping cells completely that are not at least partly on the plane shapes and adjusting the electrical parameters of unit cells that are either not entirely on the plane shape or are not solidly filled (e.g., due to antipads).

In each unit cell, the amount of metal within the unit cell's area is calculated separately for the two conductive planes; the conductive loss values are adjusted according to those fill ratios. The common set of the two planes' metal contents is also calculated (as shown in Figure 4.18), and this is used to adjust the transmission characteristics of the SPICE grid elements.

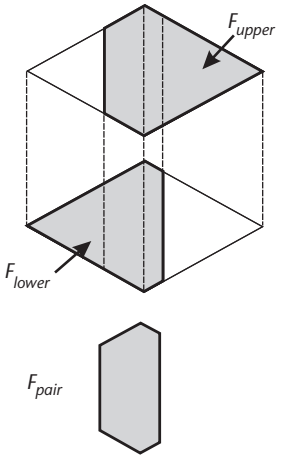


Figure 4.18 Illustration of metal fill ratios used for the adaptive grid.

To further preserve the static capacitance value of planes, as indicated in Figure 4.19, compensating capacitors are introduced in the SPICE grid to account for the missing coverage on the boundary of different-size unit cells.

Finally, following the same procedure, multiple plane pairs connected in parallel by vias can be handled as separate pairs first, then the SPICE grids of individual pairs can be linked. Figure 4.20 shows the adaptive grid for the example plane shape. Figure 4.21 shows the measured impedance profile compared to the simulated responses with uniform and adaptive variable-size cell grid.

Note that the adaptive grid captures the static capacitance and the modal resonances accurately. Since the uniform rectangular grid follows the outer envelope of the shape, it overestimates the static capacitance (as it does not account for the cutouts and missing portions along the jagged outline); it also overestimates the first modal resonance frequency. However, with the rectangular uniform grid, both conditions cannot be met at the same time by adjusting the envelope of the rectangular uniform grid: any attempt to decrease the outline to match the static capacitance more closely would increase the predicted first modal resonance frequency further, and vice versa.

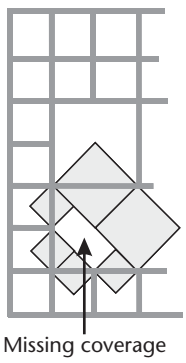


Figure 4.19 Compensation for missing unit-cell coverage.

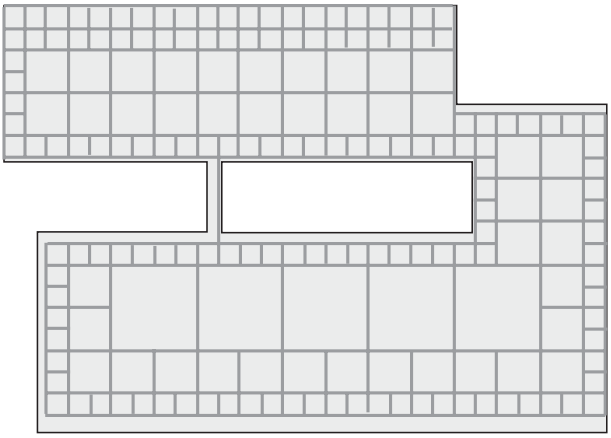


Figure 4.20 Result of adaptive subgridding on the inner plane shape shown in Figure 4.16.

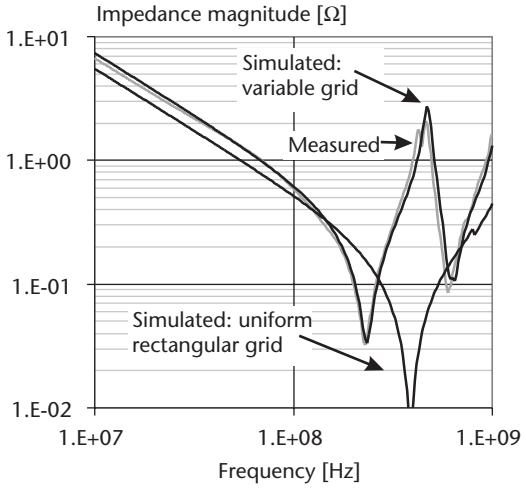


Figure 4.21 Impedance profiles of the inner plane shape shown in Figure 4.16, obtained from measurement and simulation using a rectangular uniform grid and adaptive grid.

The first modal resonance from the propagation delay along the longer side of the rectangular envelope can be calculated from the length and dielectric constant: it is 800 MHz for the first peak. Note that there is a small glitch at around 800 MHz in the impedance simulated with a rectangular uniform grid. It is not pronounced because of the location of the test point. If the plane had no cutout and were to follow the rectangular outline of the envelope, the modal resonance would be highly suppressed at this same location. However, due to the odd outline and cutout of the inner plane shape, the actual plane cut has a much lower first modal resonance frequency, about half of the frequency obtained from the uniform grid.

The dual peak at the first modal resonance in the measured impedance profile of Figure 4.21 is the result of a trace passing over both the inner and outer plane shapes shown in Figure 4.16. This was proven in measurement by cutting the inner plane shape along its periphery, thus cutting the trace while leaving intact the inner plane

shape, and then remeasuring. Figure 4.22(a) shows the new measured impedance profile compared against the impedance profile obtained with the same adaptive grid that was used for Figure 4.21. Figure 4.22(b) shows the simulated results using Ansoft SIwave to analyze the whole board shown in Figure 4.16. The board was simulated, including and excluding coupling from the trace to the inner plane shape (all other coupling was enabled). The simulation results demonstrate that the trace that crosses over the inner and outer plane shapes is responsible for the dual peak observed in the measurement results shown in Figure 4.21.

To capture in simulation the coupling between split plane shapes using the adaptive grid mode, both plane shapes can be modeled with its own adaptive grid and the nodes along the interfacing contour can be connected with coupling capacitors to represent the plane-to-plane edge capacitance between the two shapes [19].

4.3.3 Transmission Matrix Model for Arbitrary Plane Shapes

The transmission matrix model [20] can be used to model both rectangular and arbitrary plane shapes. The method relies on the fact that power planes are linear networks, and as such the plane can be subdivided into smaller networks and the networks cascaded. The overall network response is simply the product of the individual transfer matrices. (Note that only transfer matrices are multiplicative, others, like [*S*] or [*Z*] are not.) This technique can be applied to irregular plane geometries, like the L-shaped structure in Figure 4.23. Although the size of the matrices associated with sections 1 and 2 of Figure 4.23 do not match, the matrix array for section 2 can be padded with zero matrix elements to match the matrix size of section 1.

The transmission matrix method starts with dividing the plane into unit cells, as shown in Figure 4.23. Each cell is represented by an equivalent circuit representation using either T or Π models. Starting with plane section 1 in Figure 4.23, the larger

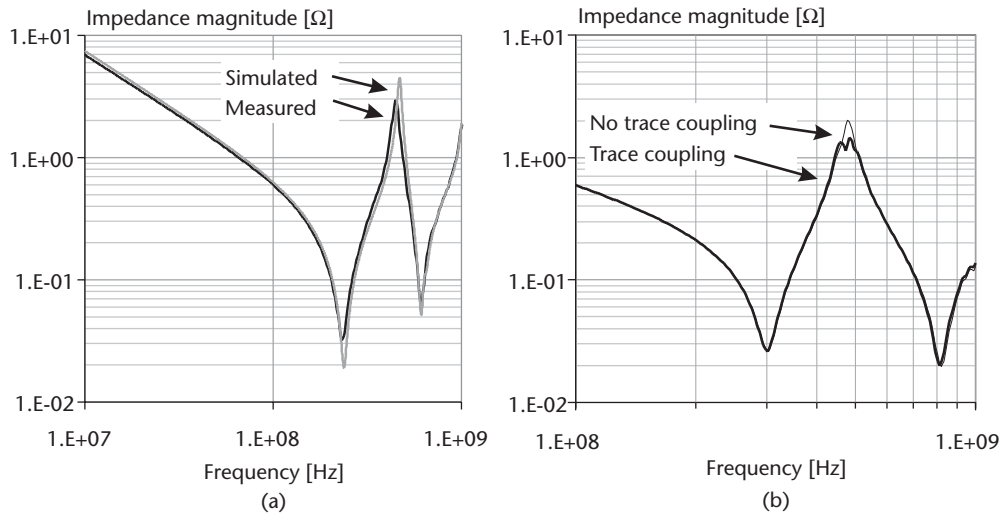


Figure 4.22 (a) Impedance profiles of the inner plane shape shown in Figures 4.16 obtained from measurement and simulation using an adaptive grid. Measured after cut around plane periphery. Part (b) shows field solver results.

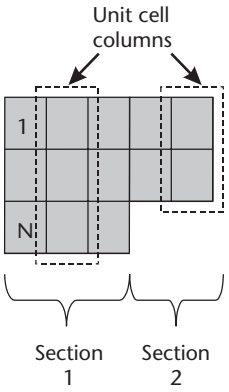


Figure 4.23 Top view of an L-shaped plane.

rectangular shape can be represented by a number of unit cell columns, in this case 3. Each $N \times 1$ unit cell can be represented as a $2N \times 2N$ matrix formed by N input ports and N output ports. Thus the transmission matrix for section 1 is a 6×6 matrix

$$[T_1] = \begin{bmatrix} T_{11} & T_{12} & T_{13} & T_{14} & T_{15} & T_{16} \\ T_{21} & T_{22} & T_{23} & T_{24} & T_{25} & T_{26} \\ T_{31} & T_{32} & T_{33} & T_{34} & T_{35} & T_{36} \\ T_{41} & T_{42} & T_{43} & T_{44} & T_{45} & T_{46} \\ T_{51} & T_{52} & T_{53} & T_{54} & T_{55} & T_{56} \\ T_{61} & T_{62} & T_{63} & T_{64} & T_{65} & T_{66} \end{bmatrix} \tag{4.36}$$

Equation (4.36) can be rewritten in a simpler form:

$$[T_1] = \begin{bmatrix} T_{1A} & T_{1B} \\ T_{1C} & T_{1D} \end{bmatrix} \tag{4.37}$$

where $[T_{1A}]$, $[T_{1B}]$, $[T_{1C}]$, and $[T_{1D}]$ are 3×3 matrices. Then the overall network for section 1 (of Figure 4.23) can be obtained by multiplying the individual matrices for each column. Since all the matrices for each of the three columns are the same, the response for the entire geometry can be obtained from a single 6×6 matrix as follows

$$[T_m] = [T_1]^3 \tag{4.38}$$

If the input and output ports are open circuited, then the $[T_m]$ would be multiplied by the identity matrix as follows

$$[T'] = [I_L][T_m][I_R] \tag{4.39}$$

Then section 2 of Figure 4.23 can be included by modifying the identity matrix on the right side of (4.39), $[I_R]$, as follows. The transmission matrix for section 2 is a 4×4 matrix that can be written as:

$$[T_2] = \begin{bmatrix} T_{11} & T_{12} & T_{13} & T_{14} \\ T_{21} & T_{22} & T_{23} & T_{24} \\ T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \end{bmatrix} \tag{4.40}$$

which can then be incorporated into the identity matrix, $[I_R]$, as follows:

$$[I'_R] = \begin{bmatrix} T_{11} & T_{12} & 0 & T_{13} & T_{14} & 0 \\ T_{21} & T_{22} & 0 & T_{23} & T_{24} & 0 \\ 0 & 0 & I & 0 & 0 & 0 \\ T_{31} & T_{32} & 0 & T_{33} & T_{34} & 0 \\ T_{41} & T_{42} & 0 & T_{43} & T_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & I \end{bmatrix} \tag{4.41}$$

The transmission matrix for the entire structure is then

$$[T'] = [I_L][T_m][I'_R] \tag{4.42}$$

Knowing the transmission matrix for the network, one can now determine the impedance matrix $[Z]$, including the impedance at specific points on the plane.

4.4 Effect of Plane Parameters on Self- and Transfer Impedances

In this section, we examine how the plane parameters influence the plane impedance and resonances. Specifically, the impact of the dielectric thickness, plane thickness, number of power ground plane pairs, and dielectric constant and dielectric loss on the plane impedance is discussed [21]. The rectangular plane structures were simulated using the transmission-line grid method with lossless transmission lines and external components to approximate the losses. Even though the model is noncausal, it is sufficiently accurate to show how the impedance profile changes as a function of the plane parameters.

4.4.1 Impact of Dielectric Thickness with Regular Conductors

Resonances of bare planes can contribute to and increase simultaneous switching noise, ground bounce, or V_{cc} bounce. Thin dielectric materials by themselves can effectively help to suppress plane resonances of bare boards. The mechanism responsible for this is best understood by looking at the real part of the propagation constant of the transmission line segments in the equivalent model circuit. The attenuation of a matched interconnect is:

$$A(f)^{dB} = 4.35\left(\frac{R_s(f)}{Z_o} + G_d(f)Z_o\right) \tag{4.43}$$

where Z_0 is the characteristic impedance of the transmission line, and $R_s(f)$ and $G_d(f)$ are the series conductive and parallel dielectric loss values versus frequency. As the dielectric thickness decreases, skin effect losses remain constant, but the characteristic impedance, that is, $Z_0 = \sqrt{L/C}$, decreases proportionally with the dielectric thickness. This happens because inductance and capacitance are proportional and inversely proportional to the dielectric thickness, respectively. With decreasing dielectric thickness, the dielectric loss term eventually decreases, thus leaving the skin loss responsible for the suppression of plane resonances. This simple approximation shows how thin dielectrics between power and ground planes have tremendous advantages for power distribution systems at high frequencies.

A uniform rectangular lossy SPICE grid model was applied to simulate a pair of 25×25 cm (10×10 inch) parallel planes with 35-μm (1-oz) copper on either side, but with variable thickness of dielectric separation. The dielectric constant was assumed to be 4. The grid size was 20×20, providing at least 1 GHz of useful upper limit for the model.

Figure 4.24 shows the magnitude and phase of simulated self-impedance measured between the upper and lower planes at the center. As the dielectric thickness is reduced, the impedance profile becomes smoother at high frequencies. There is another obvious advantage: due to the increase of static capacitance, the low-frequency impedance is reduced. In turn, this reduction helps to reduce the need for low-frequency bulk capacitors. Furthermore, this results in a complete suppression of plane resonances for dielectric thicknesses below 8 μm (0.3 mil). Phase figures manifest this trait as well [see Figure 4.24(b)]; with thin dielectrics, the phase of the self-impedance becomes more resistive. Also note that the slant of the self-impedance magnitude at high frequencies is due to the increase of skin resistance with the square root of frequency. Figure 4.25 proves the assumption that increasing series losses create a low-pass transfer function. While dielectric thicknesses above 25 μm (1 mil) yield a transfer function with noticeable peaks at high frequencies. A thickness of 2.5 μm (0.1 mil) creates a flat response. Even a thinner dielectric separation provides a monotonic low-pass function. The series losses also increase the upper

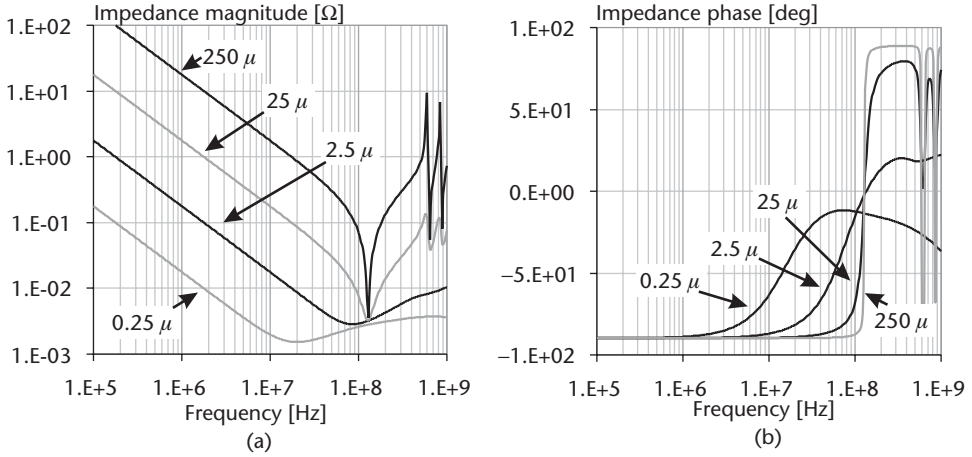


Figure 4.24 Effect of dielectric thickness on the self impedance of a pair of 25×25 cm planes, with 35-μm copper on either side. (a) The simulated self-impedance magnitude and (b) the phase are probed at the center of planes.

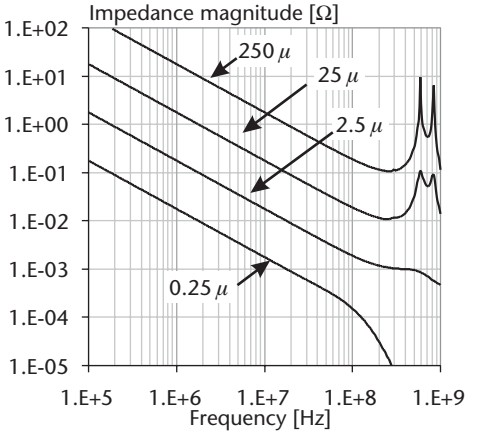


Figure 4.25 Effect of dielectric thickness on the transfer impedance of a pair of 25 × 25 cm planes, with 35-μm copper on either side. The simulated magnitude of the transfer impedance is probed between the center and one of the corners of the planes.

frequency limit of the simulation model by reducing the reflections, thereby effectively creating a resistor rather then transmission line grid at high frequencies. The illustrations in this section are shown for 10 × 10-inch plane sizes, smaller plane shapes result in higher characteristic impedance. Hence, from (4.43) the damping of resonances due to conductive losses will be less.

4.4.2 Impact of Plane Thickness

While the advantages of thin dielectrics are clear from the simulations results of Figures 4.24 and 4.25, it is not easy to manufacture and process a very thin dielectric layer of a few micrometer or less thickness with the usual several micrometer or more copper layers. With a 0.25-μm (0.01-mil) dielectric layer, the conductor layers may be about 100 times thicker.

To look at the other possible extreme, Figures 4.26 and 4.27 show the same structure under the same assumptions as Figures 4.24 and 4.25, except the conductive layer on both sides is assumed to be 0.25-μm (0.01-mil) copper. Note that the skin depth in copper at 1 GHz is approximately 2 μm (0.08 mil); that depth is about eight times higher than the selected copper thickness. Hence the series loss resistance is less dependent on frequency. By comparing Figure 4.24 to Figure 4.26 and Figure 4.25 to Figure 4.27, we can see that the series losses of the 0.25-μm conductive layers still leave considerable peaking in the impedance profile with thick (> 25-μm) dielectric layers.

In case of thin conductive layers, the high-frequency impedance does not drop inversely proportionally to the plane separation (as one would expect based on the equivalent inductance between the planes). Because the impedance now becomes limited by the series ac loss resistance. With a 0.025-μm (0.01-mil) copper conductors, the self-impedance profile is almost totally flat, because near 10 MHz the impedance of the static capacitance intercepts the series resistance. The higher series resistance also creates stronger low-pass filtering.

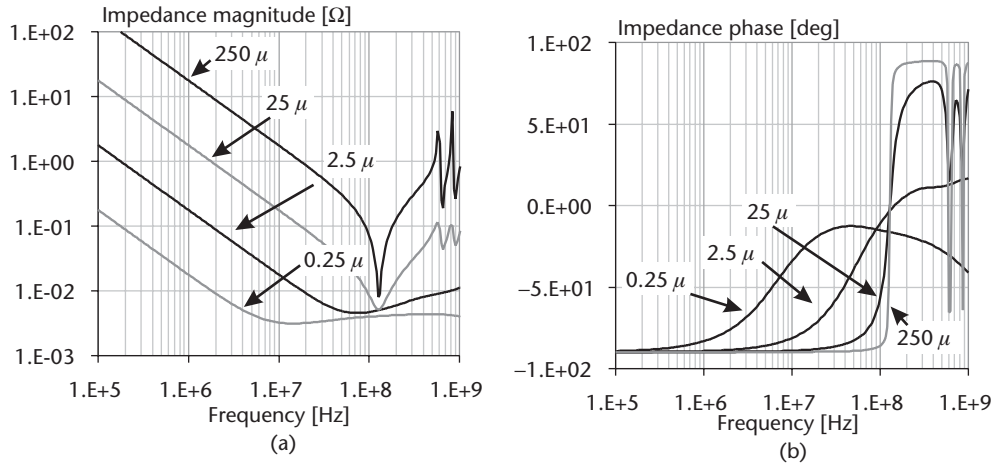


Figure 4.26 Effect of dielectric thickness on the self impedance of a pair of 25 × 25 cm planes, with 0.25-μm copper on either side. The simulated self-impedance (a) magnitude and (b) the phase, probed at the center of planes.

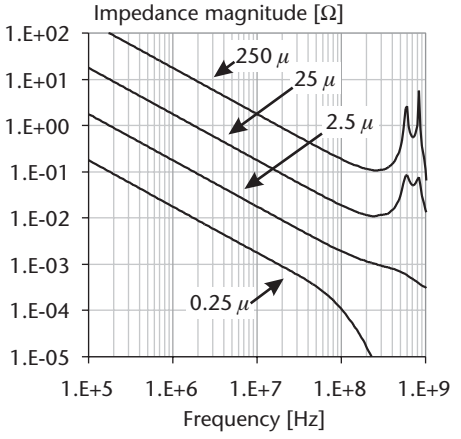


Figure 4.27 Effect of dielectric thickness on the transfer impedance of a pair of 25 × 25-cm planes, with 0.25-μm copper on either side. The simulated transfer impedance magnitude is probed between the two planes from the center to the corner.

On the other hand, using very thin conductive layers alone is not practical either because the copper weight may be needed to handle the large dc currents in the systems. However, by using both thin dielectric and thin conductive layers, we can provide the necessary copper weight by stacking up several of these thin layers. At the same time, this will reduce the impedance further because of the parallel connection of individual plane pairs. A typical 50-μm dielectric separation with 35-μm (1 oz) copper has a total thickness of 120 μm. If we used the 120 μm total thickness and we stacked up 240 pairs of 0.025-μm dielectrics with 0.025-μm conductive layers, we would end up with the same total thickness, same amount of total conductor weight on either side, and (neglecting the connecting impedance between the stacked lay-

ers) an approximately 25-$\mu\Omega$ flat resistive impedance in the 10–1,000-MHz frequency range. However, to use multiple thin conductive and dielectric layers in large-size rigid PCBs, several technological problems have to be addressed first.

4.4.3 Parallel Plane Pairs

Stacking power-ground plane pairs in parallel has most of its advantages if we reached the resistive bottom of the impedance profile with the thin dielectrics already. As illustrated in Figure 4.28, in the unsaturated range of the curves, a smoother impedance profile is obtained using one plane pair with thinner dielectrics as opposed to a stack of several thicker laminates.

4.4.4 Impact of Dielectric Constant and Dielectric Losses

The granularity of the power-ground plane models is important: each transmission line segment in the model should represent a small fraction of the wavelength of the highest frequency of interest. With a 15.24-cm (6-inch) square plane with 8×8 grid and $\varepsilon_r = 4$ dielectric constant, the accuracy of the model significantly deteriorates above 2 GHz. Since the propagation delay goes linearly with $\sqrt{\varepsilon_r}$, the same grid model is limited to about 1 GHz and 0.5 GHz, as the dielectric constant is increased to 16 and 64.

The typical PCB materials have been optimized for low-loss signal transmission; as a result, they do not provide sufficient suppression of plane resonances. If used only between the power/ground planes, intentionally high dielectric losses may be utilized. Figure 4.29 shows the effect of dielectric losses on the real part and magnitude of the self-impedance. The impedance magnitude curve show that a dielectric loss tangent of 0.3 or higher is sufficient to suppress almost completely the plane resonances.

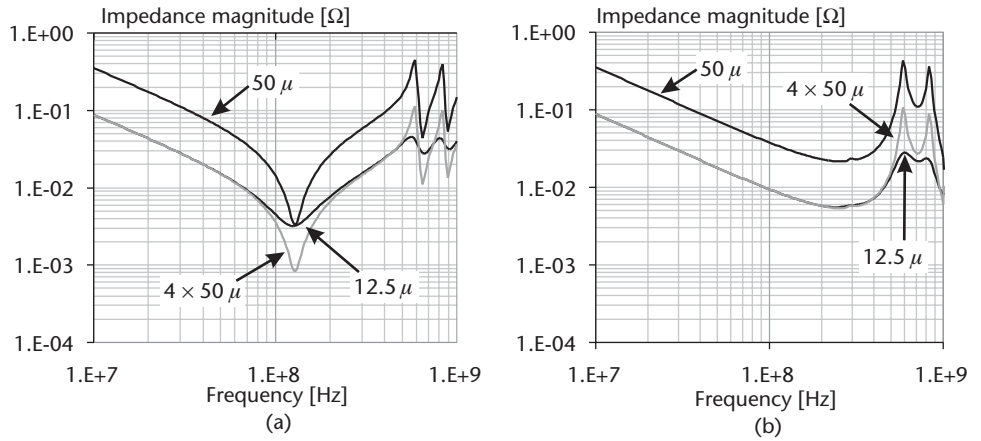


Figure 4.28 (a) Self- and (b) transfer impedance magnitude of a pair of 25×25 cm parallel planes with three different configurations: stand-alone pair with a 50-μm dielectric separation, stand-alone pair with a 12.5-μm dielectric separation and four pairs of planes with a 50-μm dielectric separation. The simulated self-impedance is probed between the planes at the center; transfer impedance is probed between the two planes from center to corner.

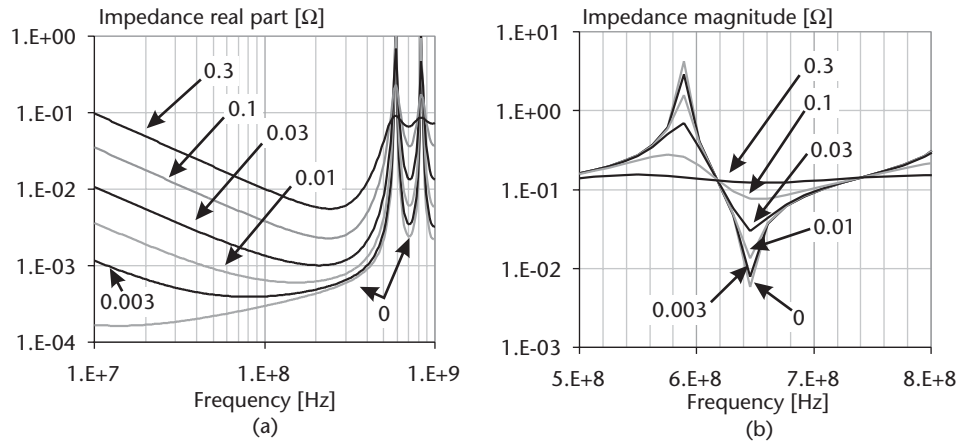


Figure 4.29 Effect of dielectric losses on the (a) real part and (b) magnitude of self-impedance measured at the center of a pair of 25 × 25-cm planes with a dielectric separation of 50-μm (2-mil), dielectric constant 4, and 35-μm (1 oz) copper.

4.4.5 Run Time Versus Number of Cells

The upper end of the valid frequency range of SPICE grid models depends linearly on the number of cells along each side. As the number of cells increases linearly along one side, the total number of cells and nodes in the SPICE equivalent circuit increases quadratically. The run time of SPICE is a nonlinear function of the number of nodes. Eventually, the total run time increases very sharply as we try to increase the upper frequency end by increasing the number of cells. Faster computers help, but the trend stays unchanged. Figure 4.30 shows the runtime as a function of number of cells along one side in a square grid. The run time is normalized to the value obtained with 10 cells along a side. Note that increasing the number of cells along a side from 5 to 30 (by a factor of 6) increases the number of cells and SPICE nodes by a factor of 36; this increases the run time by a factor of 91.

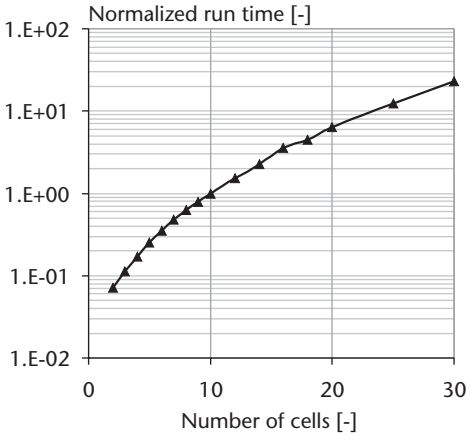


Figure 4.30 Normalized run time versus number of cells along one side of a square grid.

4.5 Characterization of Plane and Laminate Parameters

In this section, we discuss approaches to calculate the dc resistance of planes with and without perforations. We use these approaches to simulate the dc voltage drop on planes and characterize the mid- and high-frequency plane parameters.

4.5.1 DC Resistance of Planes

At high frequencies the plane thickness matters little, because the skin depth limits the current flow to a thin layer on the plane surface. At low frequencies (significantly below the frequency at which skin depth equals the plane thickness) the entire volume of plane carries the current. Especially in high-power applications, the dc resistance may become a major limiting factor. Therefore, it is important to understand how to characterize the plane resistance.

With the definitions of Figure 4.31, the dc resistance, R_{dc}, of a rectangular conductor shape composed of a homogeneous material of conductivity σ, can be calculated as:

$$R_{dc} = \frac{1}{\sigma}\frac{l}{wt} \tag{4.44}$$

where σ, l, w, and t are the conductivity of the plane in S/m, length, width, and thickness of plane in meters. Equation (4.44) assumes that not only the conductive material, but also the current flow is homogeneous in the material; in other words, the current distribution is assumed to be uniform through the entry and exit surfaces at the shaded sides. Equation (4.44) can be simplified by introducing the R_s sheet resistance:

$$R_s = \frac{1}{\sigma t}, \quad R_{dc} = R_s \frac{l}{w} \tag{4.45}$$

In printed circuit boards the typical conductor material is copper, either electrodeposited or rolled-annealed. The conductivity of raw bulk copper at room temperature is $\sigma = 5.8\text{E}^7$ S/m. The plane thickness is defined implicitly by the weight of the copper plane. The copper weight is given for 1 ft^2 (or 0.0929 m^2) of material. The density of copper is 8,920 kg/m^3. The weight of the copper is usually given in ounces where 1 oz is 28.35g. From the above numbers, a one-ounce copper plane corresponds to a nominal 34.2-μm plane thickness. Eventually, the porosity of material

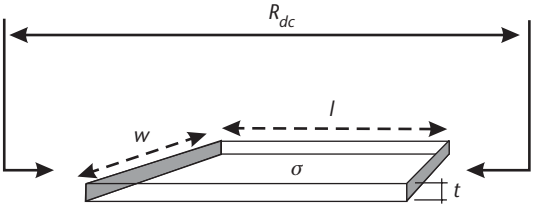


Figure 4.31 Parameters defining the dc resistance of a homogeneous rectangular plane between its opposing parallel sides.

and the surface roughness influence the sheet resistance also. The plane thickness may vary, too, with the processing steps during lamination. Treatment steps, especially when multiple repairs are used, will tend to reduce the plane thickness.

When the tooth structure of the copper has significant peaks and valleys with respect to the overall thickness of the plane, it is reasonable to assume that the dc resistance comes primarily from a plane thickness between the baselines of the tooth profiles, because we can expect little current to penetrate the individual bumps. The definition of equivalent plane thickness is illustrated in Figure 4.32.

Organic packages have copper planes; therefore the above numbers apply. For high-temperature cofired ceramic packages, the conductive layers are made of tungsten with a typical bulk resistivity of $7.5E^{-7}$ Ωm; this translates to $1.33E^{6}$ S/m, as opposed to $5.8E^{7}$ S/m for copper. The manufacturing process may require vent holes on solid planes; this perforation increases the resistance. The resistance increase can be calculated similar to the effect of the antipads.

Due to practical design constraints, using rectangular plane shapes with uniform current distribution is rather rare. A somewhat more practical scenario is when current spreads out in a radial fashion, for instance at the entry point around a copper slug. The spreading resistance is shown by the resistance of planes between two concentric circles.

With the definitions of Figure 4.33, the dc resistance, R_{dc}, of the homogeneous conducting plane between the concentric circles of radii r_1 and r_2 is given by:

$$R_{dc} = \frac{R_s}{2\pi} \ln\left(\frac{r_2}{r_1}\right) \tag{4.46}$$

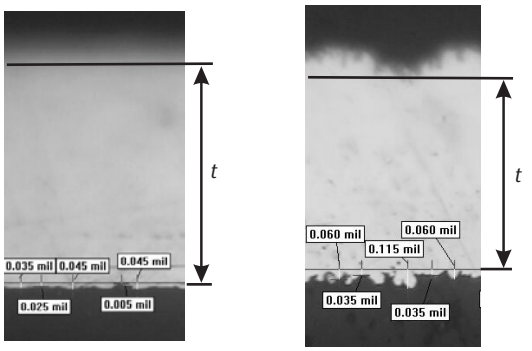


Figure 4.32 Cross sections of (a) rolled-annealed copper foil and (b) electrodeposited foil. Rough surface leaves less copper for current flow not only at high frequencies, but also at dc. (Courtesy of Sanmina-SCI.)

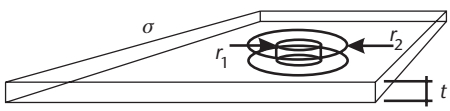


Figure 4.33 Parameters defining the dc resistance of a homogeneous solid rectangular plane between concentric circles.

where R_s is the sheet resistance in Ω-square and r_1 and r_2 are the radii of concentric circles in arbitrary but identical units. Here, too, the assumption is uniform current flow: the current density within each concentric circle is independent of direction.

Another realistic (but still simple) scenario is to calculate the resistance between two circular connections on a large plane. Reference [22] provides an approximate closed-form expression for the resistance. With the notions of Figure 4.34, and assuming a plane thickness of t, radii of connecting hemispherical electrodes of a, and electrode center-to-center spacing of d, the resistance is:

$$R_{ab} \approx \frac{1}{\pi\sigma a}\left[1+\frac{a}{t}\ln\left[\frac{\sqrt{1+\left(\frac{d}{2t}\right)^2}+1}{\sqrt{1+\left(\frac{a}{2t}\right)^2}+1}\right]\right] \tag{4.47}$$

4.5.2 Measuring DC Resistance of Planes

To measure the sheet resistance of a conductive foil, we can use the definition from Figure 4.31. A known number of squares can be measured by sending through a uniform dc current and then measuring the voltage drop. If we use a large number of squares (long, skinny plane shape), a single entry and exit point may be sufficient; all that needs to be measured is the voltage drop across one square of plane where the current is sufficiently uniform. Alternatively, to ensure uniform current distribution, the entry and exit connections can be formed of multiple connections. Figure 4.35 shows this measuring arrangement on a 25.4 × 2.54 cm (10 × 1 inch) strip of two-sided PCB laminate with 1-oz copper on either side. The copper foils are shorted at the end to create a loop. Eight power resistors are soldered to the copper foil, four to each end.

By measuring the voltage drop along a known number of squares generated by a uniform current, we obtain the sheet resistance directly. The accuracy of measurement depends on how accurately we can measure the voltage and current across the plane as well as how accurately we can count the number of squares. Larger plane sizes make it easier to maintain good accuracy when we cut and trim the conductive sheet.

In a finished package or PCB, measuring the dc resistance of the planes is not easy, usually because we do not have the number of connection points necessary for accurate measurements. If we measure around vias, the spreading resistance at the entry and exit points will distort the data. However, we can measure the dc drop on the planes with respect to a selected reference point. When we measure dc voltage,

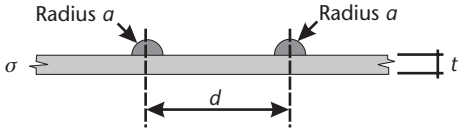


Figure 4.34 Two identical hemispherical electrodes of radii a on a plate of finite conductance and thickness of t.

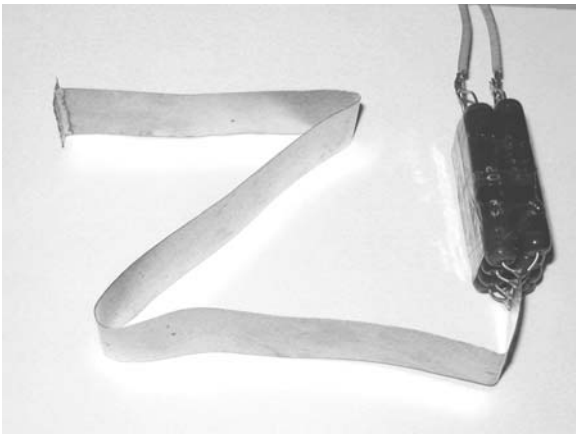


Figure 4.35 Setup showing the dc resistance measurement.

connecting to bypass capacitors is acceptable; as long as we use a voltmeter with high input resistance, the presence of capacitors will not alter the result.

4.5.3 Effect of Perforations on DC Plane Resistance

In PCBs and packages, the vertical signal connections require antipad holes around via barrels. The antipads reduce the amount of the conductive material and increase the plane resistance. With a uniform array of antipads, and as long as the remaining webbing is not very small (see Figure 4.36), we can approximate the sheet resistance by applying a correction factor:

$$R_s' = R_s \frac{total\ area}{total\ area - \sum cutout\ area} \tag{4.48}$$

With heavy perforations, where the remaining webbing is small, detailed meshing is necessary to take into account the current crowding at the narrow sections.

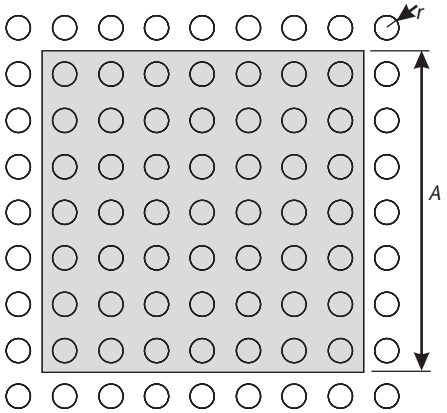


Figure 4.36 Illustration of plane perforations.

4.5.4 Simulating DC Voltage Drop and Effective Plane Resistance

Sheet resistance and resistance between concentric circles are useful concepts for understanding the dc drop on planes, but real-life connections seldom follow these simple geometries. With a complex geometry, the calculation of voltage drop requires detailed simulations. SPICE can also be used with a resistive grid. It is basically the same grid as discussed in Section 4.3.1, except we can omit the inductive part for the planes and all capacitive components. Also, the resistive grid can also take into account the effect of light perforations. Figures 4.37 and 4.38 show the voltage drop over a square shape of 35-μm (1-oz) copper plane, with 1-A dc current and two different connection schemes. We assume that the load connects at 25 nodes in the middle of the plane, whereas the source is connected to 7 nodes around the lower right corner. The simulation deck assumes a 1-A dc current total uniformly distributed among the 25 entry nodes at the center. The seven exit nodes at the lower right are all tied to SPICE node 0. The voltage surface exhibits a local peak where the 1-A current enters the plane. There is a large gradient of voltage in the lower right quadrant of the plane where the conductive plane is effectively utilized. The voltage gradient is low in the opposite direction at the upper left of the plane; this low gradient indicates that this portion of the plane, does not contribute effectively to carrying the current between the entry and exit points.

4.5.5 Characterization of Mid- and High-Frequency Plane Parameters

The procedure outlined below assumes rectangular planes, and a uniform and homogeneous cross section and materials. We also assume that the w_x and w_y dimensions of the planes (see Figure 4.1) are known: they can be obtained with sufficient accuracy either from the board CAD file or from mechanical measurements on the finished board. Also, as long as the dielectric material in all pairs is the same, the procedure below can be applied to multiple plane pairs connected in parallel by

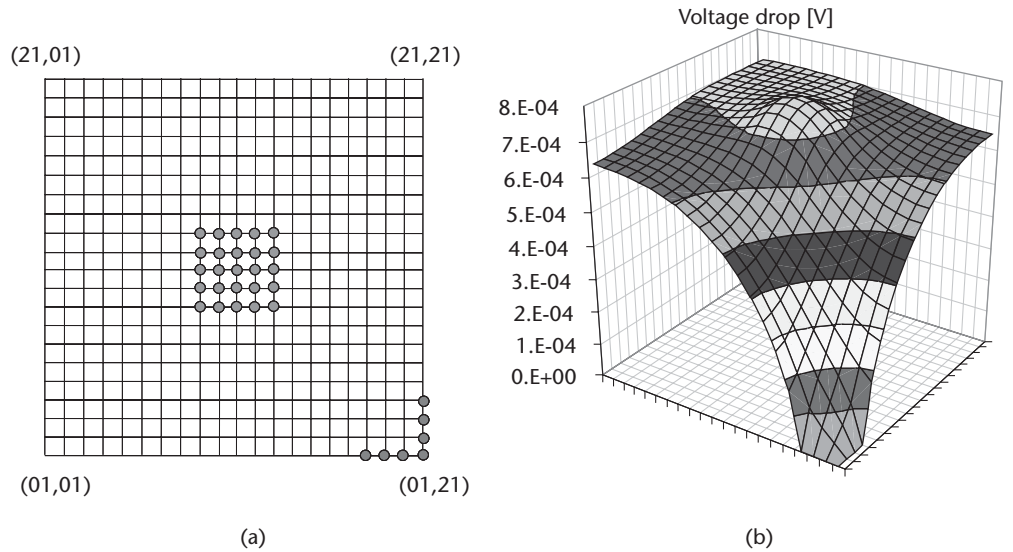


Figure 4.37 Voltage drop on 35-μm (1-oz) plane due to 1-A dc current: (a) shows the floor plan and connections and (b) shows the voltage drop surface.

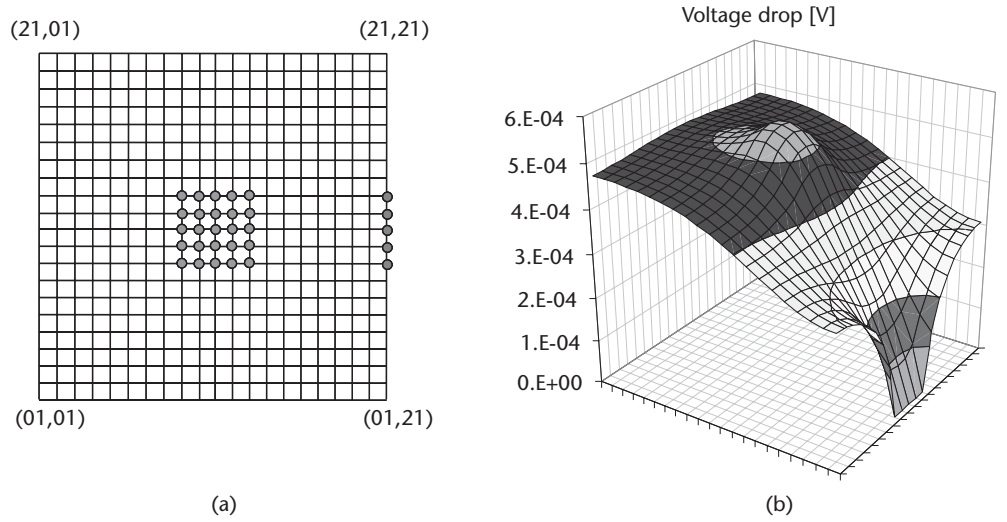


Figure 4.38 Voltage drop on 35-μm (1 oz) plane due to 1-A dc current: (a) shows the floor plan and connections and (b) shows the voltage drop surface.

many vias distributed evenly over the planes. In this case, the h separation will be the parallel equivalent of the individual laminate thickness values. For two parallel plane pairs with h_1 and h_2 plane separations, the equivalent plane separation is:

$$h = \frac{1}{\frac{1}{h_1} + \frac{1}{h_2}} \tag{4.49}$$

There are parameters, however, that on a finished board cannot be measured directly without destructive probing: the plane separation, thicknesses of planes, and surface roughness of planes. Furthermore, the electrical properties of the dielectrics and metals are not usually measurable on finished boards, due to cutouts and the stackup.

To obtain an estimate for the dielectric constant and the plane separation, we can use the formulas for the static capacitance and modal resonance frequencies, as illustrated in Figure 4.39. The measured static plate capacitance can be equated to its calculated value. This value has two unknowns: ε_r and h (since we assumed that the horizontal dimensions of the rectangular planes, w_x and w_y are known). The parallel-plate modal resonance frequencies are the integer multiples of where the half wavelength equals the w_x or w_y dimensions. The second formula in (4.50) takes the lowest resonance frequency along the w_x dimension.

$$C_p = \varepsilon_0 \varepsilon_r \frac{w_x w_y}{h} \tag{4.50a}$$

$$f_{res} = \frac{1}{2w_x \sqrt{\varepsilon_0 \varepsilon_r \mu_0}} \tag{4.50b}$$

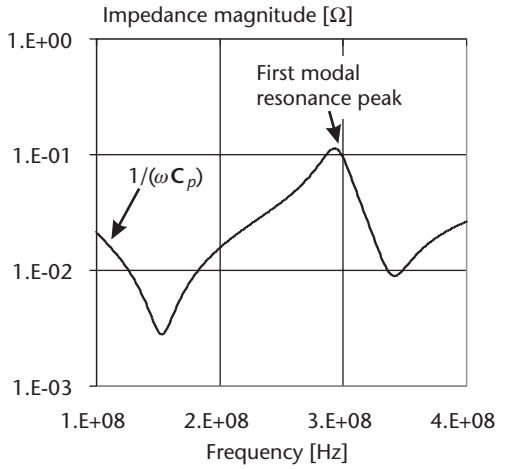


Figure 4.39 Impedance magnitude versus frequency plot, identifying the two parameters in (4.50).

In the formulas, ε_0 and μ_0, as well as w_x and w_y, are frequency-independent constants. Therefore, as long as ε_r is approximated as frequency independent, we can solve for ε_r and h. By rearranging (4.50), we get:

$$\varepsilon_r = \left(\frac{1}{4w_x^2 f_{res}^2 \varepsilon_0 \mu_0} \right), \quad h = \varepsilon_0 \varepsilon_r \frac{w_x w_y}{C_p} \tag{4.51}$$

If the capacitance is frequency independent, its value can be obtained from a low-frequency measurement point with (5.27). The frequency has to be high enough to ensure a reliable and low-noise measurement but low enough to ensure that the modal impedance minimum will not distort the result.

4.5.5.1 Determining the Modal Resonance Frequency of Lossy Dielectrics

If conductors and dielectrics were all ideally lossless, the first modal resonance frequency, f_{res}, could be obtained by probing the plane pair almost anywhere. However, with conductive and dielectric losses, the impedance profile and the frequencies of the modal resonance peaks do depend on the location over the planes. Furthermore, the peaks are not unique anymore: the frequency of the peak depends on how we define the peak itself. The peak implies maximum magnitude of impedance. Resonance, however, is usually understood to happen at frequencies where the imaginary part is zero; hence, the phase of impedance is zero. As shown in Figure 4.40, the values extracted according to these two definitions will be close, but not exactly the same. Figure 4.40 shows the extracted first modal resonance frequency from the simulated impedance profile of a lossy pair of FR4 planes with 35-μm (1-oz) copper on either side and with plane dimensions of w_x = 25.4 cm (10 inches), and w_y = 12.7 cm (5 inches). Note that the frequency extraction is not unique; the values depend on the location on the planes. If, instead of impedance magnitude peak or phase zero crossing, we define the resonance frequency where the phase derivative has its

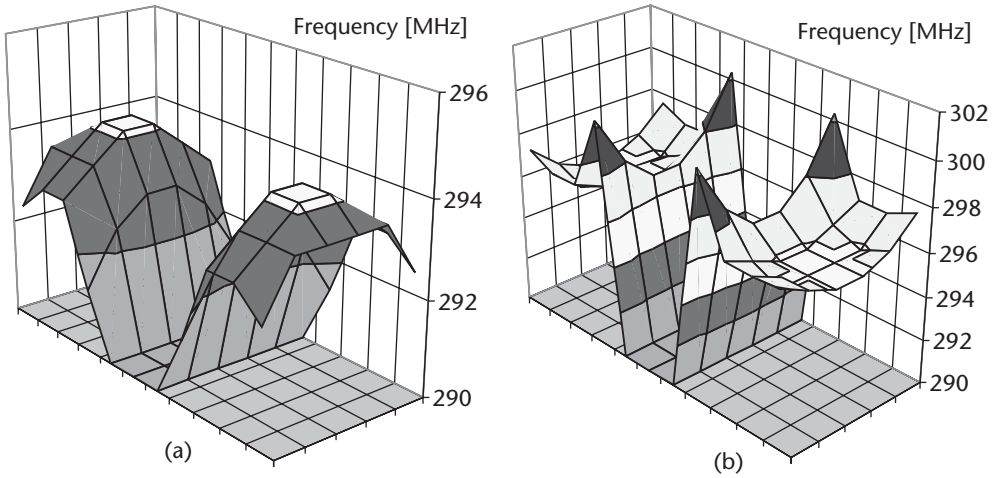


Figure 4.40 Extracted first modal resonance frequency from the simulated impedance of a lossy pair of planes with lossy dielectric. Part (a) shows the frequencies where the impedance magnitude is the highest. Part (b) shows the frequencies where the phase of impedance crosses 0. The gap in the middle reflects locations where the modal resonance is suppressed by the 2:1 aspect ratio. (The sharp slope in the middle is due to plotting artifacts.) The floors of the charts represent the surface of the planes.

extreme value, the extracted frequency becomes the same, regardless of the location on the planes.

Figure 4.41(a) shows the same pair of planes with the first derivative of phase plotted at one given location on the planes. Figure 4.41(b) shows the first modal resonance extracted from the extreme value of phase derivative (in case of first modal resonance: minimum) over the surface of the planes.

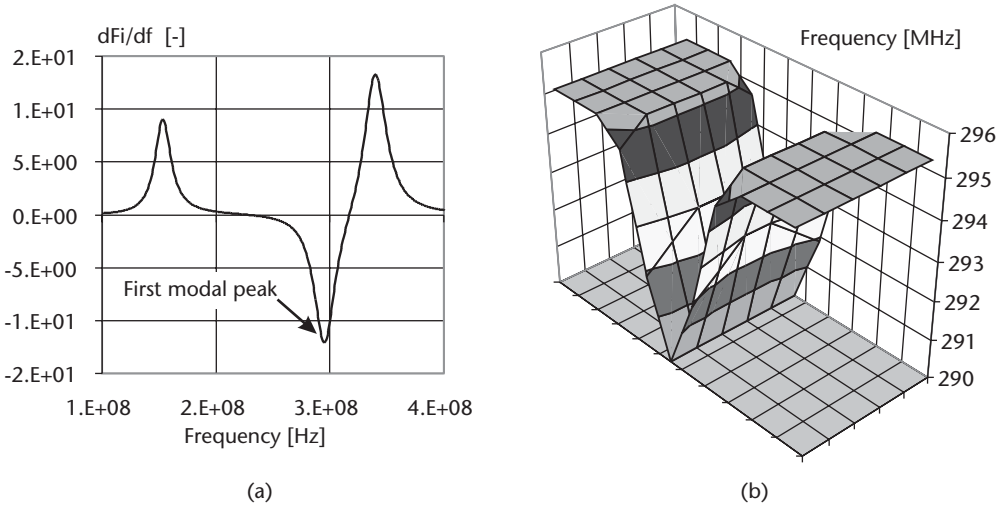


Figure 4.41 Extracted first modal resonance frequency from the simulated impedance of a lossy pair of planes with a lossy dielectric: (a) shows the first derivative of frequency at the corner of the planes and (b) shows frequencies where the first derivative of the phase has its extreme. The floor of the graph represents the surface of the planes.

As a summary, for plane pairs where the losses are not negligible (increasingly the case with thinner laminates), the first modal resonance frequency should be extracted from the extreme value of the phase derivative. Note, however, that phase itself is already more noisy in measurements than magnitude. The derivative of the phase becomes even noisier due to the high-pass nature of the derivative process. Therefore, measuring the plane parameters based on this procedure requires averaging and narrow measurement bandwidth to sufficiently suppress noise. Measured examples will be shown later in Section 4.5.5.5.

4.5.5.2 Dielectric Constant and Dielectric Loss

Now we can return to (4.50) and continue the parameter extraction using the static plane capacitance and the frequency of lowest modal resonance. The relative dielectric constant appears in both constraints, but with (5.28) we cannot extract the static plane capacitance at the first modal resonance frequency; there will be at least one, possibly two or more decades of frequency separation between the frequencies of the static plane capacitance and first modal resonance. We can uniquely solve for the two unknowns from (4.49) only if ε_r were frequency independent. If ε_r is not frequency independent, we have to know and model its frequency dependency. We have to obtain a scaling factor for ε_r to the frequency of first modal resonance before we solve for the two unknowns.

By measuring the complex impedance of the DUT, we could obtain the capacitance from the imaginary part and the loss tangent from the phase of the impedance. Unfortunately, with low-loss materials, the phase angle is very close to $-90°$; the finite accuracy of measuring instruments will not allow us to accurately measure the loss tangent. Knowing how the frequency-dependent capacitance and frequency dependent loss tangent relate to each other can help us in characterization. From the causality constraint of impedances, we know that the real and imaginary parts of the impedance are interrelated; their values and their frequency dependencies are linked to each other [23]. Dielectric constant and dielectric loss and inductance and resistive loss share tightly coupled frequency dependency [24]:

$$H(\omega) = \alpha(\omega) + j\beta(\omega) \tag{4.52}$$

$$\alpha(\omega) = \alpha(0) - \frac{\omega^2}{\pi}\int_{-\infty}^{\infty} \frac{\beta(u)}{u\left(u^2 - \omega^2\right)}\,du \tag{4.53}$$

$$\beta(\omega) = \frac{\omega}{\pi}\int_{-\infty}^{\infty} \frac{\alpha(u)}{u^2 - \omega^2}\,du \tag{4.54}$$

The dielectric constant and dielectric loss are expressed with the real and imaginary parts of the complex permittivity:

$$\varepsilon_r(\omega) = \varepsilon_r'(\omega) - j\varepsilon_r''(\omega) = \varepsilon_r'(\omega)\left(1 - j\tan\_\delta\right) \tag{4.55}$$

Equation (4.55) also defines the loss tangent, tan_δ. In its general form, (4.51) allows for a number of different frequency dependencies. The real and imaginary

parts of the complex permittivity show very complex frequency dependencies as frequency varies from a few Hertz up to light wave frequencies. At lower frequencies, dipolar and ionic relaxation are typical; at higher frequencies atomic and electronic resonances are typical. Relaxation losses typically exhibit a changing real part of permittivity in a relatively narrow frequency range accompanied by a peak in the imaginary part. Relaxations are usually modeled by the Debye relaxation model [25], named after the chemist Peter Debye. The relaxation model for a single contributor can be expressed as:

$$\varepsilon(\omega) = \varepsilon_{\infty} + \frac{\Delta\varepsilon}{1 + j\omega\tau} \tag{4.56}$$

where the first term is the high-frequency asymptotical permittivity, $\Delta\varepsilon$ is the permittivity change between low and high frequencies, and τ is the relaxation time of the material.

Multiple relaxation processes over a broader frequency range can be modeled by a sum of N first-order relaxation terms:

$$\varepsilon(\omega) = \sum_{i=1}^{N} \frac{a_i}{1 + j\omega\tau_i} \tag{4.57}$$

which is suitable to capture any frequency dependency.

Experimental data shows that for a large number of commonly used PCB materials the dielectric constant drops, whereas the dielectric loss tangent increases with the same percentage value over a logarithmic frequency scale. In other words, on a linear-logarithmic scale, both the dielectric constant and the loss tangent are straight lines. Reference [26] shows that the measured capacitance of FR-4 laminates is constant up to about 1 kHz and drops linearly on a logarithmic frequency scale from 1 kHz to 10 GHz. To maintain causality and at the same time to meet common-sense expectations, the responses should deviate from this linear shape at very low and very high frequencies. If the curves maintained their slope over all conceivable frequencies, it would result in infinite capacitance at dc and infinite loss tangent at infinite frequency.

To obtain a simpler formula to approximate the empirical data, (4.57) can be modified to replace the finite sum either with an integral [26] or infinite sum [27] so that the multipole Debye model yields a linear change on the logarithmic frequency scale between a user-selected ω_1 lower frequency and ω_2 upper frequency:

$$\sum_{i=1}^{N} \frac{\Delta\varepsilon_i'}{1 + j\dfrac{\omega}{\omega_i}} \to \frac{\Delta\varepsilon'}{m_2 - m_1} \int_{x=m_1}^{m_2} \frac{dx}{1 + j\dfrac{\omega}{10^x}} = \frac{\Delta\varepsilon'}{m_2 - m_1} \frac{\ln\dfrac{\omega_2 + j\omega}{\omega_1 + j\omega}}{\ln 10} \tag{4.58}$$

where $m_1 = \log_{10}(\omega_1)$ and $m_2 = \log_{10}(\omega_2)$.

The causal frequency dependence of the dielectric constant and loss tangent from (4.58) are illustrated in Figure 4.42.

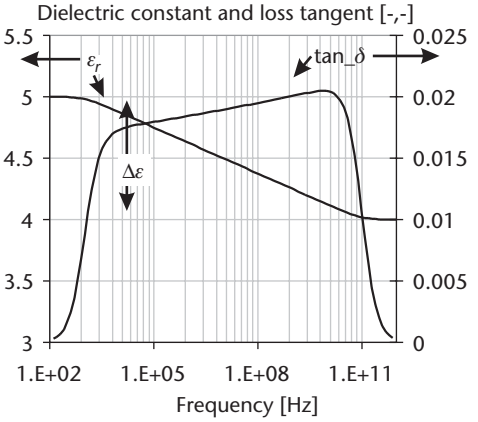


Figure 4.42 Simulated relative dielectric constant (ε_r) and dielectric loss tangent (tan_δ) following the modified Debye model of (4.58), with the following parameters: $m_1 = 3$, $m_2 = 11$, $\Delta\varepsilon = 1$, $\varepsilon_\infty = 4$.

Note that (even though we may want to maintain causality in our models) if we need only the frequency range where the data is a straight line on a linear-logarithmic scale, an even simpler approximation can be used. From a dielectric constant and slope at a working frequency, f_w, we can calculate the approximate lines for the dielectric constant and loss tangent. Note also that we turn to the causality constraint primarily to help in the measurement procedure; this constraint allows us to deduce the loss tangent from the change of capacitance versus frequency. As it was stated in Chapter 1, strictly speaking causality is less of a concern in PDN characterization, as we usually do not need the wave shape of the noise to be very accurate.

Though (4.58) provides a causal solution, we very rarely need laminate characterizations over such a wide frequency range that we would actually enter the frequency range below ω_1 and above ω_2. We can further simplify (4.58) by realizing that in the frequency range of interest the slopes of the ε' and tan_δ curves have the same magnitude but opposite signs: based on the above model, the capacitance always decreases with increasing frequency while the loss tangent always increases. By selecting an arbitrary working frequency of f_w somewhere conveniently within the range of linear slope (see Figure 4.43), the real part of permittivity and the loss tangent can be expressed by the value and first derivative of ε':

$$\tan\_\delta(f_w) = -\frac{m(\varepsilon_r)}{\varepsilon_r(f_w)}\frac{\pi/2}{\ln(10)} \tag{4.59}$$

where

$$m(\varepsilon_r) = \lim_{\Delta\to 0}\frac{\varepsilon_r(f_{w+\Delta}) - \varepsilon_r(f_{w-\Delta})}{\log_{10}\left(\frac{f_{w+\Delta}}{f_{w-\Delta}}\right)} \tag{4.60}$$

Equations (4.59) and (4.60) help us to characterize the laminates primarily by measuring the capacitance versus frequency curve in a frequency range where the data has the lowest noise, permitting a straightforward fit to the Debye model.

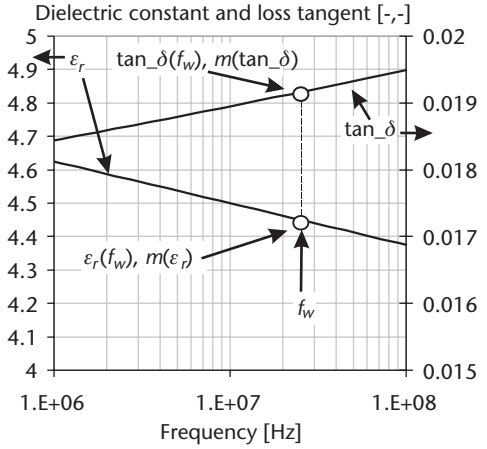


Figure 4.43 Illustration of (4.59) through (4.60) with the dataset of Figure 4.42 enlarged in the 1–100-MHz range.

4.5.5.3 AC Plane Resistance and Inductance

As dielectric constant and loss tangent are linked by the causality constraint, the same causality constraint also applies to the series branch of the transmission-line equivalent circuit: resistance and inductance. The resistance starts with the R_{dc} value at dc, then it gradually moves toward the resistance dictated by the high-frequency sheet resistance determined by the skin depth (4.8). Inductance is easier to follow from high frequencies going toward low frequencies. At very high frequencies, the current flows in thin layers on the facing surfaces of the planes; this results in the *external inductance*. In case of plane pairs, it is also called interplane inductance (in H/square):

$$L_\infty = \mu_0 \mu_r h \tag{4.61}$$

As frequency decreases, the current penetrates the planes more deeply; also as the skin depth increases, so does the inductance. The portion of inductance that comes from the current loop inside the planes is called *internal inductance*. The finite current penetration in the planes results in a complex surface impedance with frequency independent 45° of phase angle [27]. Using the definitions shown in Figure 4.1, the complex surface impedance is the sum of the surface impedances of the upper and lower planes:

$$Z_{surface}(\omega) = \frac{1-j}{\delta_u \sigma_u} \cot\left((1-j)\frac{t_u}{\delta_u}\right) + \frac{1-j}{\delta_l \sigma_l} \cot\left((1-j)\frac{t_l}{\delta_l}\right) \tag{4.62}$$

If the upper and lower planes are identical in thickness and conductivity, the two terms of (4.62) can be combined.

The series plane impedance can be expressed as the sum of the dc resistance, complex surface impedance, and the reactance of external interplane inductance:

$$Z_s(\omega) = R_{dc} + Z_{surface}(\omega) + j\omega L_\infty \tag{4.63}$$

The complex surface impedance of planes given by (4.63) assumes smooth plane surfaces. Realistic plane surfaces are never ideally smooth. As the skin depth becomes comparable to and smaller than the surface roughness with increasing frequency, the surface impedance will increase. There is a widely quoted empirical formula (originally from microwave trace measurements and simulations) describing the approximate rise of surface impedance. The scalar multiplier, K_{sr}, is:

$$K_{sr}(\omega) = 1 + \frac{2}{\pi}\arctan\left(1.4\left(\frac{\Delta}{\delta(\omega)}\right)^2\right) \tag{4.64}$$

where Δ is the rms surface roughness and $\delta(\omega)$ is the skin depth in the same, but arbitrary units.

With (4.64), (4.63) becomes:

$$Z_s(\omega) = R_{dc} + K_{sr}(\omega)Z_{surface}(\omega) + j\omega L_{\infty} \tag{4.65}$$

4.5.5.4 Resonator Quality Factor

One of the challenges in accurately characterizing plane pairs is that there are several interrelated unknowns. Unless we use trusted and proven models to fit the measured data, there is no direct way to measure the parameters one-by-one. As it was shown in Section 4.5.5.2, we can measure the static plane capacitance at frequencies much lower than the first modal resonance, but to obtain the plane separation from (4.51), we need the dielectric constant at the modal resonance frequency. We can measure the dc resistance of a plane; however, its high-frequency losses eventually depend not only on the plane thickness, but also on the conductivity and surface roughness. Another means of cross-correlating data is to measure the quality factor, Q, of the modal resonances and then equate it to the quality factor calculated from the assumed loss contributors. For microwave resonators, Q is expressed in terms of the quality factors resulting from conductive losses, Q_c, dielectric losses, Q_d, and radiation losses, Q_r [28]:

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_r} \tag{4.66}$$

The quality factors due to conductive and dielectric losses are directly related to the complex surface impedance and loss tangent, respectively:

$$Q_c = f\left(Z_{surface}\right) \tag{4.67}$$

$$Q_d = \frac{1}{\tan\_\delta} \tag{4.68}$$

For plane pairs, where the plane separation is much smaller than the w_x and w_y horizontal dimensions, the Q_r radiation loss can be neglected.

4.5.5.5 Measurement-Model Correlations

Dedicated methods and setups exist to measure and characterize conductive and dielectric materials for PCBs as accurately as possible. Many of these methods rely on the measurement of a combination of conductive and dielectric layers, such that the static capacitance and the resonance pattern of the cavity can be measured [29]. There are several measurement methods recommended by IPC; two widely used options are the stripline method [30] and the full-sheet resonance method [31]. A good practical overview of available options can be found in [32].

In simple and unsophisticated setups, our best means of achieving the highest accuracy is to eliminate unnecessary variables as much as possible. When we measure dielectric materials, the uncertainty due to conductor parameters can be greatly reduced by preparing a dielectric sample and adding the necessary conductive layers as parts of the measurement fixture as electrodes. In this way the electrodes can be prepared and characterized more accurately and carefully. Similarly, when measuring the parameters of conductive layers, eliminating the insulating material helps to reduce uncertainties. While these characterizations are possible, they do not represent the final construction of the PCB. In a real PCB, the building block is a plane-dielectric-plane sandwich, as shown in Figure 4.1. This comes from a core or is the result of a prepreg facing the planes on the cores above and below or is the result of a layer-by-layer buildup process.

To characterize a basic two-sided laminate, we can start with a rectangular shape either as a stand-alone three-layer structure or as part of a finished PCB or package. By measuring the dc resistance and the impedance profiles with open boundaries and with shorts, we can fit the model of our choice to the measured data. The geometric parameters can be measured either by simple visual inspection or after cross-sectioning to yield the dielectric and plane thicknesses, as well as surface-roughness numbers.

As we show in the first characterization and correlation example, in a limited frequency range, sufficient correlation can be achieved, even with mostly frequency-independent models. Figure 4.44 shows the photo of a 20-layer test board with w_x = 25.4-cm (10-inch) and w_y = 12.7-cm (5-inch) dimensions. The test board had five plane pairs with 50-μm (2-mil) laminate separation (see Figure 4.45), arranged into two groups: the upper two thin laminate pairs are connected by the test vias; the bottom three laminate pairs were unconnected. The first plane pair was 75 μm (3

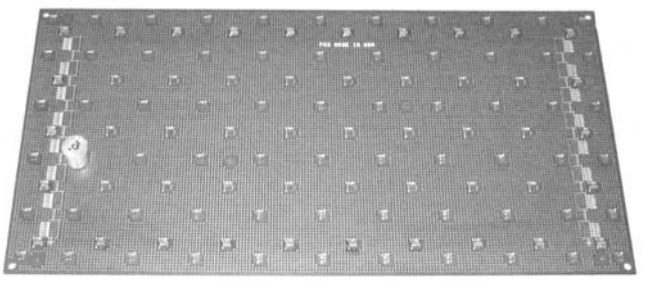


Figure 4.44 Rectangular multilayer test board for laminate and capacitor characterizations. The board size is w_x = 25.4 cm (10 inches) and w_y = 12.7 cm (5 inches). The board is shown with one bulk capacitor attached.

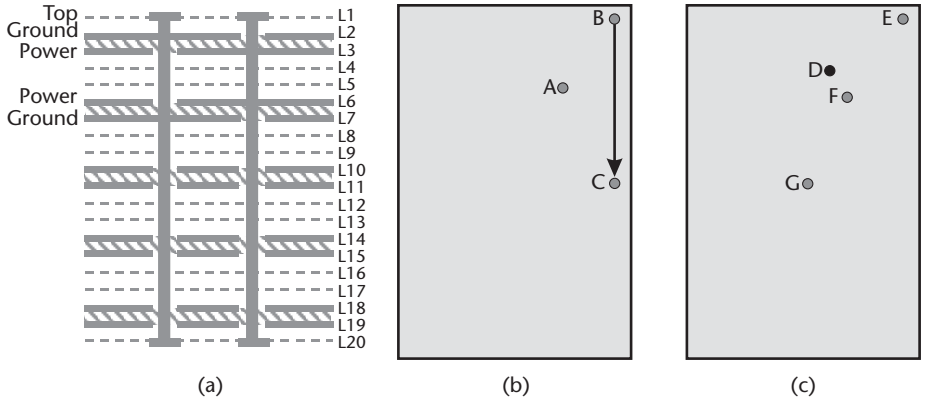


Figure 4.45 (a) Stackup and connections in the test board of Figure 4.44. (b) Connection points for the bare-board correlations shown in Figure 4.46. (c) Connection points for the shorted correlations shown in Figure 4.47.

mils) below the surface. There were two sets of vias, both on a 2.54-cm (1-inch) grid, with a 1.27-cm (0.5-inch) offset with respect to each other. One set of vias were through holes for probing purposes, connecting to the planes on layers 2 and 3. The second grid of vias was groups of blind vias connecting the same planes to surface pads for eight-terminal capacitors.

The board was measured at various test points with nothing attached to it (bare), as well as with shorts attached in different combinations to the capacitor sites. First, the dielectric constant and plane separations were calculated from the average of static capacitances and first modal resonances measured at three different locations. Based on (4.51) this resulted in $h_1 = h_2 = 52.3\,\mu$m (2.06 mils) and $\varepsilon_r = 4.22$. A uniform SPICE grid with a 6.35-mm (0.25-inch) cell size was created to simulate the planes where the dielectric constant, loss tangent, and plane inductance were assumed to be frequency independent. Second, the resistance and inductance of the individual shorts (vias, pads, and shorting bar) were obtained by fitting the unknown parameters to measured data. It was found that 0.5-mΩ dc resistance, $1.6\text{E}^{-7}\,\Omega/\sqrt{f}$ skin resistance and 47-pH inductance gave good agreement for all measured locations. The attached impedance of the shorted structure thus was (in ohms):

$$Z_{attached} = 5\text{E}^{-4} + 1.6\text{E}^{-7} * \sqrt{f} + j2\pi f * 47\text{E}^{-12} \tag{4.69}$$

Finally, the measured and simulated impedance profiles were compared for various self- and transfer-impedance combinations for the bare and shorted cases. Figures 4.46 and 4.47 show the degree of correlation for the bare and shorted cases, respectively.

The process outlined above is convenient to obtain the approximate laminate characteristics in real-life stackups and board constructions. The test via pairs dispersed evenly over the board provide a convenient way to measure the laminate characteristics at various locations. However, the test-via pairs require small cutouts (i.e., antipads) around via barrels. These cutouts change the plane parameters: by reducing the static capacitance and slightly distorting the resonance pattern.

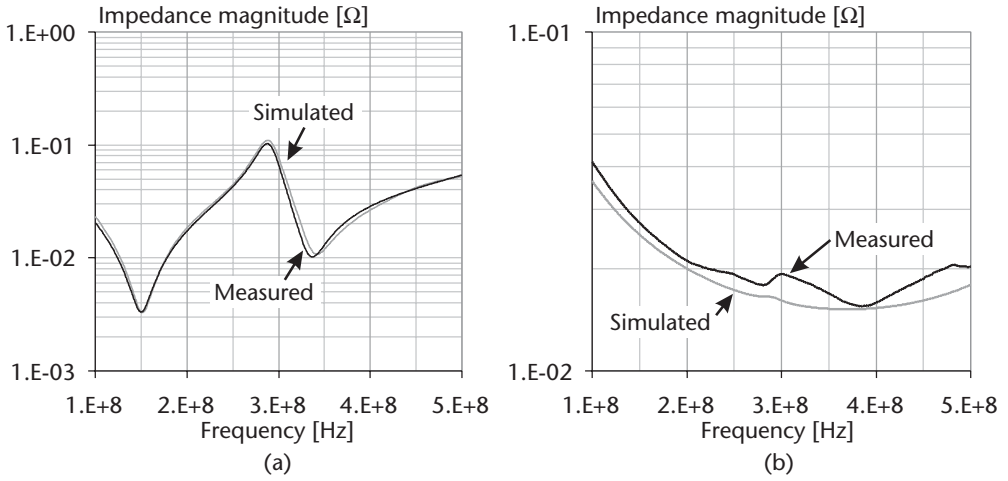


Figure 4.46 Simulated and measured impedance magnitudes at two different locations on the test board. (a) Self-impedance at location A. (b) Transfer impedance between B and C.

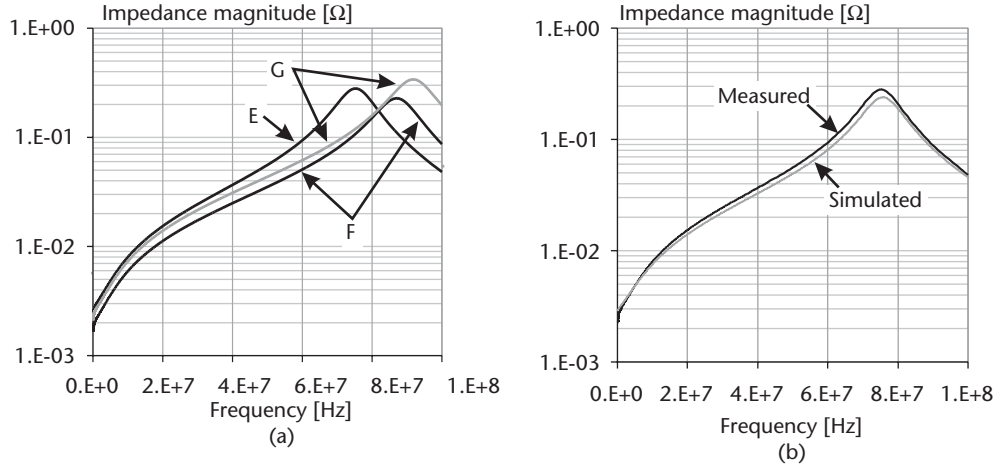


Figure 4.47 (a) Measured self-impedance plots at various locations of *shorts* as identified on Figure 4.45(c). Measurement point is D for all three traces. (b) Correlation between measurement and simulation for trace E.

The same test-board construction was used to compare various laminates, as reported in [33]. Figures 4.48 and 4.49 show the frequency-dependent capacitance and inductance of various laminates, all of which were tested in the same nominal board construction. Table 4.1 summarizes the major parameters of the laminates and decodes the labels. The dielectric thickness and copper thickness values are nominal; they were not checked by cross-sectioning. The column of relative dielectric constant, ε_r, shows the measured values on the test boards at 1 MHz. The dielectric loss, tan_δ column gives the measured value calculated from the rate of capacitance change with (4.59) and (4.60).

The data in Figure 4.48 is normalized to the low-frequency capacitance value of each board, and thus the impact of dielectric thickness and dielectric constant differ-

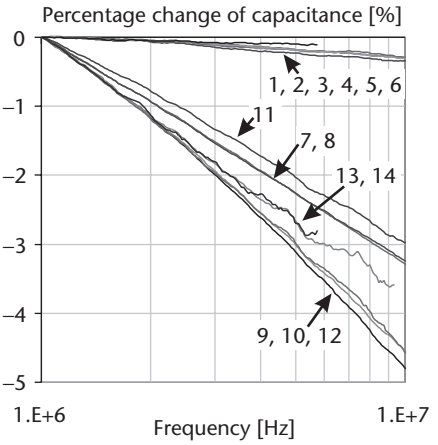


Figure 4.48 Percentage change of capacitance of boards with laminates from Table 4.1, measured in bare boards of construction, as shown in Figures 4.44 and 4.45.

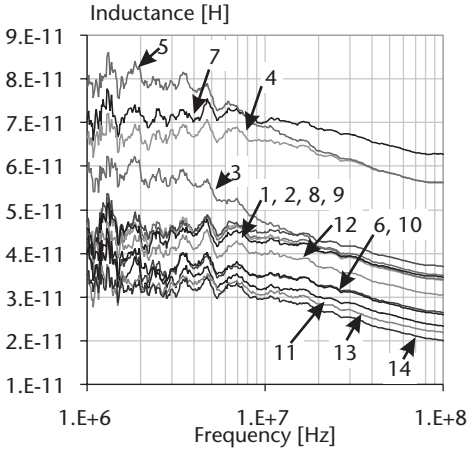


Figure 4.49 Inductance of boards with laminates from Table 4.1, measured in shorted boards of construction, as shown in Figures 4.44 and 4.45.

ences is removed. All six unfilled polyimide laminates (1–6) exhibit approximately, –0.3%/decade capacitance drop. The two glass-reinforced laminates (7 and 8) show –3.2%/decade capacitance change. The highest rate of capacitance drop comes from laminates 9, 10, and 12.

The inductance values in Figure 4.49 were measured on the same test boards when all capacitor sites around the board periphery were shorted. There are three major phenomena we can observe on the inductance data. The first obvious trend is that the high-frequency inductance is proportional to the nominal dielectric thickness. The second trend is that the saturated inductance at low frequencies is proportional to the average thickness of the dielectric *and* copper. The third trend is the drop of inductance with increasing frequency as the current penetration inside the planes is reduced by the skin effect.

Table 4.1 Summary of Parameters of Laminates Shown in Figures 4.48 and 4.49

	Dielectric Thickness [mm]	*ε_r at 1 MHz [-]*	*tan_δ at 1 MHz [-]*	*Dielectric Type*	*Copper Thickness [mm]*	*Copper Type*	*Reference*
1	25	3.15	0.002	unreinforced, unfilled	36	ED	HK042536E
2	25	3.17	0.0024	unreinforced, unfilled	36	RA	HK042536R
3	25	3.13	0.0019	unreinforced, unfilled	72	RA	HK042572R
4	50	3.14	0.0021	unreinforced, unfilled	36	RA	HK045036R
5	50	3.15	0.0021	unreinforced, unfilled	72	RA	HK045072R
6	50	14.7	0.0032	unreinforced, filled	36	RA	HK1014
7	50	3.4	0.022	reinforced, unfilled	36	ED	ZBC2000
8	25	3.7	0.022	reinforced, unfilled	36	ED	ZBC1000
9	24	4.4	0.033	unreinforced, unfilled	36	RA	BC24
10	16	4.0	0.031	unreinforced, unfilled	36	RA	BC16
11	12	3.8	0.02	unreinforced, unfilled	36	RA	BC12
12	24	16.8	0.031	unreinforced, filled	36	ED	C-Ply24
13	12	14.2	0.024	unreinforced, filled	36	ED	C-Ply12
14	8	13.1	0.023	unreinforced, filled	36	ED	C-Ply8

The second characterization example uses the same structure that was shown in Chapter 2, Figure 2.1. The sample piece of a nominal size of $w_x = 5.08$ cm (2 inches) and $w_y = 2.54$ cm (1 inch) was manually cut out from a multilayer board; this cut is similar to the one shown in the previous example, except for the fact that the outermost plane pair was connected to the test-via pair. The laminate thickness was nominally 50 μm (2 mils). The cut was made in such a way that the test vias were located in the middle; this was the only point on the planes where self-impedance was measured. The measuring instrument was an Agilent N5230, with a logarithmic sweep in the 1-MHz–10-GHz frequency range. We use this example to show in more detail how to extract the frequency-dependent ε_r and tan_δ. Figure 4.50 shows the measured self-impedance magnitude and phase. The same data is shown on both charts: (a) shows the full-span impedance and (b) shows the zoomed impedance profile around the first modal resonance.

The size of the sample was remeasured more accurately; it was found that the longer dimension was $w_x = 5.22$ cm (2.05 inches). From the impedance data shown in Figure 4.50(b), the first modal resonance frequency was extracted as $f_{res} = 2.9768$ GHz. From this resonance frequency, (4.50b) yields a relative dielectric constant of 3.7254. To get the plane separation from (4.50a) and to allow for frequency-dependent parameters, we need the measured capacitance and the extracted dielectric constant at the same frequency. To do this, we extract the capacitance versus frequency curve at frequencies below the first impedance minimum, fit a causal multipole Debye model on the extracted capacitance, and then, from the model, we extrapolate the dielectric constant at f_{res}. The extracted capacitance versus frequency and the dielectric constant, as well as the loss tangent from the Debye model, are shown in Figure 4.51.

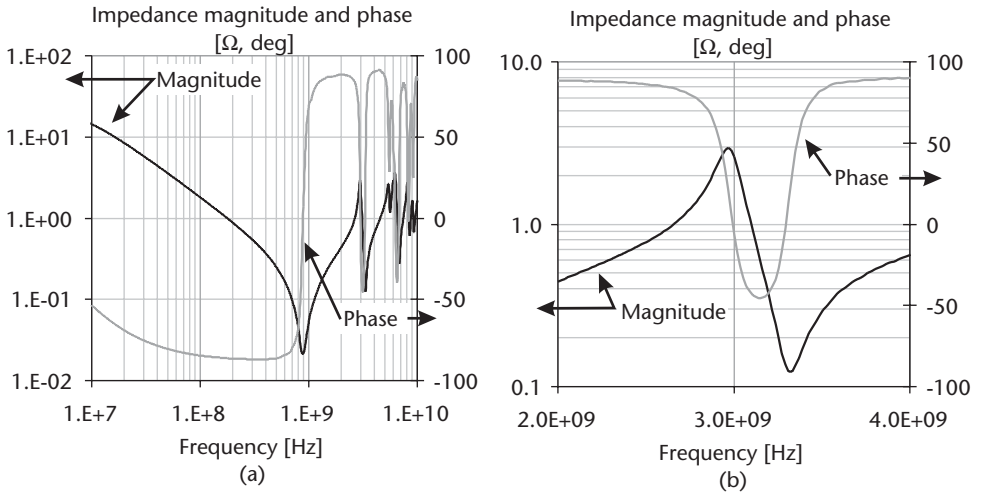


Figure 4.50 Self-impedance (a) magnitude and (b) phase of the 50-μm laminate sample.

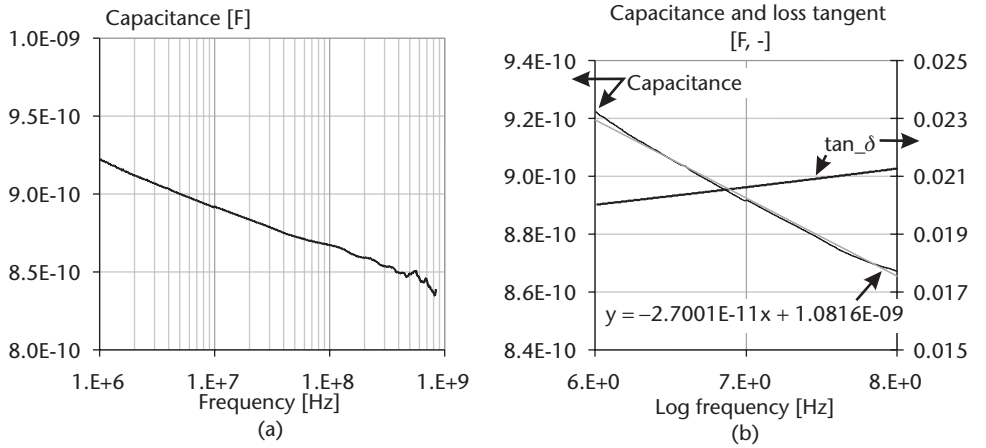
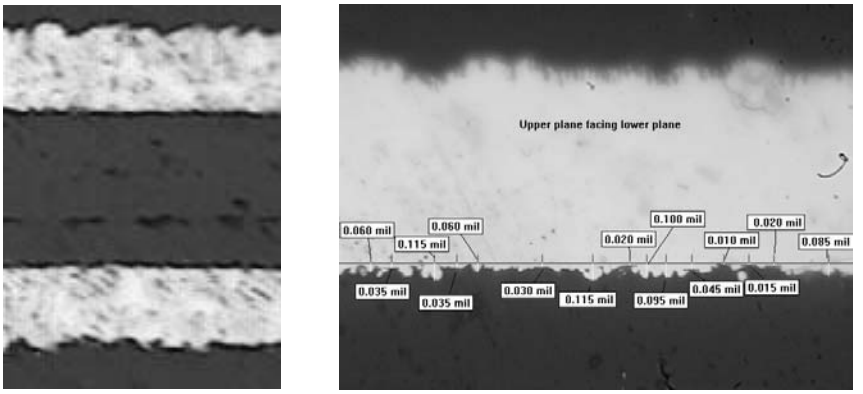


Figure 4.51 (a) Capacitance versus frequency and (b) capacitance and loss tangent from the Debye model for the 50-μm laminate.

The capacitance versus frequency plot on Figure 4.51(a) uses (5.28) and accounts for the plane inductance. Figure 4.51(b) shows both the measured capacitance and the straight line best-fit approximation of the Debye model. With the straight-line approximation of capacitance on the logarithmic frequency scale, we can extrapolate the capacitance out to f_{res}: the result is $C(f_{res}) = 825.8$ pF. Using the above $C(f_{res})$ estimate, (4.50a) yields $h = 59.8$ μm (2.35 mils) for the laminate thickness. Finally, the sample was cross sectioned, and the laminate thickness, upper and lower plane thicknesses and surface-roughness values were extracted, as illustrated in Figure 4.52.

The correlation between the measurement and simulation results was shown in Chapter 2.

The third and final characterization example uses a bare sheet of two-sided composite laminate, a DuPont Pyralux LF911R, which was probed at the edges with



(a) (b)

Figure 4.52 Cross-section (a) and surface-roughness measurement (b) on the 50-μm laminate. Cross-section and photo courtesy of Sanmina-SCI.

250-μm wafer probes. The nominal dimensions and probe connections are shown in Figure 4.53.

Measurements were carried out with two separate VNAs. The 100-kHz–1,800-MHz range was measured with a logarithmic sweep with an Agilent 4396A VNA with the 85046 *S*-parameter test kit. The 1–10-GHz frequency range was measured with linear sweep with an Agilent N5230 VNA. For both VNAs, calibration was done to the tips of the probes with a GGB Industries CS-14 calibration substrate.

The square sample was measured in three configurations: self-impedance at the corner (A), self-impedance in the middle of a side (B), and transfer impedance between the corner and middle of a side (see Figure 4.53). Figures 4.54 and 4.55 plot the measured self- and transfer impedances. Note that in the frequency range of 1.0–1.8 GHz there are two measured traces originated from two different instruments. The independent datasets run on top of each other; this indicates that the data is of good quality.

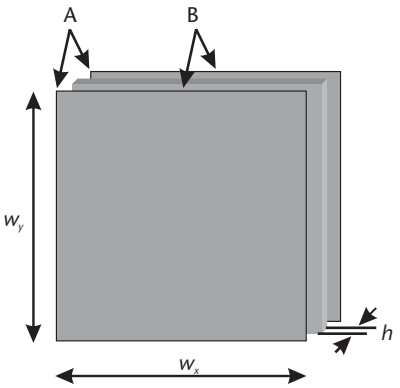


Figure 4.53 Bare laminate characterization. The sample size was $w_x = w_y = 6.35$ cm (2.5 inches) with a nominal dielectric thickness of $h = 75$ μm (3 mils).

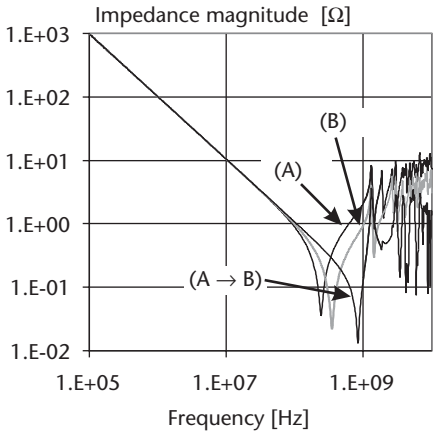


Figure 4.54 Self- and transfer impedance magnitudes measured on the sample shown in Figure 4.53.

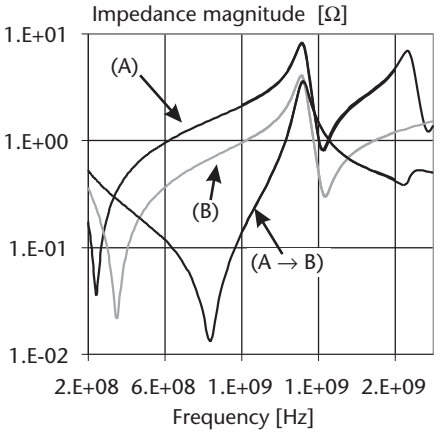


Figure 4.55 Self- and transfer impedance magnitudes measured on the sample shown in Figure 4.53. Zoomed horizontal scale.

The capacitance versus frequency curves were extracted from the measured impedance for all three cases. The capacitance measured at (B) is shown on Figure 4.56(a). Capacitance is shown as a function of the logarithm of frequency. The linear best-fit approximation over the highlighted 300 kHz–15 MHz is also shown on the chart. Figure 4.56(b) shows the dielectric constant and loss tangent independently extracted from the three datasets. The relative dielectric constant curves run on top of each other. The loss tangent curves are also close, but have a slight separation.

The first modal resonance frequency is f_{res} = 1.3144 GHz, the calculated laminate thickness is h = 78.8 μm (3.1 mils). The quality factor at the first modal resonance at location (B) is Q = 26.8. The calculated Q from the loss tangent and surface impedance is Q = 21.5.

The cross section of the laminate is shown in Figure 4.57. Figure 4.57(a) shows the entire two-sided laminate: the light strips on the top and bottom are the rolled anneal copper foils; the dark strip in the middle is the dielectric layer. By graphical postprocessing the photo can be enhanced to show the three layers of dielectrics: the

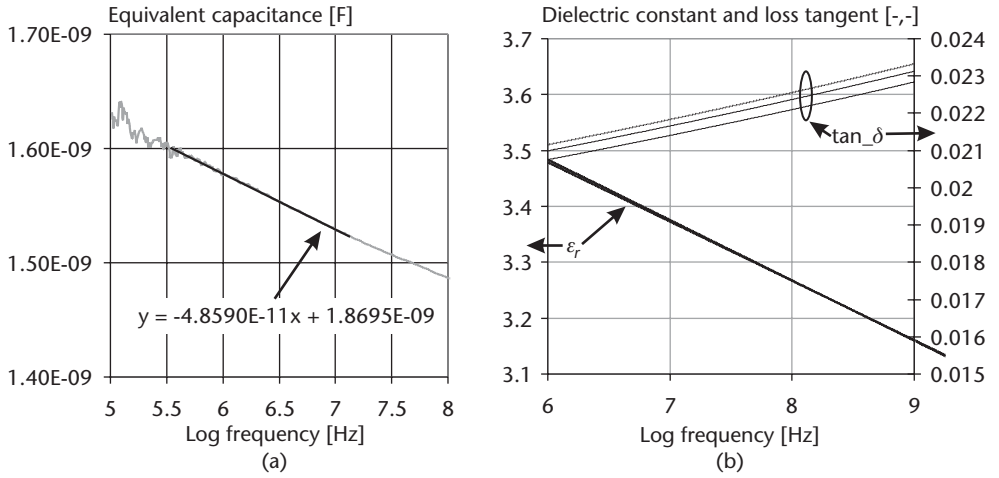


Figure 4.56 (a) Extracted and modeled capacitance from data at location (B). (b) Multipole Debye dielectric constant and loss tangent models from all three measured locations. Horizontal scale is the logarithm of frequency. There is no difference among the three dielectric constant (ε_r) curves; the top loss tangent (tan_δ) curve is from location (B); the middle trace is extracted from the transfer impedance; the bottom trace was extracted from data measured at location (A).

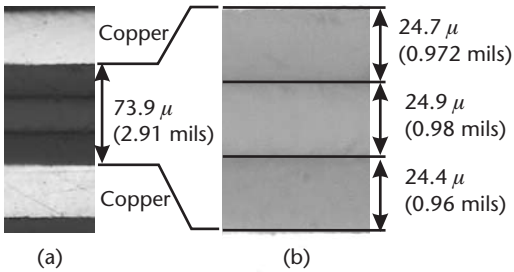


Figure 4.57 (a, b) Cross-section of the 75-μm laminate. (Laminate is courtesy of DuPont, cross section photo courtesy of Sanmina-SCI.)

polyimide layer in the middle and the two C-staged modified acrylic layers above and below. This is shown in Figure 4.57(b). The measured dielectric thickness is 73.9 μm, and from (4.50a) we get 77.2 μm, which agree within less than 5%. The surface roughness was measured at four different locations on the inner surfaces of the upper and lower planes; the root-mean-square surface roughness varied between 0.56 μm and 1.19 μm. Reference [34] is useful for analyzing multilayer structures.

Note that measuring the laminate parameters as shown above yields the average electrical properties of the three stacked dielectric layers.

To close the correlation loop, full-wave field-solver simulations were performed with the plane separation and dielectric parameters extracted from the measured impedance data. The frequency-dependent dielectric constant and loss tangent were entered into the tool. A surface impedance approximation was used to capture the frequency dependence of the inductance and resistance. The probes were modeled

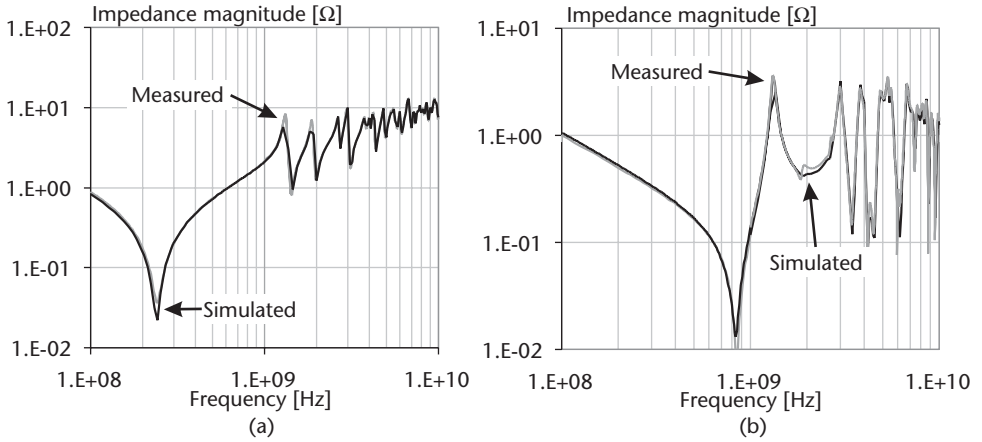


Figure 4.58 (a) Correlation between measured and simulated impedance magnitude at location (A) and (b) transfer impedance between locations (A) and (B).

with $75 \times 75\,\mu$m lumped ports, and the self-impedance at location (A) and the transfer impedance between locations (A) and (B) were simulated in the 0.1–10-GHz frequency range. The correlation is shown in Figure 4.58.

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