

# Table of Contents

About the Executive Editor .....	iii
About the Publisher.....	iv
Acronym Guide.....	???

<b>Preface</b> .....	vii
<b>Acknowledgements</b> .....	xix

## Part I

Chapter 1: Power Supply Compensation for Capacitive Loads .....	3
<i>Jonathan L. Fasig, Principal Engineer, Mayo Clinic</i>	
<i>Barry K. Gilbert, Director, Mayo Clinic</i>	
<i>Erik S. Daniel, Deputy Director, Mayo Clinic</i>	
1.1: Introduction .....	3
1.2: System Overview .....	4
1.3: Power Supply Stability Primer .....	5
1.4: Analysis .....	9
1.5: Conclusion.....	12
Chapter 2: DC–DC Converters: What is Wrong with Them? .....	15
<i>István Novák, Senior Signal Integrity Staff Engineer, SUN Microsystems</i>	
2.1: Introduction .....	15
2.2: DC-DC Converter Parameters Related to.....	18
Signal Integrity	
2.3: Potential SI Problems from the User’s Perspective.....	22
2.4: Conclusion.....	32
Chapter 3: The Advantage of Controlled ESR Polymer .....	35
Capacitors	
<i>Hideki Ishida, Design and Application Section Manager, Sanyo Electric Co.</i>	
3.1: Introduction .....	35
3.2: Controlling ESR Value of Tantalum Polymer Capacitor...	35
3.3: Importance of Controlled ESR Value Capacitor .....	37

3.4: Tantalum Polymer Capacitor with DC/DC Capacitor .....	42
Switching in the MHz Range	
3.5: Equivalent Circuit of Polymer Tantalum Capacitor .....	46
Chapter 4: ESR–Controlled MLCCs and Decoupling .....	49
Capacitor Network Design	
<i>Masaaki Togashi, Senior Development Engineer, TDK Corp.</i>	
<i>Chris Burket, Senior Applications Engineer, TDK Corp.</i>	
4.1: Introduction .....	49
4.2: Decoupling Capacitor Network .....	51
4.3: ESR and ESL .....	54
4.4: ESR Control Method .....	55
4.5: ESR/ESL Measurement of MLCCs .....	56
4.6: Measurement Results .....	60
4.7: Lower ESL Development .....	64
4.8: Conclusion .....	64

## Part II

Chapter 5: A Power Distribution System .....	69
<i>K. Barry, Principal Engineer, Hewlett Packard</i>	
<i>A. Williams, Principal Engineer, Hewlett Packard</i>	
5.1: Introduction .....	69
5.2: An Example of a Power Distribution Design System .....	69
5.3: The Problem Schematic .....	69
5.4: The Characterization of the Load .....	71
5.5: System Bandwidth .....	72
5.6: Determination of the Maximum Impedance .....	74
5.7: The Q of the System .....	74
5.8: Capacitance and Inductance Determination .....	75
5.9: Resonant Frequency Points .....	82
5.10: Number of Capacitors .....	84
5.11: Summary of Compiled Results .....	85
5.12: Summary of the Capacitor Selections and Graphical .....	84
Selections	
5.13: Graphics Result with Added Resistance .....	88
5.14: Sensitivity .....	90
5.15: Summary of the Design .....	92

Chapter 6: Designing Minimum Cost VRM8.2/8.3	123
Compliant Converters	
<i>Richard Redl, President, ELFI S.A.</i>	
<i>Brian Erisman, Project Engineer, Analog Devices, Inc.</i>	
6.1: Introduction	97
6.2: Objective Specifications	98
6.3: Load Transient Performance Limits of the Buck Converter	99
6.4: Optimal Load Transient Response	102
6.5: Commonly Used Control Techniques	104
6.6: Design for Optimal Output Impedance	107
6.7: Computer Simulations and Experimental Results	111
6.8: Summary	115
Chapter 7: Frequency Domain Target Impedance Method for Bypass Capacitor Selection for Power Distribution Systems	119
<i>Larry D. Smith, Principal Signal Integrity Engineer, Altema Corp.</i>	
7.1: Introduction	119
7.2: Target Impedance	120
7.3: Impedance in the Frequency Domain	122
7.4: PCB Bypass Capacitor	124
7.5: Capacitor Sizing from Target Impedance and Corner Frequency	127
7.6: ESR Considerations	130
7.7: Problems at High and Low Frequency	133
7.8: Comparing FDTIM to Other Methods	134
7.9: Conclusion	135
Chapter 8: Resonant Free Power Network Design Using Extended Adaptive Voltage Positioning Methodology	137
<i>Alex Waizman, Principal Engineer, Intel Corp.</i>	
<i>Chee-Yee Chung, Principal Engineer, Intel Corp.</i>	
8.1: Introduction	137
8.2: Lumped Power Delivery Model	138
8.3: Adaptive Voltage Positioning	139
8.4: EAVP	147
8.5: Time Domain Results	155
8.6: Future Work	159
8.7: Summary	159

Chapter 9: Distributed Matched Bypassing for Board-Level.....	163
Power Distribution Networks	
<i>Istvan Novak, Senior Staff Engineer, SUN Microsystems</i>	
<i>Leesa Nonjeim, Staff Engineer, SUN Microsystems</i>	
<i>Valérie St. Cyr, Supply Base Development Manager, SUN Microsystems</i>	
<i>Nick Biunno, Principal Engineer, Sanmina-SCI</i>	
<i>Atul Patel, Process Engineer, Sanmina-SCI</i>	
<i>George Korony, Senior Member of Technical Staff, AVX Corp.</i>	
<i>Andy Ritter, Senior Member of Technical Staff, AVX Corp.</i>	
9.1: Introduction .....	163
9.2: Distributed Matched Bypassing of Power.....	164
Distribution Networks	
9.3: Implementation of Distributed Matched Bypassing.....	180
9.4: The Concept of Bypass Resistor.....	192
9.5: Conclusion.....	194

### Part III

Chapter 10: Comparison of Power Distribution Network .....	201
Design Methods – An Approach to System-Level Power	
Distribution Analysis	
<i>Dale Becker, Senior Technical Staff Member, IBM Corp.</i>	
10.1: Introduction .....	221
10.2: The Process of IP Selection.....	203
10.3: Power Distribution Noise Analysis .....	204
10.4: Summary .....	211
Chapter 11: Bypass Filter Design Considerations for Modern.....	213
Digital Systems, a Comparative Evaluation of the Big “V,”	
Multipole, and Many Pole Bypass Strategies	
<i>Steve Weir, Consultant, Teraspeed Consultant Group</i>	
11.1: Introduction .....	213
11.2: What Does the Bypass Network Do?.....	213
11.3: Multilayer Chip Capacitor s Bypass Basics.....	215
11.4: Bypass Strategies – Three Methods, Three Faiths? .....	221
11.5: Summary .....	241
11.6: Conclusion.....	243
11.7: Points of View.....	254
11.8: Conclusion.....	255

Chapter 12: Comparison of Power Distribution Network .....	245
Design Methods: Bypass Capacitor Selection Based on Time Domain and Frequency Domain Preferences	
<i>Istvan Novak, Senior Signal Integrity Staff Engineer, SUN Microsystems</i>	
12.1: Introduction .....	245
12.2: So, What Is the Metric? .....	250
12.3: Comparison of Popular Methods Based on.....	251
Lumped Self-Impedance	
12.4: Component Placement.....	264
12.5: Implementation Examples.....	267
12.6: Conclusion.....	272
 Chapter 13: PDN Design Strategies: .....	275
Ceramic SMT Decoupling Capacitors – What Values Should I Choose?	
<i>James L. Knighten, Senior Staff Engineer, NCR Corp.</i>	
<i>Bruce Archambeault, Distinguished Engineer, IBM</i>	
<i>Jun Fan, Senior Hardware Engineer, NCR Corp.</i>	
<i>Giuseppe Selli, Ph.D. Candidate, University of Missouri-Rolla</i>	
<i>Samuel Connor, Senior Engineer, IBM</i>	
<i>James L. Drewniak, Professor, University of Missouri-Rolla</i>	
13.1: Introduction .....	275
13.2: The Power Bus Function .....	277
13.3: The Decoupling Capacitor.....	279
13.4: Interconnect Inductance .....	281
13.5: Conclusion.....	290

## Part IV

Chapter 14: Power Integrity Analysis of DDR2 Memory.....	297
Systems during Simultaneous Switching Events	
<i>Ralf Schmitt, Signal Integrity Engineers, Rambus, Inc.</i>	
<i>Joong-Ho Kim</i>	
<i>Chuck Yuan</i>	
<i>June Feng</i>	
<i>Woopoung Kim</i>	
<i>Dan Oh</i>	
14.1: Introduction .....	297
14.2: Supply Noise Modeling Methodology for.....	299
Interface Systems	

14.3: SSN Model for DDR2 Test System .....	307
14.4: Determining Worst-Case Switching Profiles .....	309
14.5: Correlating Supply Noise Parameters .....	313
14.6: Measuring Supply Noise on Internal Supply Voltage.....	317
14.7: Summary .....	320
 Chapter 15: Analysis of Supply Noise Induced Jitter in .....	323
Gigabit I/O Interfaces	
<i>Ralf Schmitt, Signal Integrity Engineers, Rambus, Inc.</i>	
<i>Hai Lan</i>	
<i>Chris Madden</i>	
<i>Chuck Yuan</i>	
15.1: Abstract.....	323
15.2: Introduction .....	323
15.3: Overview of Gigabit I/O Interface Test System .....	328
15.4: Measurement of Supply Noise Induced Jitter in a.....	337
Gigabit I/O Interface	
15.5: Summary .....	349
 Chapter 16: PCB Design Methods for Optimum FPGA .....	353
SerDes Jitter Performance	
<i>Steve Weir, Consultant, Teraspeed Consulting Group</i>	
<i>Steve McMorrow, President, Teraspeed Consulting Group</i>	
<i>Al Neves, Consultant, Teraspeed Consulting Group</i>	
<i>Tom Dagostino, Vice President, Teraspeed Consulting Group</i>	
<i>Brian Vicich, Signal Integrity Engineer, Samtec, Inc.</i>	
16.1: Abstract.....	353
16.2: FPGA SerDes Design Challenge.....	353
16.3: Virtex 4™ Rocket I/O Transmitter.....	354
16.4: MGT PDN PCB Reference Model.....	356
16.5: Linear Regulator Ripple Regulator .....	356
16.6: Jitter Evaluation Test Vehicle.....	363
16.7: Jitter Evaluation Tests.....	366
16.8: Summary .....	370
16.9: Conclusion.....	371
 Chapter 17: Power Distribution System Design.....	373
<i>Mark Alexander, Senior Staff Engineer, Xilinx, Inc.</i>	
17.1: Abstract.....	373
17.2: Required PCB Decoupling Capacitors.....	373

17.3: Basic Decoupling Network Principles .....	379
17.4: Role of Inductance .....	381
17.5: Simulation Methods .....	395
17.6: PDS Measurements .....	395
17.7: Optical Decoupling Network Design .....	400
17.8: Other Concerns and Causes .....	401
Chapter 18: Aperiodic Resonant Excitation of Microprocessor ..	405
Power Distribution Systems and the Reverse Pulse Technique	
<i>Victor Drabkin, Senior Member of Technical Staff, Hewlett Packard</i>	
<i>Chris Houghton, Senior Member of Technical Staff, Hewlett Packard</i>	
<i>Isaac Kantorovich, Senior Member of Technical Staff, Hewlett Packard</i>	
<i>Michael Tsuk, Senior Member of Technical Staff, Hewlett Packard</i>	
18.1: Abstract .....	405
18.2: Introduction .....	405
18.3: Definitions .....	406
18.4: Reverse Pulse Technique – Plausible Reasoning .....	407
18.5: Reverse Pulse Techniques – Proof .....	411
18.6: Development .....	418
18.7: Conclusion .....	419
Chapter 19: Modeling Noise on Printed Circuit Board .....	421
Power Planes	
<i>John Grebenkemper, Ph.D., Development Engineering Manager, Hewlett Packard</i>	
19.1: Abstract .....	421
19.2: Introduction .....	422
19.3: Phases of Power Plane Phase .....	423
19.4: Methods to Predict Noise .....	426
19.5: Noise Prediction Method .....	427
19.6: Noise Control Methods .....	436
19.7: Bypass Capacitor ESR .....	439
19.8: Measurement of Bypass Capacitors .....	443
19.9: Conclusion .....	445
Chapter 20: Toward Developing a Standard for Data .....	449
Input/Output Format for PDN Modeling and Simulation Tools	
<i>Ravi Kaw, Senior Staff Engineer, Agilent Technologies, Inc.</i>	
<i>Istvan Novak, Senior Staff Engineer, SUN Microsystems, Inc.</i>	
<i>Madhavan Swaminathan, Professor, Georgia Institute of Technology</i>	

20.1: Abstract.....	449
20.2: Introduction .....	449
20.3: PDN Classification.....	441
20.4: IO PDN + SDN .....	455
20.5: Desirable Common Features for Both PDNs.....	458
20.6: Proposed Requirements for Modeling Tools .....	459
20.7: Proposed Requirements for Simulation Tools.....	461
20.8: Methodology .....	463
20.9: Standards .....	462
20.10: Standards .....	463
20.11: Conclusion.....	464
Chapter 21: Overview of Frequency-Domain Power-.....	439
Distribution Measurements	
<i>Istvan Novak, Senior Signal Integrity Staff Engineer, SUN Microsystems</i>	
21.1: Abstract.....	439
21.2: Block-Based Video Decompression Algorithms.....	440
21.3: Architectural Evaluation Phase and IP Selection.....	441
21.4: Design Phase.....	446
21.5: MP Partition of Decoder Applications and .....	460
Validation on ESL Models	
21.6: System Emulation on FPGA Platform.....	461
21.7: Physical Design of Full System .....	462
21.8: Packing Video Decoder IP .....	463
21.9: Conclusion.....	465
Chapter 22: Simple Transmission Line Causal Model for.....	501
Multilayer Ceramic Capacitors	
<i>Istvan Novak, Senior Staff Engineer, SUN Microsystems</i>	
<i>Gustavo Blando, Staff Engineer, SUN Microsystems</i>	
<i>Jason R. Miller, Senior Staff Engineer, SUN Microsystems</i>	
22.1: Abstract.....	502
22.2: Introduction: Present Modeling Options .....	502
22.3: Periodically Loaded Causal Transmission-Line Model ..	509
22.4: Conclusion.....	521
<b>Author Biographies .....</b>	<b>??????</b>