3D Connection Artifacts in Modern PDN Measurements

Istvan Novak, Gustavo Blando, Ethan Koether, Kristoffer Skytte, John Phillips, Shirin Farrahi, Abe Hartman, Sammy Hindi, and Mario Rotigni

Based on *3D Connection Artifacts in PDN Measurements*, DesignCon 2023, Santa Clara, CA

INNOVATIVE TECHNOLOGIES • SUDDEN SERVICE • GLOBAL REACH

SPEAKERS

Ethan Koether

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Ethan Koether earned his master's degree in Electrical Engineering and Computer Science in 2014 from the Massachusetts Institute of Technology. He is a Sr. SIPI engineer with Amazon's Project Kuiper where he has been for the past 1.5 years. Prior, Ethan worked at Oracle Corporation for 7 years. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

Kristoffer Skytte

Application Engineer Architect, Cadence
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Kristoffer Skytte is Application Engineer Architect at Cadence focusing on chip, package, board and full system analysis. He is helping companies in Europe apply simulation tools to solve some of their toughest SI, PI and EMC related challenges in their design process. One of his interest is system level immunity/emissions and how these affect overall system performance. Kristoffer has a M.Sc.EE. degree from the Technical University of Denmark.

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SPEAKERS

John Phillips

Principal Applications Engineer, Cadence

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John Phillips is a principal application engineer with Cadence Design Systems. Prior to joining Cadence John worked at many different companies covering such diverse marketplaces as high end compute platforms and mil-aero. During his career he acquired a broad knowledge of SI, PI and EMC at chip, board and system level. John holds an MSc. Degree form Bolton University, UK. His current interests are SI/PI co-simulation and modelling for both serial and parallel interfaces.

Shirin Farrahi

Senior Principal Software Engineer, Cadence

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Shirin Farrahi is a Senior Principal Software Engineer at Cadence working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

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SPEAKERS

Abe Hartman

Principal Hardware Engineer, Oracle Corporation
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Joseph 'Abe' Hartman is a Principal Hardware Engineer focusing on system signal and power integrity at Oracle. Abe has worked as a signal integrity engineer at Amphenol TCS, Juniper Networks, and Enterasys. Abe also worked at General Motors. Abe holds a MS in Electrical Engineering from the University of Massachusetts-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, a BS in Mechanical Engineering and a BS in Electrical Engineering from Kettering University in Flint, MI.

Sammy Hindi

Senior Principal Engineer, Ampere Computing Inc.
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Sammy Hindi is a Senior Principal Engineer at Ampere Computing. He has over 30 years of engineering experience, focusing on high-speed design, SerDes, Interconnect, Packaging, and forward error correction codes. Besides engineering, he enjoys reading in astrophysics and mathematics. He also enjoys biking, photography, and family life.

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SPEAKERS

Mario Rotigni

SoC EMC Manager, STMicroelectronics

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Mario Rotigni was born in Bergamo, Italy, in 1958 and received a diploma in Electrical Engineering in 1977. He was with the R&D Department of Magrini Galileo for 12 years working on design of process instrumentation operating in very hostile electromagnetic environments. After designing an Automatic Test Equipment for microcontrollers he joined STMicroelectronics, holding various position in the Engineering, Design, R&D in the Automotive Product Group. He is currently in charge of the EMC of Microcontroller and System on Chip for the automotive applications. He has co-authored 21 papers about EMC of Integrated Circuits for various Conferences.

Gustavo Blando

Senior Principal SI Architect, Samtec

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Gustavo Blando is a Senior Principal SI Architect at Samtec Inc. In addition to his leadership roles, he's charged with the development of new SI/PI methodologies, high speed characterization, tools and modeling. Gustavo has twenty-five years of practical experience in Signal Integrity, high speed circuits design and has participated in numerous conference publications

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SPEAKERS

Istvan Novak
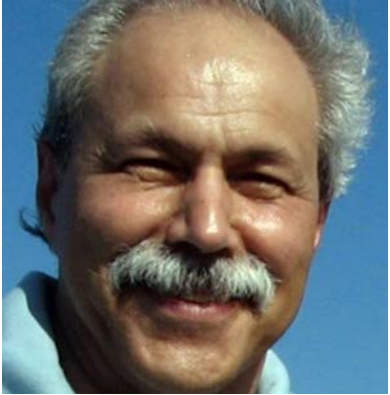
Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 μm power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-nine patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website. Istvan was named Engineer of the Year at DesignCon 2020.

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Outline

- PDN Measurement Background

- 3D PDN Measurement Artifacts

- PDN Simulation Background

- Sensitivity Analysis

- Measurement Setup

- Copper Sheet Investigation

- Test Board Investigation

- Customer Board Investigation

- Conclusion

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The Motivation, the Paradigm Shifts Over Time

- Paradigm Shift #1: late 1990s
  - Requirements to measure milliohms
  - Frequency domain design and verification
 - Horizontal incremental impedance was relatively small
  - 3D interactions in PI measurements were small
  - **Solution: VNA with Two-port Shunt-through connection**
  - Frequency and time-domain verifications lined up

- Paradigm Shift #2: early 2020s
  - Requirements to measure microohms
  - 3D interactions in PI measurements become dominant
  - Horizontal incremental impedance becomes relatively high
  - Increasing gap between frequency and time-domain verification results
  - **Solution: ???**

Cadence Live Boston, September 12, 2023

Measuring a Full PDN
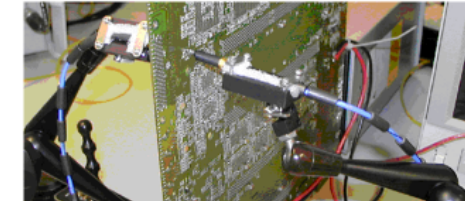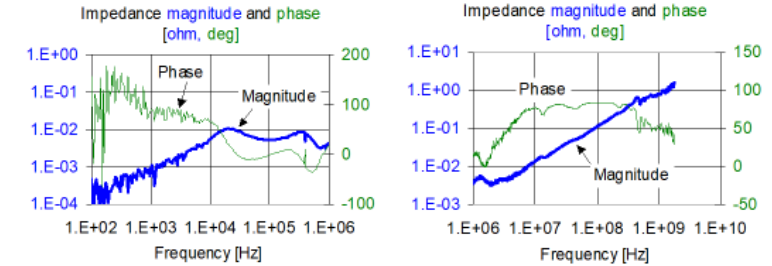
June 23, 2003   DesignCon East 2003 HP-TF1   Istvan Novak   26

- Oracle M8/T8 CPU module
- 1 CPU
- 6" x 5"
- 637 capacitors
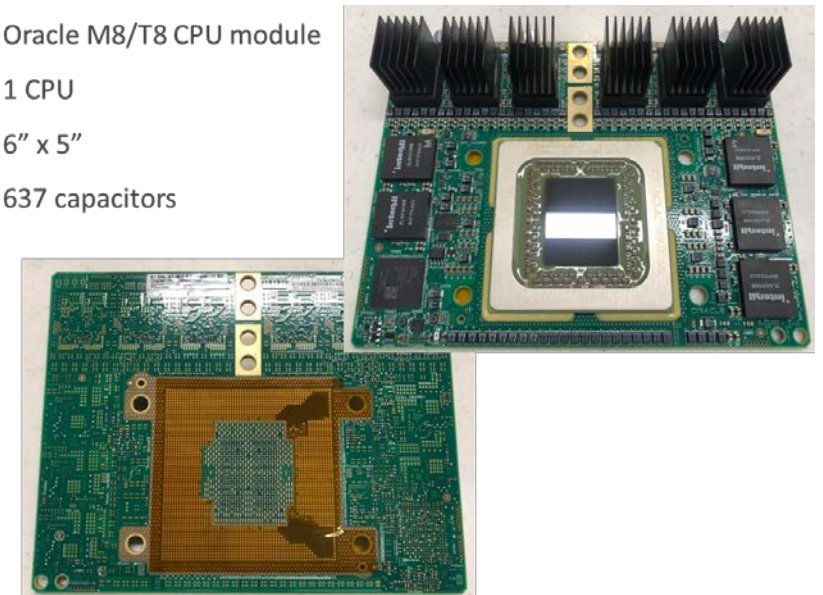
From: Is Power Integrity the New Black Magic?
Cadence Design Forum, April 2021

PDN Measurement Background

- Two Port Shunt-Thru Measurement
  - Transmission measurements have greater dynamic range than reflection measurements
  - Probe series parasitics are suppressed with this strategy

- DUT impedance can be extracted from S21 measurement

- More complete description of DUT can be obtained with [S] >> [Z] transform having T-network configuration
  - Requires S11 and S22 measurements which will be inaccurate
  - Enables removal of series parasitics
  - Does not remove mutual coupling within PCB launch area

$$S_{21} = \frac{Z_{DUT}}{25 + Z_{DUT}} \cdot \frac{V_S/2}{V_S/2} \rightarrow Z_{21} = 25 \cdot \frac{S_{21}}{1 - S_{21}}$$

From thru calibration

Consider full impedance matrix in T-network configuration
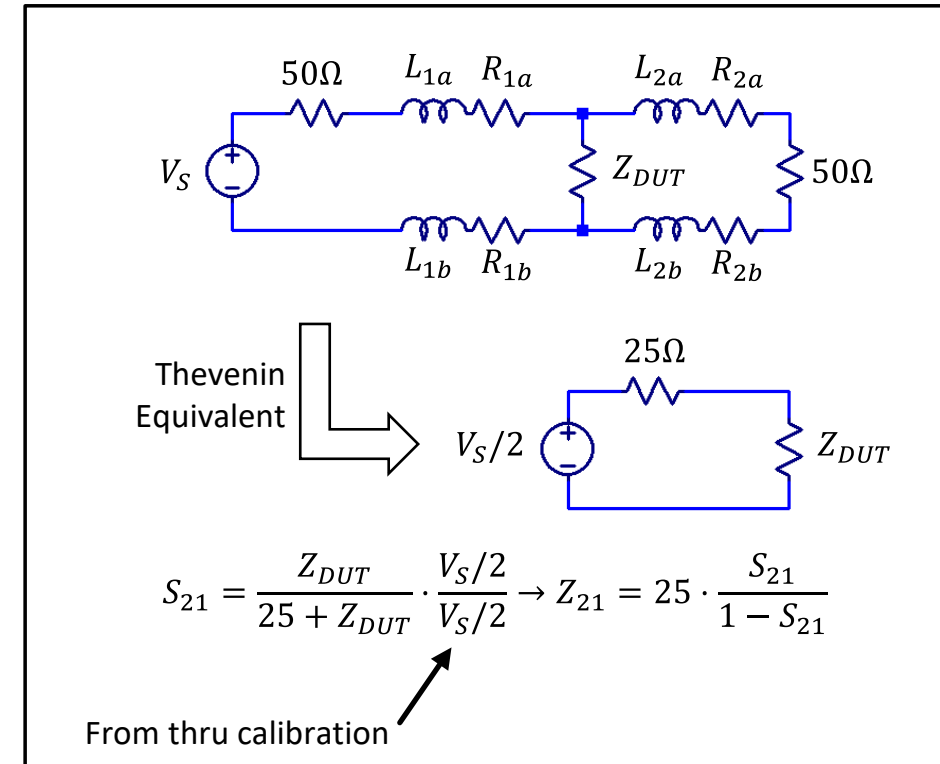
$$Z_A = Z_{11} - Z_{12}$$

$$Z_B = Z_{22} - Z_{21}$$

$$Z_C = Z_{12} = Z_{21}$$
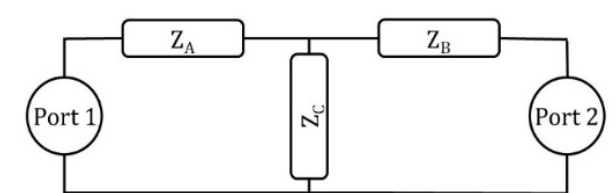
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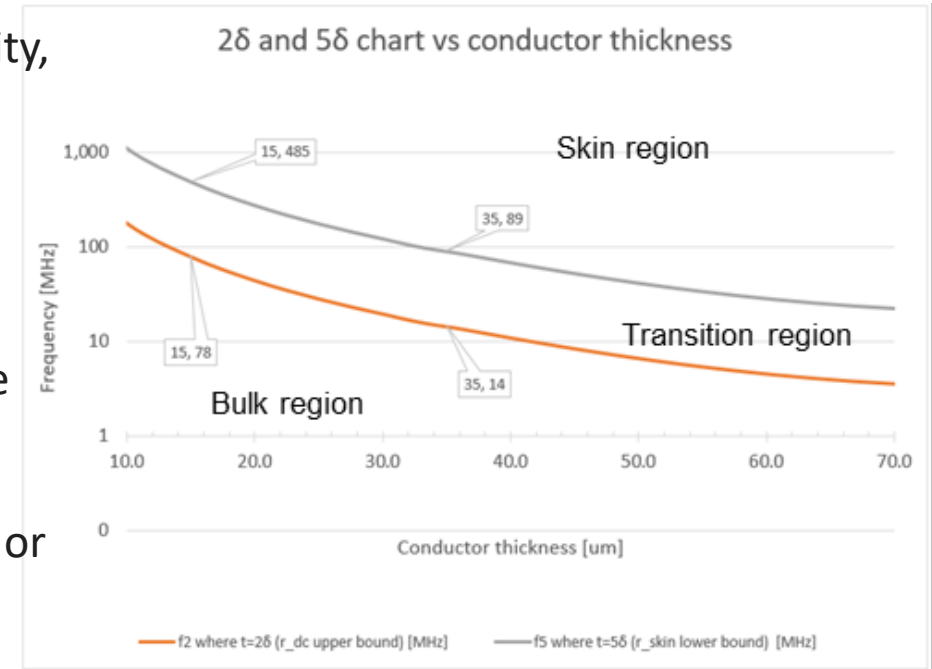
- Conclusion

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3D PDN Measurement Artifacts

- PDN measurements require connecting to the DUT, e.g., with probes

- No techniques for avoiding 3D PDN measurement artifacts in electrically dense regions (BGA, pin-field, mechanical constraints, etc.)

- Instrument calibration does not remove coupling to/from DUT via-trace landing geometry

- De-embedding these artifacts in postprocessing requires S11 and S22 data, which may carry large errors in PDN measurements

- Hybrid field solvers approximate local details (e.g. vias, traces, antipads)

- These parasitic measurement coupling effects must be investigated and understood for proper removal from measurement data
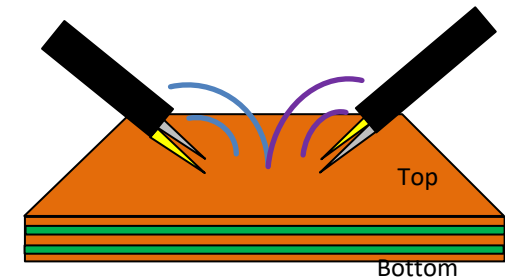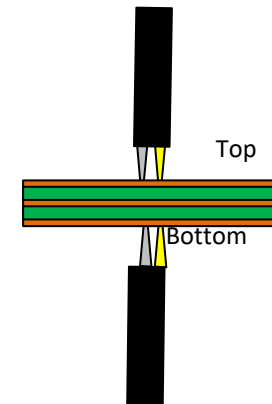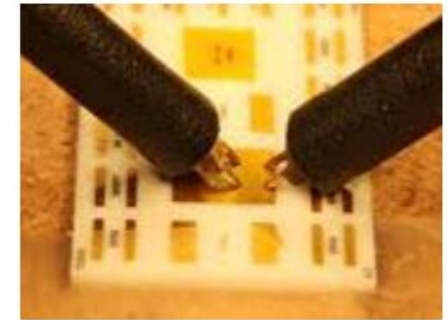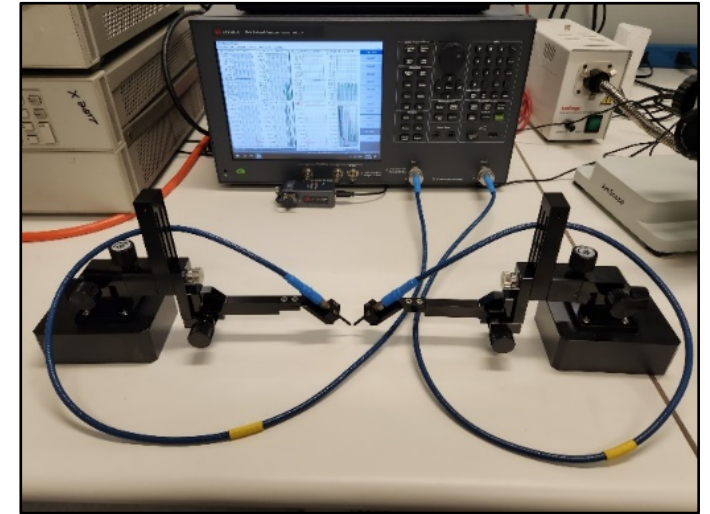
PDN Measurement Coupling

- Probe landing geometry has coupling factor, k:
  - Power/GND via pair inductive loop, L_P
  - Plane inductance between via launches, L_G

- Z_C will include term from via coupling
  - Coupling term will grow with frequency and can mask DUT impedance
  - Minimize term by reducing PWR/GND probe tip distance, reducing L_P
  - Minimize term by putting probe1 and probe2 close together, reducing L_G
    - Maximizes contribution from coupling between probes, themselves
  - L_P and L_G are not easy to isolate

- Two port shunt through measurement good at removing series parasitics
  - Consider probe landing via pads and vias as extension of DUT that can be de-embedded to port centered between them
  - Post-processing step after standard two port shunt thru measurement to remove launch parasitics and isolate Z_{DUT}
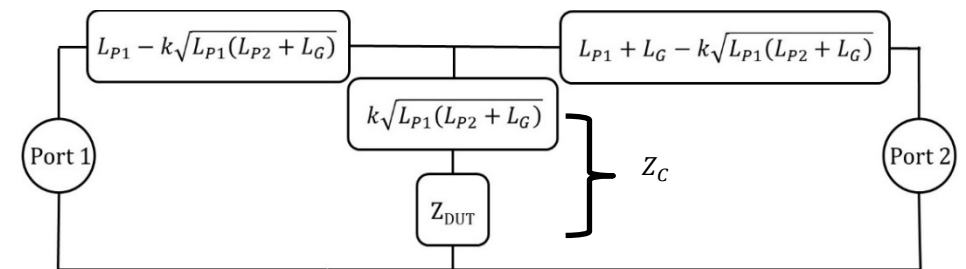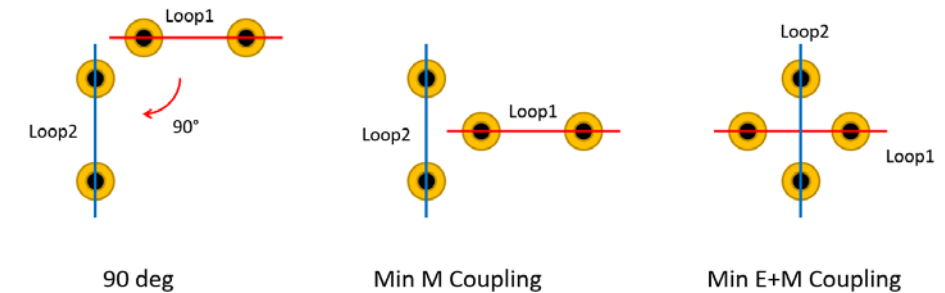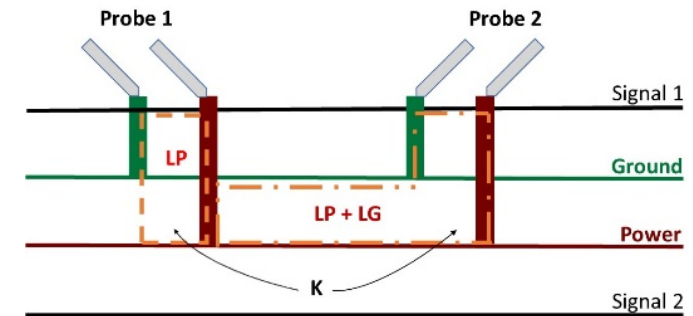
$$Z_{DUT} \sim 25 \cdot \frac{S_{21}}{1 - S_{21}} - j\omega k \sqrt{L_p(L_p + L_g)}$$

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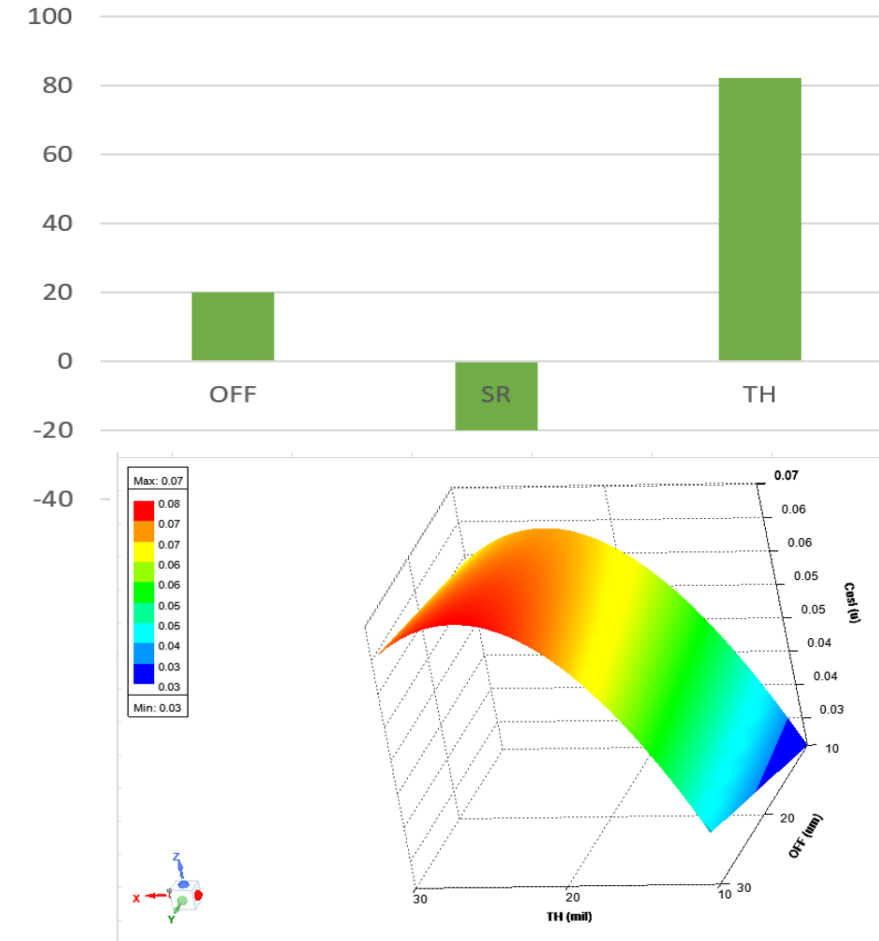
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PDN Simulation Background

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}.$$

- Electrical parameters defining DUT need to be captured in simulation setup (e.g. stack-up dimensions, plating thicknesses, dielectric constant, conductivity, etc.)

- Hybrid EM solvers (Cadence PowerSI) commonly used for PDN simulations
  - Decompose the DUT into plane modes, transmission line modes, and localized discontinuity models (e.g. vias and padstacks)

- Study of detailed localized behaviors may require 3D EM extraction (Cadence Clarity)
  - Be careful about assumptions in full wave solver for low frequency, low frequency stability settings and volumetric conductor mesh can be used or
  - Quasi-static solver may be more appropriate for PDN studies such as Cadence PowerSI
  - At any rate for these low impedances careful studies of meshing and convergence should be completed

- Low frequency characterization challenging
  - Full bulk current conduction mode when conductor thickness < 2x δ
  - $\sqrt{f}$ current flow scaling when conductor thickness > 5x δ

2δ and 5δ chart vs conductor thickness

Skin region

Transition region

Bulk region

15, 485

35, 89

15, 78

35, 14

Frequency [MHz]

Conductor thickness [um]

—— f2 where t=2δ (r_dc upper bound) [MHz]   —— f5 where t=5δ (r_skin lower bound) [MHz]

(35μm ~1oz copper)

The bulk conduction region is over a 75MHz wide band (14MHz – 89MHz) and is typically where low PDN impedance is designed.
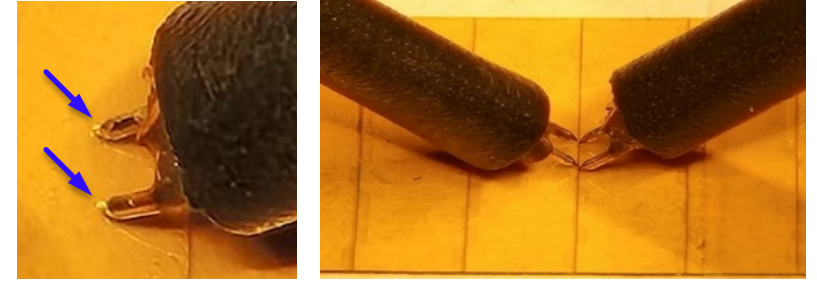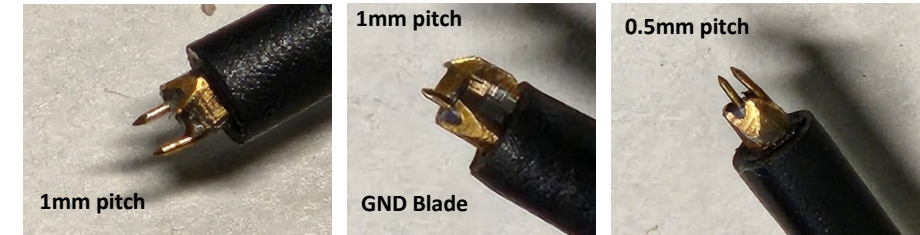
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Sensitivity Analysis

Cost Local Sensitivity (%)

- Sensitivity analysis completed with Ansys HFSS to identify high priority parameters to include when modeling probed measurement of DC resistance

- DC resistance of simulated structure function of
  - Sheet thickness (TH): [10mil, 23mil]
  - How deep probe goes into the copper (probe offset, OFF): [10um, 30um]
  - Surface roughness of the copper: Nodule radius [2um, 6um]

- $$\min_{\text{TH,OFF,NR}} \left\{ \left| Re\{Z_{C,Sim.}\,(f = 100Hz, \text{TH, OFF, NR})\} - 0.407m\Omega \right| \right\}$$
  - 0.407mΩ measured impedance with straight probe orientation at 100Hz

- Cost function has highest sensitivity to sheet thickness variation

- Optimizing values are:
  - TH = 10mils (minimum value of range)
  - OFF = 10um (probe barely touching)
 - Surface Roughness NR =6um (maximum value of range)
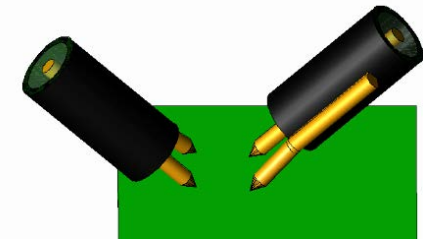
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Measurement Setup

- PDN impedance measurements commonly completed with VNAs using two port shunt thru configuration

- Common mode choke used in path of port 2:
  - Ferromagnetic materials sensitive to AC bias and Port 2 sees little AC bias in S_{21} measurement

- Emphasized aligning probes robustly as coupling sensitive to small changes in measurement geometry

- Probes with three different tip configurations investigated since loop area directly impacts coupling

- Probe spacing and landing angle measured precisely

- 45° landing angle used due to probe protection sleeve and optical vision system in use

- Preliminary measurements taken to validate setup

(Left) Deflection of light shows probe touchdown. (Right) Mylar sheet supplied with probes confirm alignment.

Three different probe types were investigated.

(Left) probe landing spacing measured. (Right) 45 degree probe landing angle used.

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Copper Sheet Investigation

- Copper sheet used as first DUT [15.6mm x 31.5mm x 0.25mm]

- Stresses measurement setup's low impedance measurement capabilities and cable braid error mitigation

- $R_{21} \propto 1/d^2$ d is spacing between probes
  - Current distribution out of positive probe 1 tip returning to negative probe 2 tip falls off as probe 2 moves away from probe 1
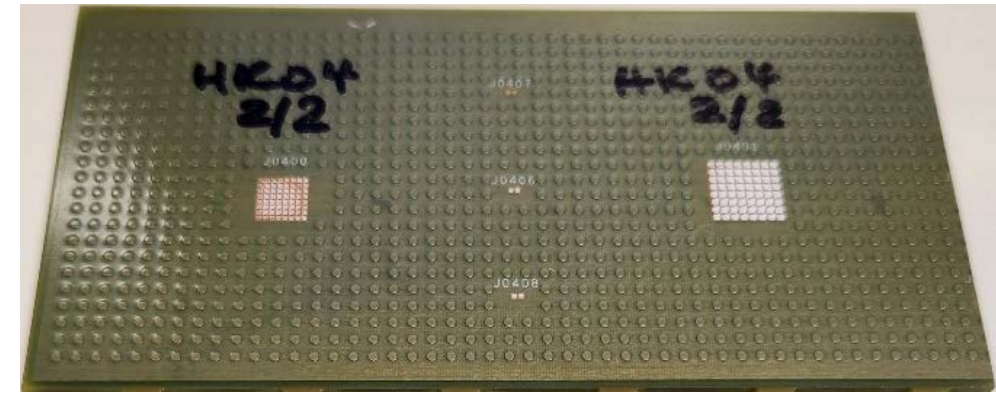 - Results in voltage excitation at probe 2 due to current at probe 1 falling off as probe 2 moves away from probe 1
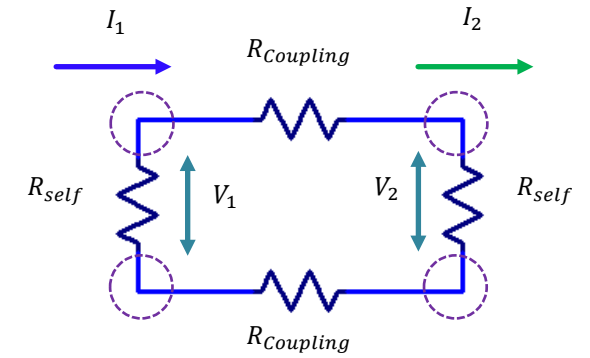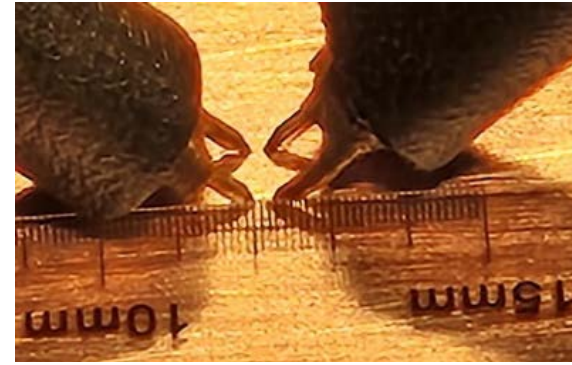
(Left) Probe landings for copper sheet impedance measurement. (Right) Equivalent circuit for probe landing configuration.
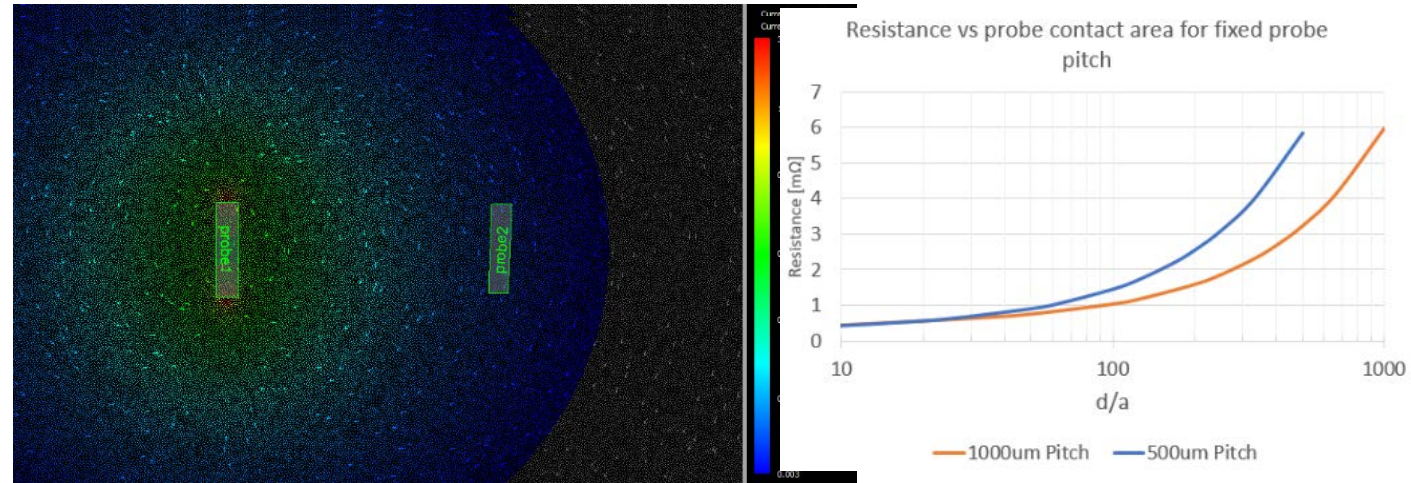
(Left) Current density plot of two port shunt thru measurement on copper sheet simulated with Cadence PowerDC. (Right) Resistance between probe tips for 500um and 1000um pitch. d/a is the ratio between the probe distance, d, and contact area of the probe points, a.

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Copper Sheet Investigation

- Simulations include both probes on top-side of 5mm x 5mm 1oz copper sheet with 1mm pitch

- Probe models parameterized

- Probe models constructed of Beryllium with 2.5e7 S/m (43% of copper's conductivity)

- Quasi-static solver (Ansys Q3D)
  - Probes 1 and 2 each had a source on center probe tip and GND ring while sink included on opposite side of copper sheet
  - Surface roughness not modeled

- Full-wave 3D field solver (Ansys HFSS)

- Impedance measurement and simulation consistent across six probe landing permutations suggesting T-network transform being performed correctly

- Correlation between impedance measurements, quasi-static 3D solver, and full-wave 3D field solver show good agreement in inductance but mismatch in lower frequency, resistive region
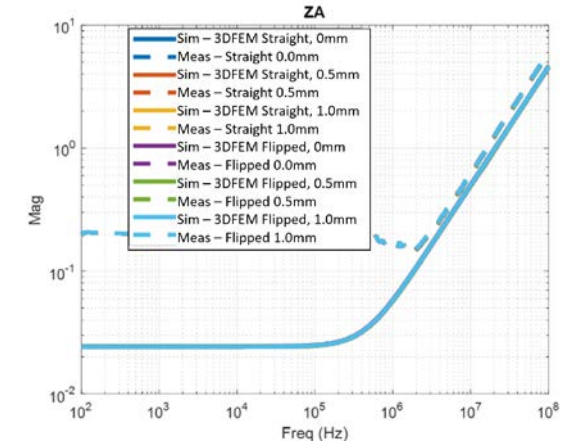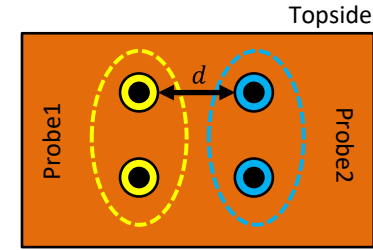
(Left) probe configuration setup and (Right) Impedance measurements and full-wave 3D field solver results across six permutations of 1mm probe configurations landed on the copper sheet.
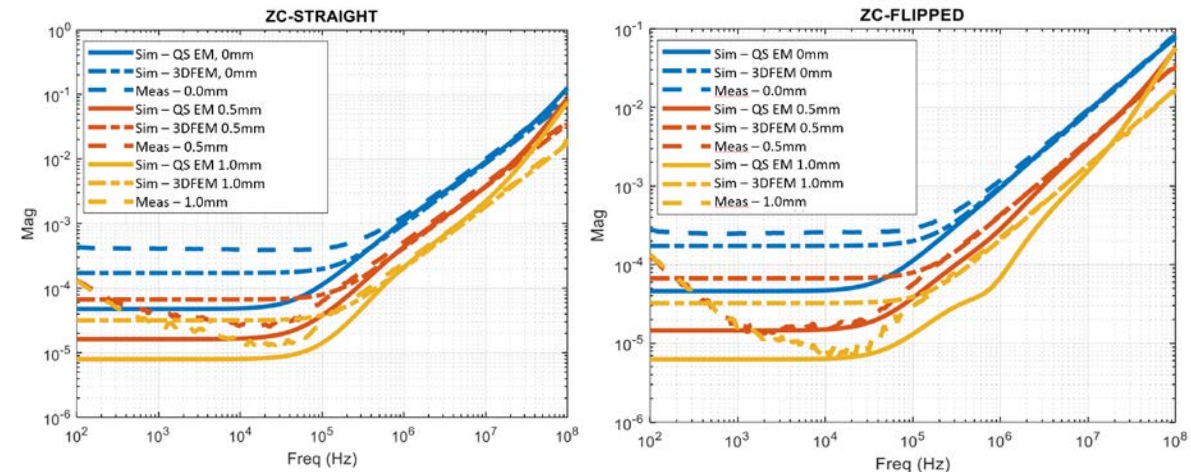
Impedance measurements, quasi-static 3D solver results, and full-wave 3D field solver results for "straight" probe orientation and "flipped" probe orientation.

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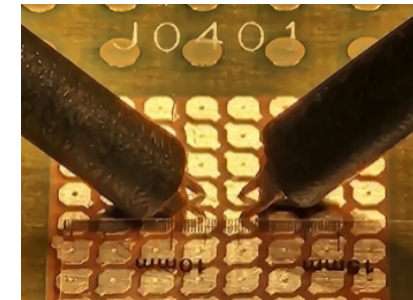- Conclusion

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Test Board Investigation

- Test board with 20 layers and 5 PWR-GND cavities

- Blind via arrays cut away from rest of board (J0401)

- Via array has alternating checkered board PWR-GND pattern

- Entire area of J0400 shorted for corresponding measurements

Test Board top-side view.

Blind via array under test.

Port landing configuration on via array with port location to which we de-embed DUT denoted in blue.

L1

Length = 64.16 μm

Length = 73.13 μm

L2

Length = 35.44 μm

Length = 24.23 μm

L3

Length = 34.99 μm

Through Via
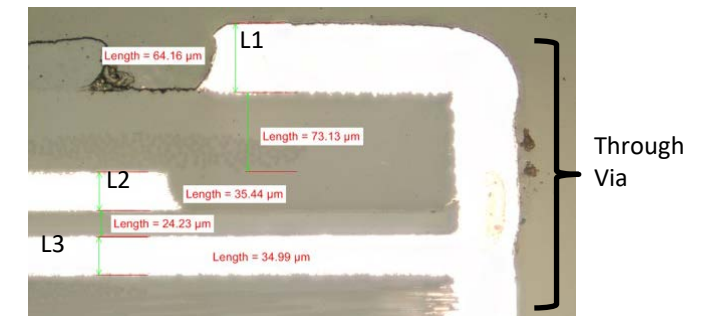
*Test board stackup cross section.*

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Test Board Investigation

- 3D FEM solver (Cadence Clarity) setup with ports at connector models mimicking ECAL setup with third port at center region

- Clarity setup with lumped ports at landing pads mimicking wafer probe substrate calibration with third port at center region

- Hybrid EM solver (Cadence PowerSI) setup with ports at landing pads mimicking wafer probe substrate calibration with third port at center region

- Reasonable agreement between simulated and measured resistance and inductance

- Resistance varies as a function of extraction method and port location

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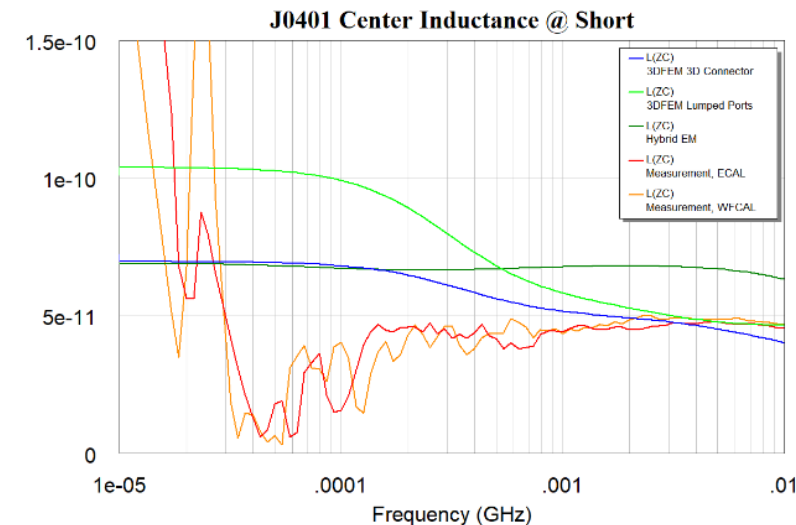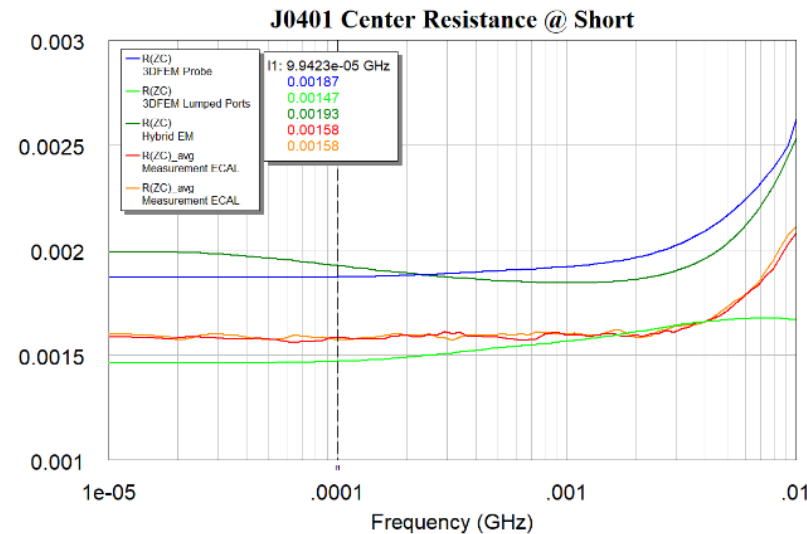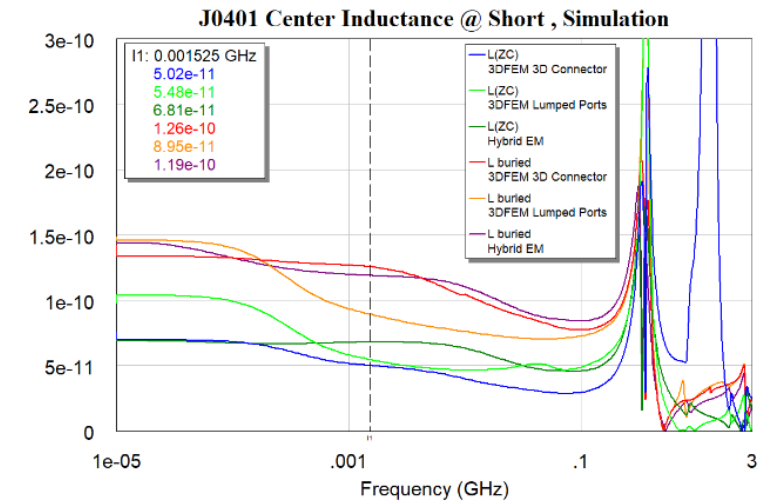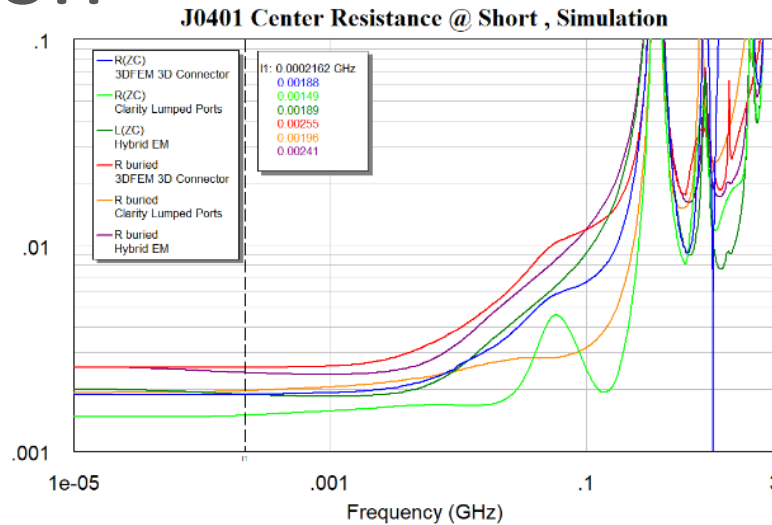
Test Board Investigation

- Buried port shows higher resistance compared to external ports

- Lumped port extraction shows more frequency dependence below 100MHz

- Buried ports show slightly higher inductance than external ports

- Inductance extraction from measurement not stable at frequencies below 1MHz

- Results from the different EM simulators agree well with greatest variation in inductive region

- 3D FEM model with full 3D probe models expect to best capture physical behavior because coupling captured is physical

- Placing lumped ports in the pads may result in coupling between ports due to their physical closeness

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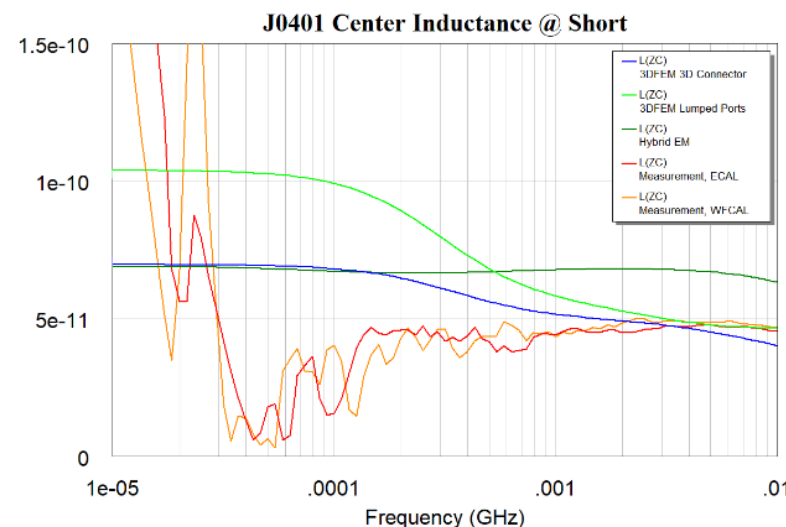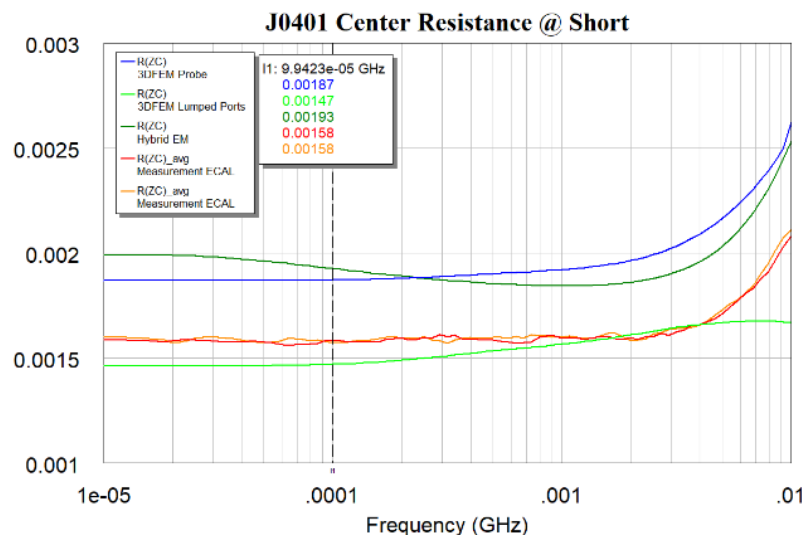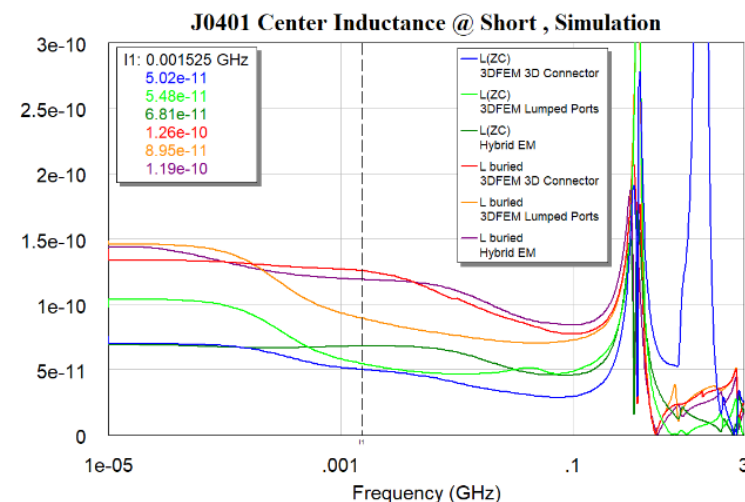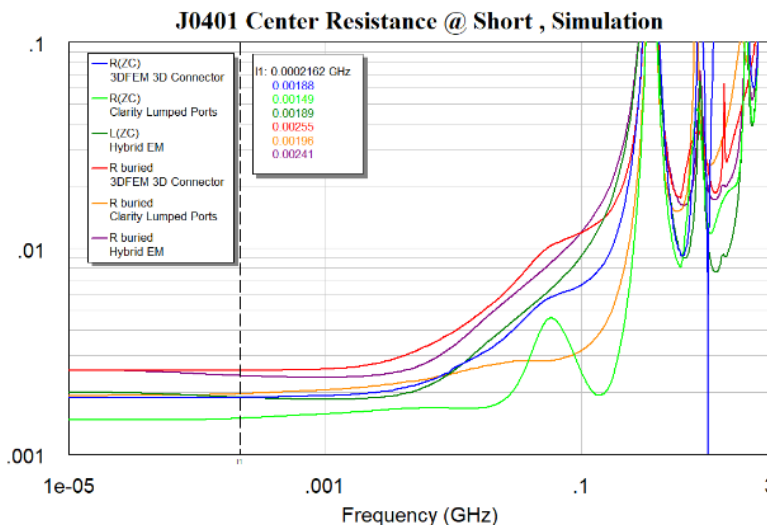
Test Board Investigation

- For both ECAL and wafer cal, measurement and simulation results show good correlation up to 10MHz

  - Best correlation between measurements and 3DFEM simulation results with lumped ports placed directly on pads

- Z_C from ECAL and wafer cal measurement setups show good agreement showing coupling from probe-to-probe or probe-to-substrate does not influence the results significantly

  - Expected to get worse in higher frequency range, when probing through vias buried deep in the stackup, or when probing in tighter pitch BGAs
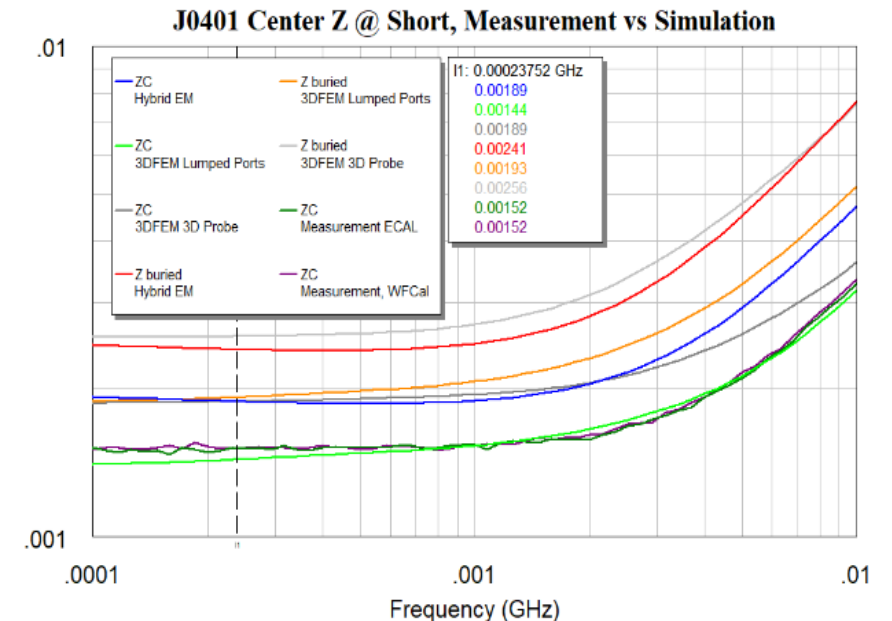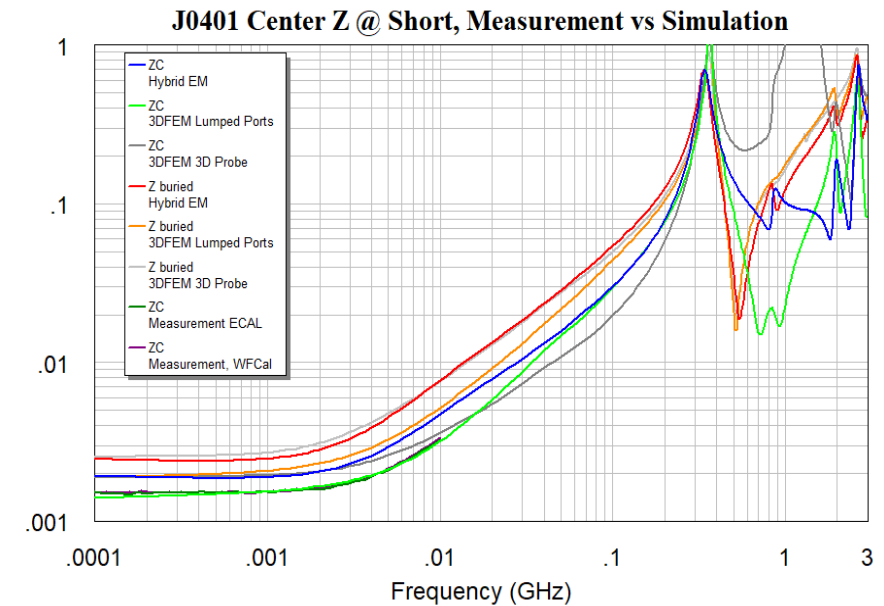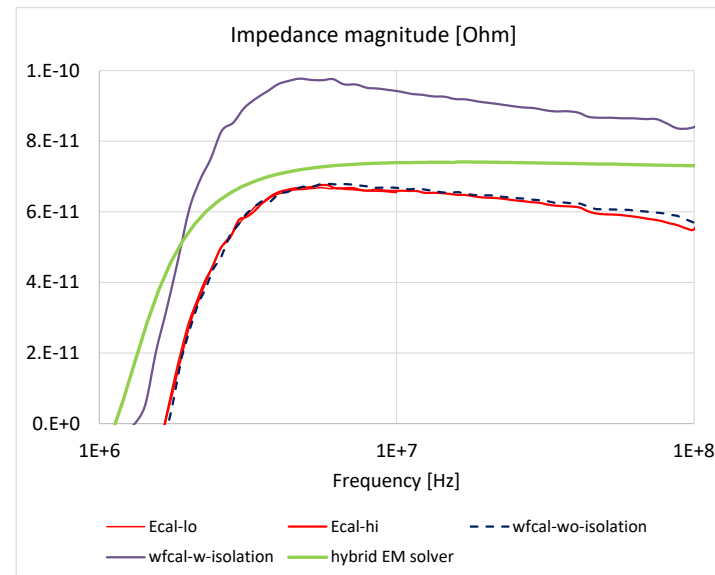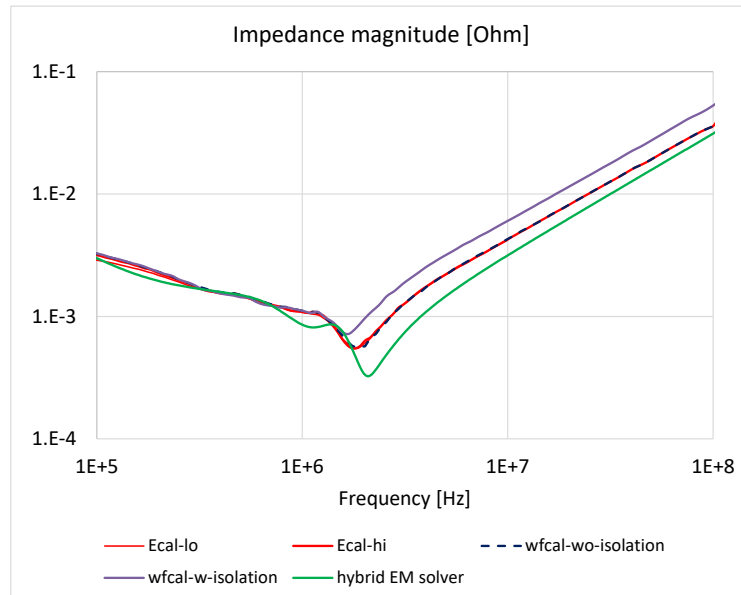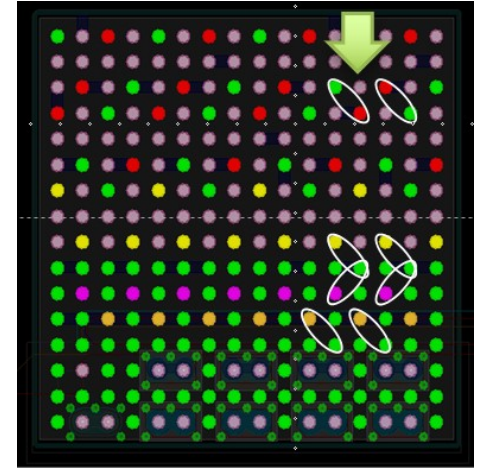
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Customer Board Investigation

- 12 Layer customer board for a high speed chip with 1mm pitch BGA field

- Probes are flipped and offset

- ECAL and wafer probe cal measurements without isolation lie on top of one another

- Wafer probe coupling with isolation shows higher inductance because probe tip coupling is removed

    - Flipped probe coupling reduces effective inductance

- PowerSI predicts impedance between wafer cal measurement results with isolation and without isolation
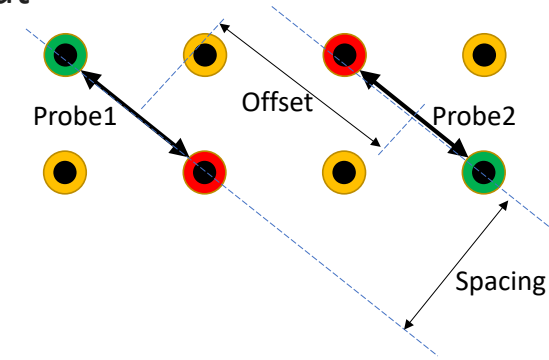
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Outline

- PDN Measurement Background

- 3D PDN Measurement Artifacts

- PDN Simulation Background

- Sensitivity Analysis

- Measurement Setup

- Copper Sheet Investigation

- Test Board Investigation

- Customer Board Investigation

- **Conclusion**

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Conclusion

- Traditional VNA calibration does not remove the effects of coupling between the DUT via-trace structures while measuring PDN impedance with probes in close proximity.

  - This coupling can mask a low DUT impedance in measurement if not de-embedded

- The isolation calibration step of the typical VNA calibration flow does not provide complete removal of the coupling effect.

- Probe spacing, offset, orientation and landing angle all heavily influence probe-tip coupling and therefore are all important parameters to be kept the same during calibration and measurements.

- Simulation engine selection needs to be considered carefully for good measurement correlation

- With the geometries we examined, we achieved good correlation between impedance simulation and measurement

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Acknowledgements

- The authors wish to thank the following individuals and companies for their help and support:
  - Jin-Hyun Hwang, DuPont
  - Pete Pupalaikis, Nubis Communications
  - Steve Sandler, Picotest
  - Richard Zai, PacketMicro
  - Graeme Ritchie, Cadence

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Thank you for attending