Manuscript for Apex2001, January 16-18, 2001, San Diego, CA

Impedance and EMC Characterization Data of Embedded Capacitance Materials

Istvan Novak
SUN Microsystems, Inc.
One Network Drive
Burlington, MA 01803
istvan.novak@sun.com

Abstract

Passive components embedded in printed circuit boards promise several advantages. In high-speed computer applications, the biggest electrical advantage is reduced parasitics by eliminating connecting vias. One attractive way of embedding bypass capacitors is to use power-ground plane pairs in close proximity in the PCB stack up, possibly with high dielectric constant material in between.

The paper gives measured electrical impedance and radiation results of embedded capacitive layers. Self and transfer impedances of power-ground plane pairs of embedded capacitance structures are shown.

Measuring the impedances of closely-spaced power-ground planes create a special challenge, because most impedance analyzer setups have an inductance limit in the order of 100pH, which makes it hard to characterize closely spaced planes correctly at high frequencies. One suitable measurement technique is explained, which enables the reduction of inductance limit by at least one order of magnitude.

Close-field radiation data of various embedded capacitance test boards are also shown with different dielectric thickness and dielectric constant values.

Introduction

There has been considerable interest recently to employ capacitive layers, embedded inside the printed-circuit board. The embedded capacitive (and/or resistive) layers can be used either to form small-size distributed or lumped circuits – such as filters, terminators, etc.- or to create embedded distributed bypass capacitor layers. For embedded bypass capacitor applications, the static low-frequency capacitance is given by the following expression:

$$C = e_0 e_r \frac{A}{s}$$

where A=a*b and s are the area and separation of the conductors, respectively; ε_r is the relative dielectric constant of the insulator, and ε_0=8.85pF/m is constant.

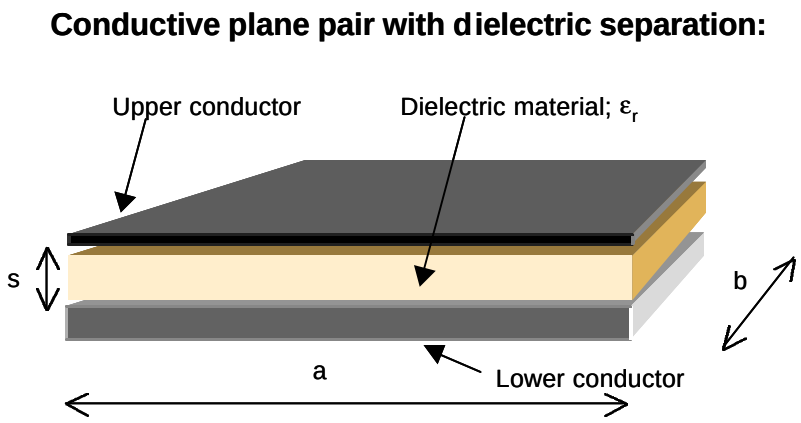

Figure 1: Plane capacitor as part of the multiplayer printed-circuit board structure.

An obvious choice to increase the capacitance is either to decrease the separation of planes, and/or to increase the relative dielectric constant. The surface area of the planes is usually defined by the application, and is not freely selectable by the designer. In a multiplayer stack up, one can decrease the separation between the power and ground planes by placing them next to each other, so that signal trace layer(s) do not increase the separation. The widely known and presently used embedded capacitance material is the power-ground plane sandwich with a nominal 2-mil FR4 separation (see e.g., [1] and [2]). Half-mil and one-mil dielectric materials are also available [3], though so far they found applications mostly in flexible and small-size rigid boards. The relative dielectric constant of the regular fiber-glass and polyimide printed-circuit-board materials is in the approximate range of 3…5. Higher dielectric constants have also been reported, see e.g., [4] and [5]. Very thin dielectrics combined with a possible high dielectric constant have been described in [6]. Earlier this year, the Embedded Capacitance Consortium published its findings on several of the newly developed materials [7].

A higher capacitance in the printed circuit board is expected to convey at least two electrical benefits: reduced number of discrete bypass capacitors, and reduced radiation from the printed-circuit board. Depending on the applications, some systems may enjoy a significant reduction of discrete bypass capacitors. Medium and high-power digital circuits, however, require a wide-band low impedance on the supply rails, therefore the capacitance provided by the embedded layers need to be complemented by discrete capacitors [8]. In such applications, the primary interest is to provide a low-impedance wide-band conduit among the power source, bypass capacitors and the electronics. At high frequencies, the interconnecting impedance of the planes become inductive, and ultimately it is the equivalent inductance of the power-ground plane pair that defines the effectiveness and performance of power-distribution system.

In this paper, an overview is given about the impedance and EMI test results of some of the test vehicles used at SUN Microsystems.

Test board construction

One of the test boards has an outline of 20” x 10”. The construction is six copper layers, nominally with 0.093” total board thickness. Every layer nominally had one-ounce copper. There were two thin cores (L2-L3, and L4-L5) with nominally 2 mil dielectrics, 8 mils below the surfaces. In the impedance-measurement tests, the surface signal traces were left floating, and were not included in the testing in any way. Three of the copper planes on the thin cores (on layers 2, 3, and 4) extend unsplit throughout the entire area of the board, the bottom side ground plane on layer 5 is split in the middle by a narrow vertical gap. This splits one of the planes, but the unsplit layer 4 copper plane connects the layers. For connecting bypass capacitors and measuring probes, there are a group of three vias connected to the four planes at every inch interval on the board area. As shown in Figure 2c, the vias are arranged in a way that either a 0.082” semirigid open-end probe or an SSMB PC-mount jack’s two pins can be conveniently used to make connections to the planes.

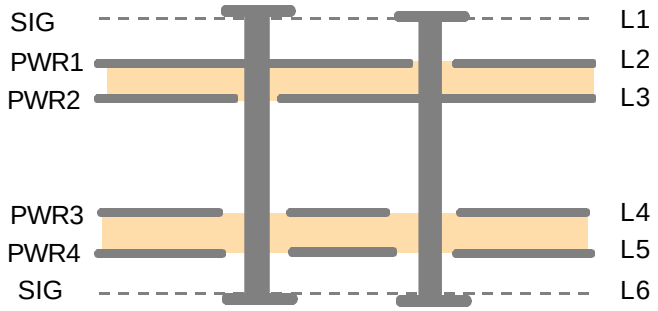

Figure 2a: Stack up of test board.

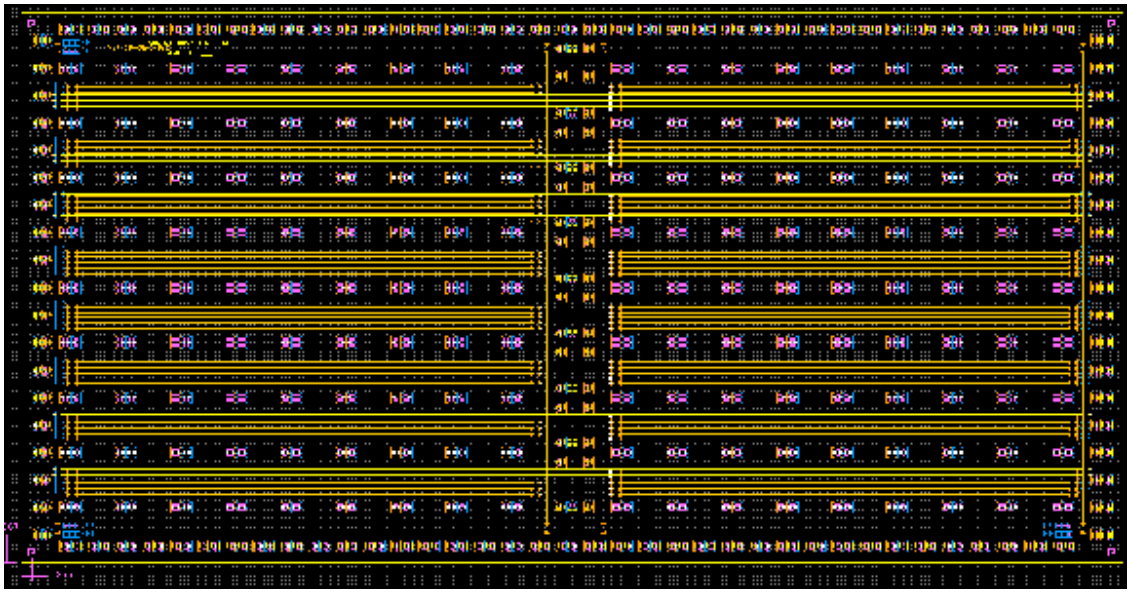

Figure 2b: Top view of the six-layer test boards. The outline is 20” by 10”.

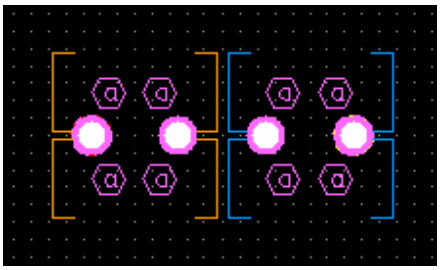

Figure 2c: Test point arrangement on the board.

The following materials have been included in the tests:

- 3.6-mil polyimide from Vendor A
- 1-mil polyimide from Vendor B
- 1.6-mil HiK laminate from Vendor C

On the test boards the dielectric thickness between layers 1 and 2, and layers 5 and 6 were kept at a fixed 8-mil value. Three flavors of the test boards were manufactured, with the laminates identified above. In one kind of test board the laminates in both plane pairs were the same.

There were 341 numbered connection points on the surface of the test boards. Ten of these test points were involved in the electrical measurements, as shown in Figure 3.

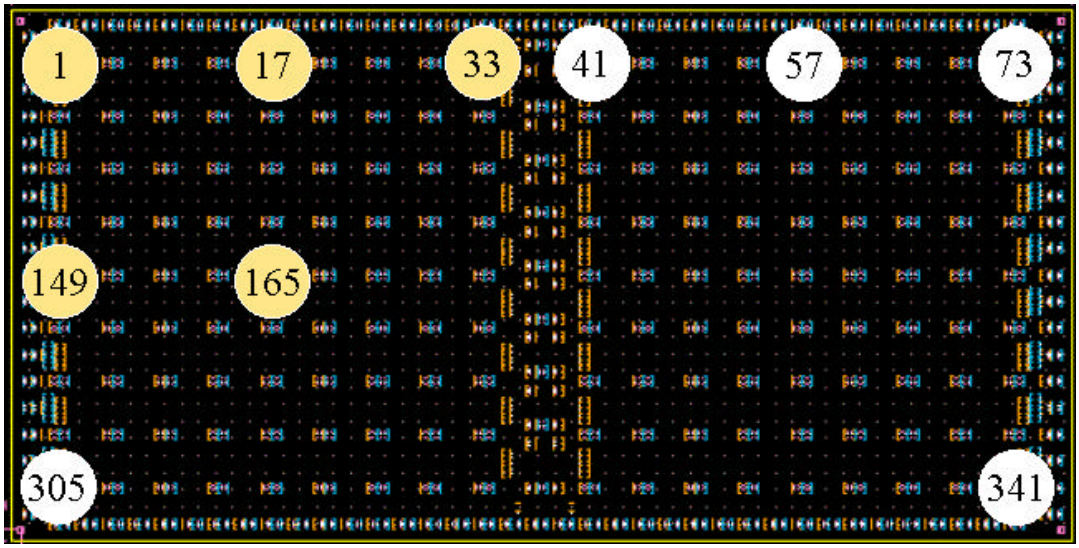

Figure 3: Test points on the board.

Impedance profile measurement setup

Measuring low impedances at high frequencies create special challenges. Impedance analyzers and network analyzers with one-port connections are limited to a few tens of milliohms as lowest impedance that can be repeatedly measured. It was shown in [8] that two-port self-impedance measurements with Vector Network analyzers can greatly reduce the effect of series connection discontinuities, the biggest error contributor of one-port measurements.

The vector-network analyzer is an instrument for measuring scattering parameters. A synthesized tuned source with calibrated source impedance and calibrated source voltage generates the incident wave at the excited port. The signal is connected to Port1 of the device under test through a directional coupler, which separates the a_1 and b_1 incident and reflected waves, respectively. Port2 of the device is terminated in the reference impedance, and the wave appearing at that port is b_2. A selective receiver is used to measure the incident and reflected waves at the ports.

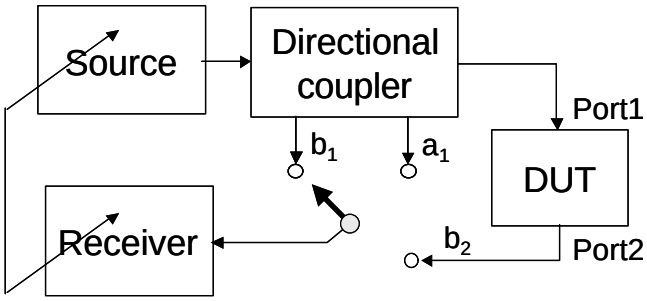

Figure 4.: Block schematic of a Vector Network Analyzer.

Because the frequency of the test signal is exactly known, the sensitivity and accuracy of the measurement is readily improved by locking the receive frequency to the transmit frequency, and/or by using averaging. In a first-order approximation, we may neglect the discontinuity connecting the probes to the DUT. We can do this because - as opposed to one-port measurements - the discontinuity is in series to 50 ohms rather than the very low unknown impedance of the DUT. The principle is similar to the four-wire DC resistance measurements: we use the source with two wires to launch a known current through the DUT, and use a second set of wires, Port 2 of the VNA, to measure the voltage across the DUT.

If we calibrate and set the S_{21} reading of the VNA without the DUT to zero dB, the unknown (low) self or transfer impedance can be approximated by $Z_{DUT} = S_{21}*25$. Here both Z_{DUT} and S_{21} are complex values, and S_{21} is the dimensionless ratio of the output and input waves. The impedance profiles shown in this paper were measured with a Hewlett-Packard HP4396 analyzer, in the 100kHz to 1.8GHz frequency range. It was found that at lower frequencies, up to a few MHz, the measurement noise floor could be reduced to about 100 micro ohms. At higher frequencies the limitation is in the probe connections, and with the probes shown in Figure 5 this limit was found to be about 5pH.

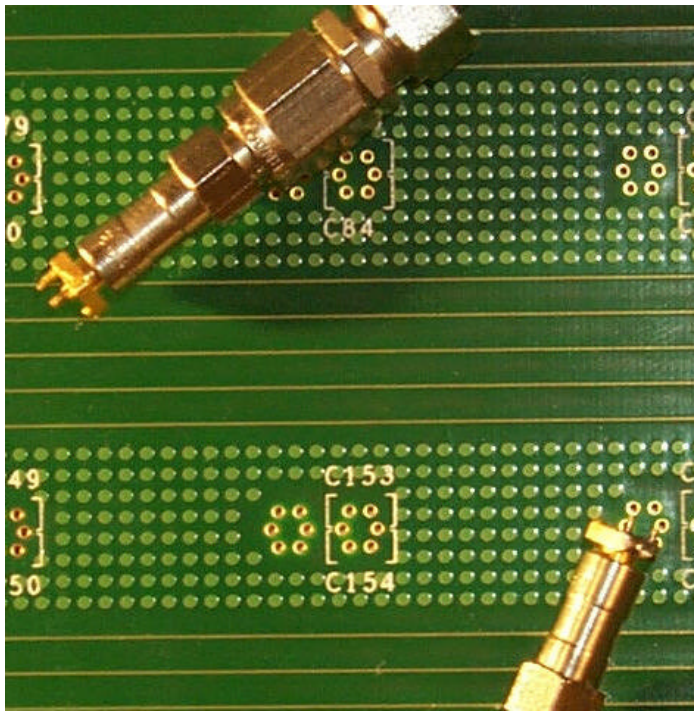

Figure 5.: SSMBC probes with the test board details.

Impedance profile measurement results on bare boards

With the instrumentation shown above, the three kinds of test boards were measured at the test points shown in Figure 3. Test points 1, 17, 33, 149, 165 and 305 were used to measure self-impedance profiles as a function of frequency; the other test points were used for transfer impedance measurements.

Figure 6 and 7 show the measured self-impedance of the unplug plane pair at one of the corners (test point #1) and the transfer impedances from the corner to the center of board (test points 1 to 165). The impedance measurements were made with a bandwidth of 100Hz, with no spectrum averaging. Up to the lowest resonance frequency, all test boards impedances follow the impedance of static capacitance. Having the same board area for all three boards, the static capacitance depends on the ratio of relative dielectric constant to plane separation: ε_r/s. The lowest impedance is achieved with the 1.6-mil HiK laminate, the second higher is the 1-mil polyimide, the highest is the 3.6-mil polyimide.

Beyond the lowest resonance frequency, the self-impedance profiles rise with increasing frequency, and they exhibit multiple resonances. Clearly the 3.6-mil polyimide has the highest self-impedance at the upper end of the spectrum, but the 1-mil polyimide and 1.6-mil HiK laminates show about the same impedance values. In the transfer impedance profile the HiK material shows more high-frequency attenuation, which could be due to its higher dielectric loss. Note that for power-distribution purposes, higher loss tangent of the dielectric material is more beneficial, as long as the same dielectric is not used for high-speed signal layers as well.

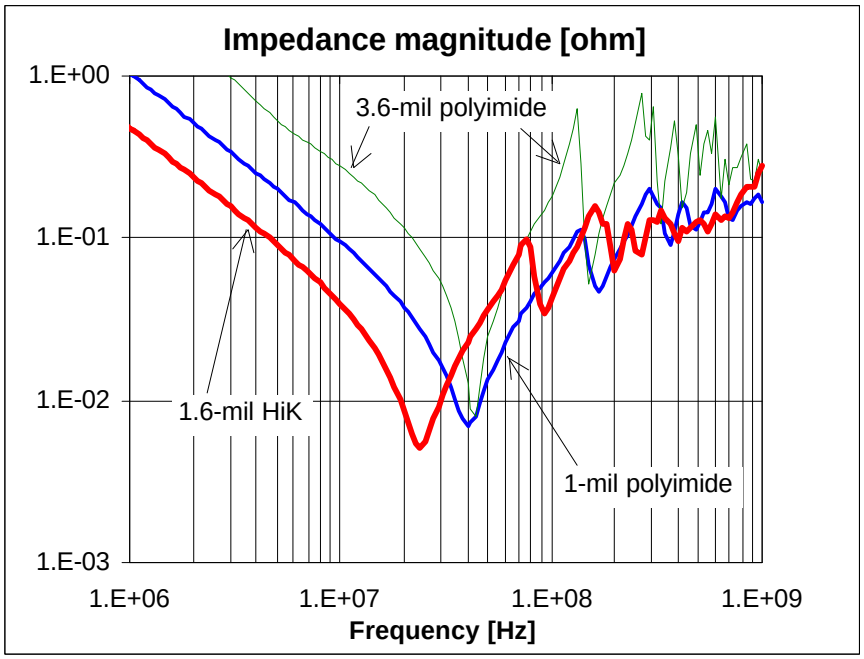

Figure 6.: Self-impedance of test boards measured at the corner. The thinnest line shows the 3.6 mils polyimide, the medium line refers to 1-mil polyimide, and the heaviest line shows the 1.6-mil HiK material.

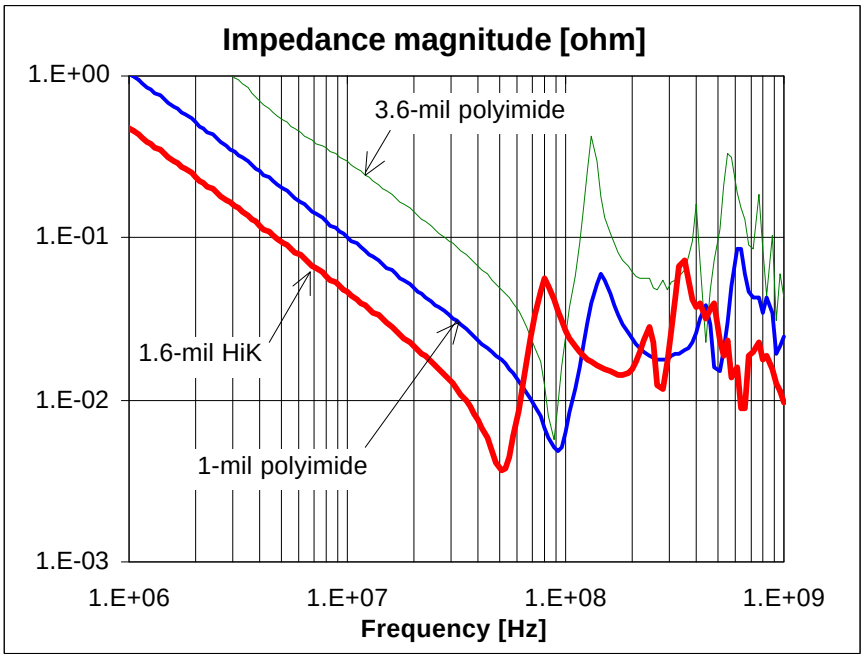

Figure 7.: Transfer impedance of test boards measured from the corner to the center. The thinnest line shows the 3.6 mils polyimide, the medium line refers to 1-mil polyimide, and the heaviest line shows the 1.6-mil HiK material.

Close and far-field radiation

The bare test boards were measured for close-field and far-field radiations as well. The close-field radiation setup used a Hewlett-Packard P4396 VNA with a low-noise preamplifier and a 1-cm EMKO close-field loop. Port 1 of the VNA was used to excite the test board at the selected location, whereas the close-field loop was positioned along the edge of the board, as shown in Figure 8.

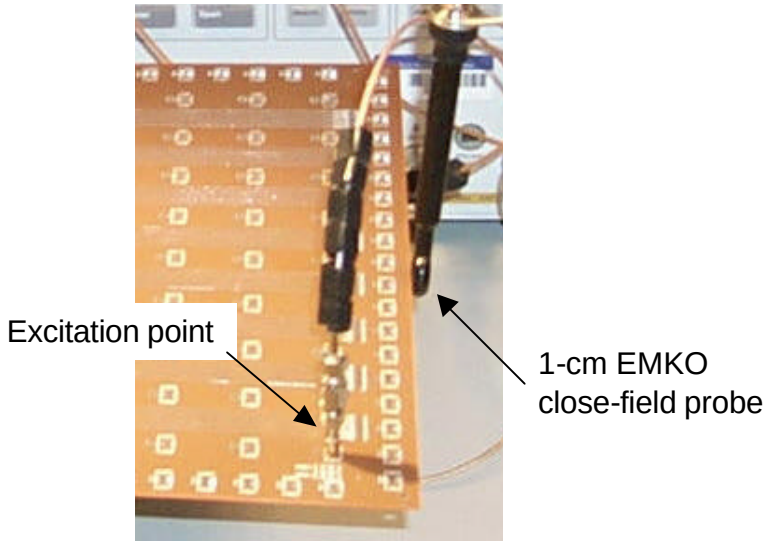

Figure 8.: Measurement setup for close-field radiation. The excitation point is at test point #1, the close-field probe is next to test point #149.

The relative close-field radiation magnitudes are shown in Figure 9. Note that consistently with the impedance curves, the 3.6-mil polyimide laminate is the worst; it exhibits the highest level of close-field radiation. The second best is the 1.6-mil HiK laminate, and the lowest radiation was measured from the 1-mil polyimide construction.

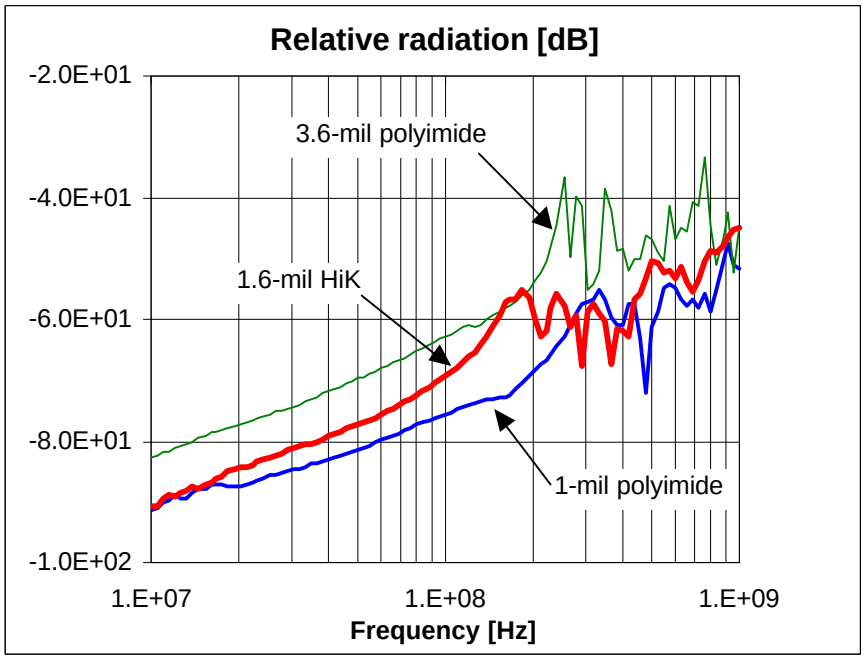

Figure 9.: Close-field radiation at test point #149. The thinnest line shows the 3.6 mils polyimide, the medium line refers to 1-mil polyimide, and the heaviest line shows the 1.6-mil HiK material.

Far-field measurements were conducted in an anechoic chamber at a distance of 3 meters from the DUT. Some of the results of the far-field measurements have been published in [10].

Measurement and simulation correlations on bare-board impedances

There are several options to simulate the electrical performance of power-ground plane pairs. One attractive solution is to use a SPICE equivalent circuit to describe the structure, since it can be conveniently integrated into further system analysis. The correlations shown below were performed with a simulation method similar to the one described in [9]. The self and transfer impedances of various structures with and without additional components on the board surface were computed and measured over the frequency range of 0.001 – 5,000 MHz. It was found that to achieve good agreement between simulated and measured data, the simulation grid must have a fine grid. In case of the results shown here, the grid segments were set to 1/50 of the wavelength of the highest frequency of interest. This is primarily required to achieve good correlation at the modal resonance dips. Fig. 10 shows the correlation of impedance profile on a test board of size 10”x5”. The test board contained two pairs of 2-mil FR4 cores connected in parallel be a set of plated through holes. Note the excellent agreement of both the minimum and maximum frequencies and including the magnitudes at the first minimum and maximum. The simulation grid was 0.25”.

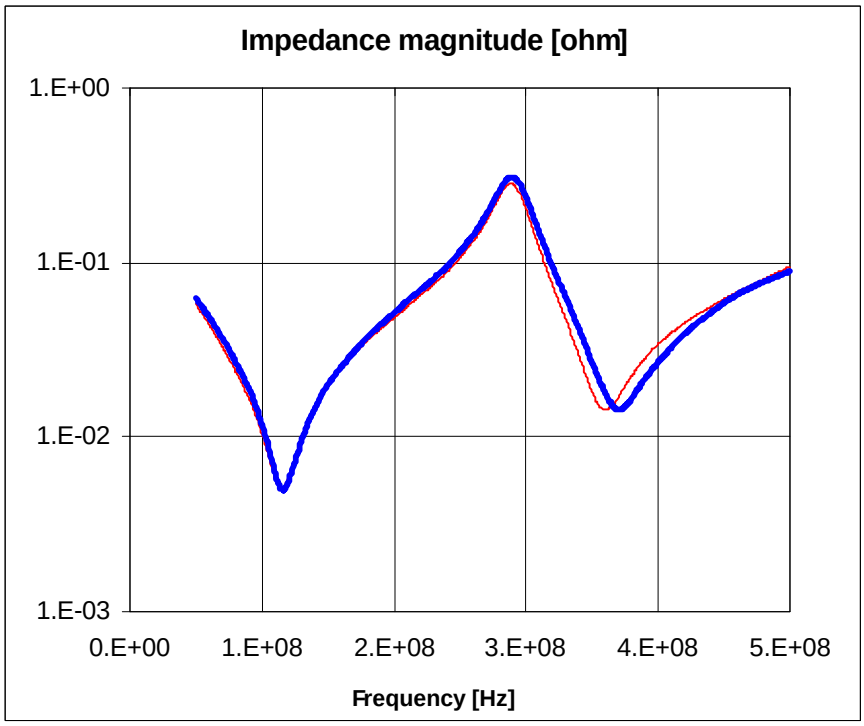

Fig. 10.: Measured (solid heavy line) and simulated (solid thin line) self-impedance of two pairs of paralleled 2-mil FR4 cores of 10”x5” size. The self-impedance was measured and simulated at one of the corners.

Conclusions

It has been shown that higher dielectric constant reduces the impedance of power-ground plane pairs at lower frequencies, but at high frequencies the self-impedance and close-field radiation profiles are dictated primarily by the separation of planes.

Acknowledgements:

The author wishes to thank Valerie St.Cyr and Ken Weiss for their help in creating the test boards, for Dan Irish, and Paul Boudreau for their assistance in making the radiation measurements.

References:

[1] ZBC 2000 datasheet at: http://www.hadco.com/products.htm
[2] US patents no. 5,079,069, 5,261,153, 5,870,274
[3] http://www.dupont.com/fcm/html/pyralux_lf.html
[4] NEMI roadmap: http://www.dupont.com/mcm/whatsnew/nemi_41.pdf
[5] EM-Cap material description: http://www.hadco.com/prod03.htm
[6] Edward J. Reardon, Richard W. Carpenter, "Novel Thin Film Materials and Processes for Integral (Embedded) Resistors and Capacitors," 8th Circuit World Convention, September 10, 1999, Tokyo, Japan.
[7] Richard Charbonneau, "An Overview of the NCMS Embedded Capacitance Project," NCMS Embedded Capacitance Conference, Tempe, AZ, February 28-29, 2000.
[8] Larry Smith, "Concepts of Selecting Capacitance Values in High-Performance Applications," NCMS Embedded Capacitance Conference, Tempe, AZ, February 28-29, 2000.
[8] I. Novak, "Measuring Milliohms and PicoHenrys in Power Distribution Networks," paper H411at DesignCon2000, Santa Clara, CA, February 1-4, 2000.
[9] Larry Smith, Tanmoy Roy, Raymond Anderson, "Power Plane SPICE Models for Frequency and Time Domains," 9th Topical Meeting on the Electrical Performance of Electronic Packaging, October 23-25, 2000, Scottsdale, AZ.
[10] Syed A. Bokhari, Istvan Novak, "Effect of Dissipative Edge Terminations on the Radiation of Power/Ground Planes," Proceedings of the IEEE EMC Symposium, August 21-25, 2000, Washington, D.C.