Reducing EMI Noise by Suppressing Power-Distribution Resonances

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Outline

- Introduction: revisiting the definition of EMI
- Possible resonances in PDN
- Suppressing resonances
- Conclusions

Introduction
SI, PI, EMI

In traditional view, the three disciplines are applied independently

- SI: 1D wave propagation effects
  - Reflections, termination, crosstalk
- PI: 2D and 2.5D wave propagation effects
  - Plane resonances, SSN due to via inductance
- EMI: 3D wave propagation effects
  - EM interaction through distance (out-of system source)

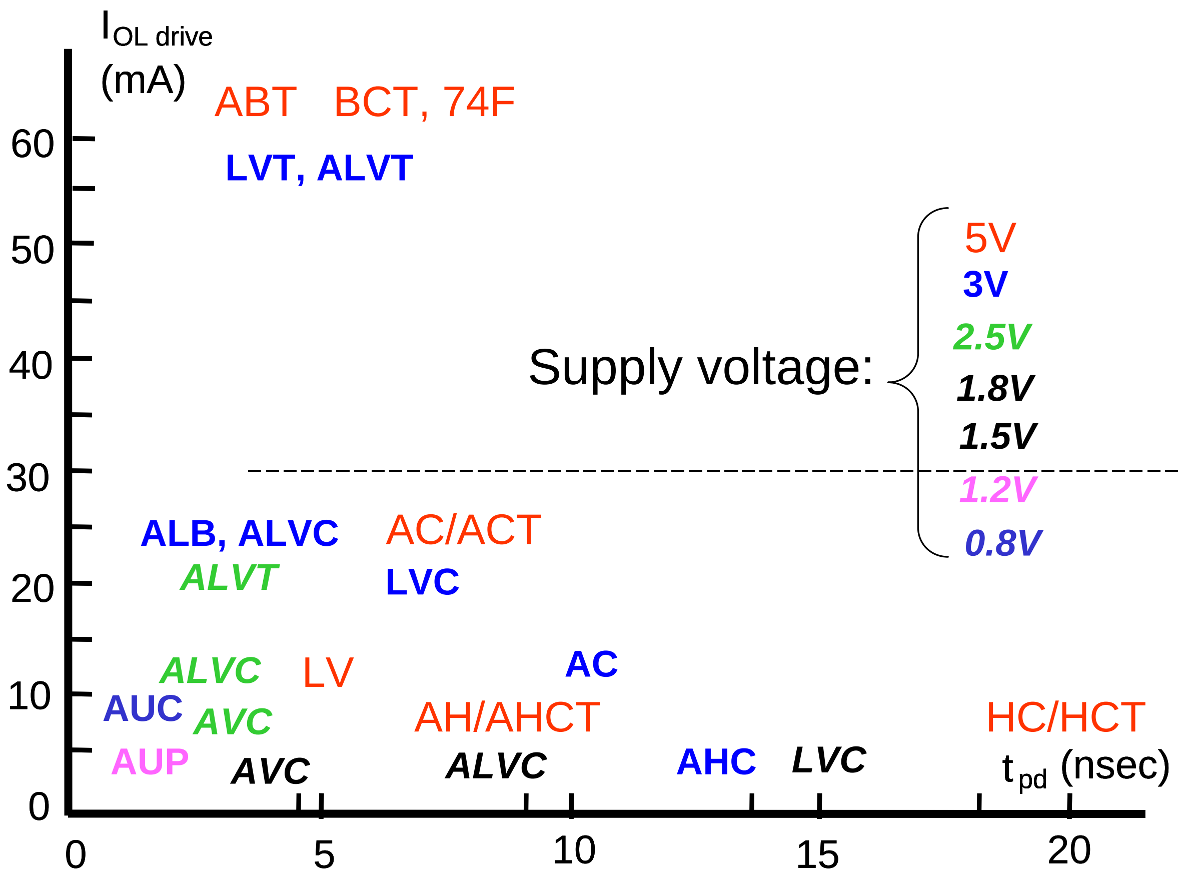
Introduction
SI, PI, EMI revisited

More and more the interactions cant be ignored

- SI>EMI: Resonances on no-care signals may create EMI problems
- *PI>EMI: Resonances on power distribution increase radiation*
- PI>SI: Resonances on power distribution increase jitter and BER
- *EMI>SI: conducted and radiated noise from in-system modules reduce BER*

In-system EMI is becoming an increasing problem

Trends in Power Distribution Design



- Clock frequencies rise

>> BW goes up

- Supply voltages drop

>>more domains

>>tighter tolerances

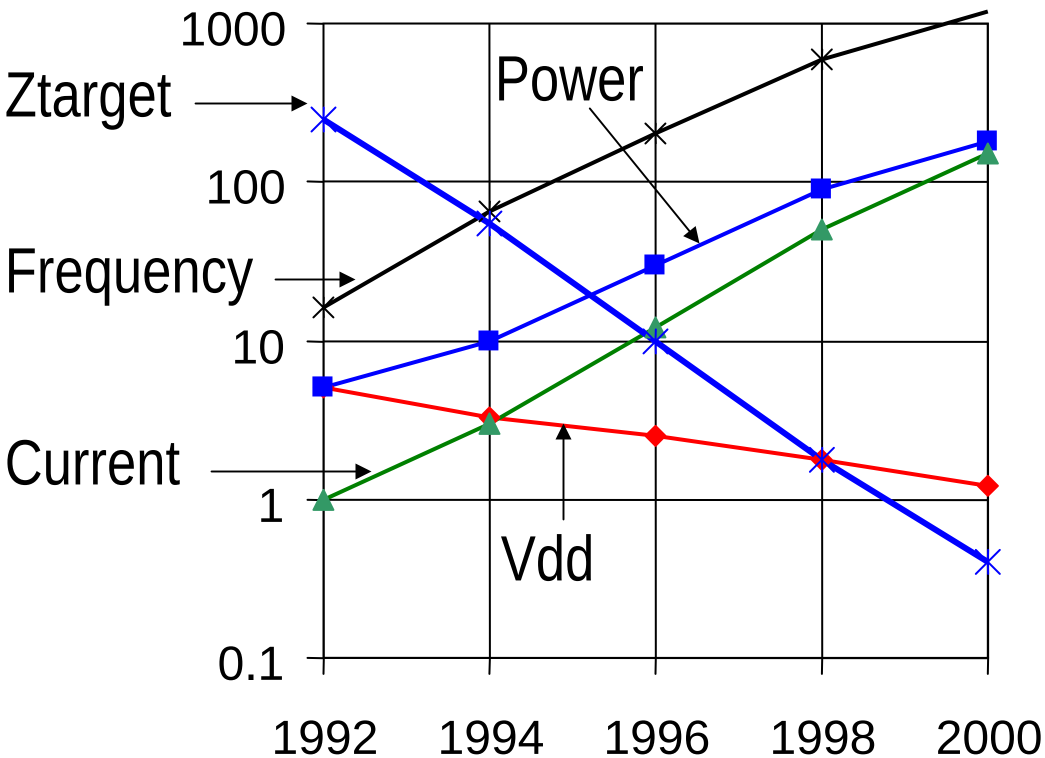
>>higher currents

>>lower PDN impedance

Source: Texas Instruments Logic Selection Guide, 2006; SDYU001Y
http://www.ti.com

Trends in PDN Requirements

Target impedance predicted in early 1998



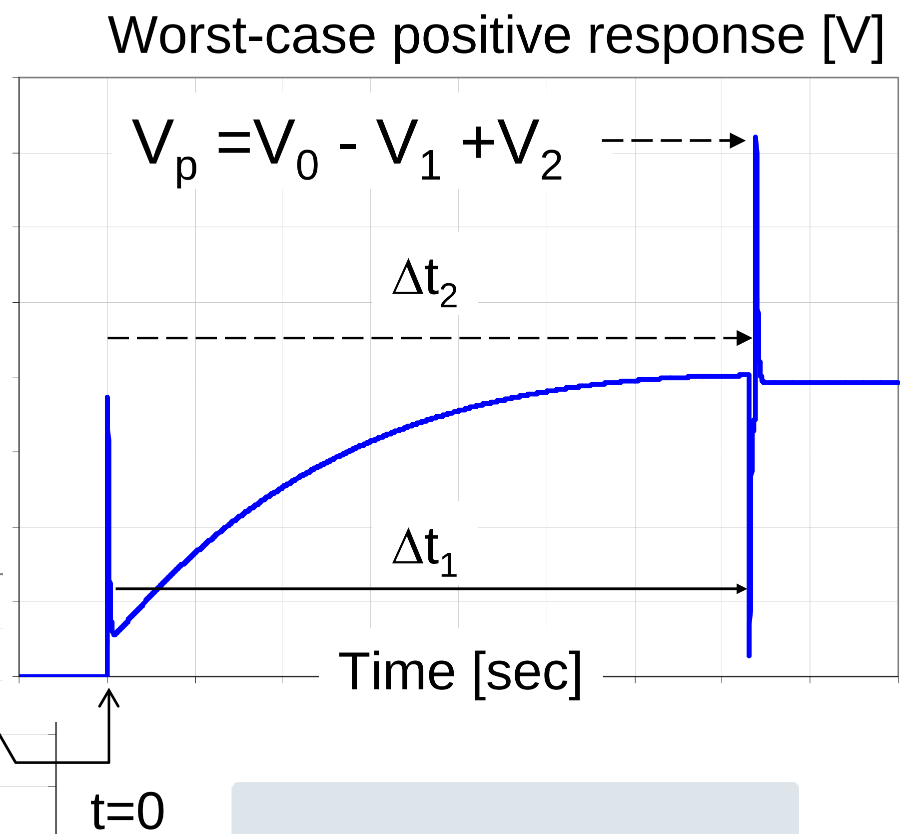
Larry Smith, “Power Distribution for High Performance Systems,” Conference Class 4, EPEP98, West Point, NY, October 26-28, 1998

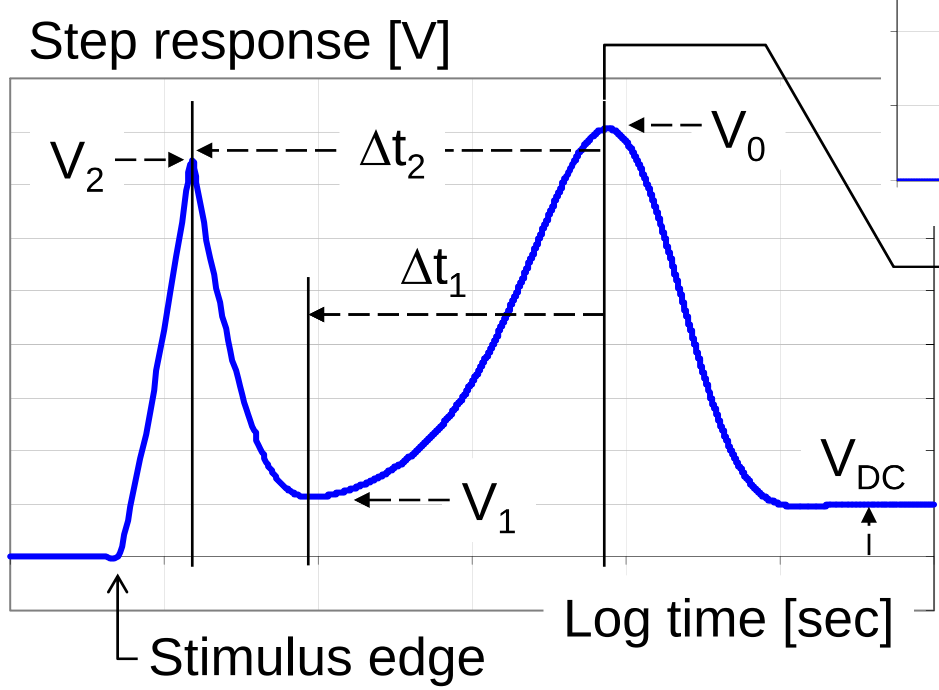
PDN Trends

- Increasing number of independent supply rails (less room for planes and PDN components)
- Increasing system density (noise sources and sensitive circuits are closer). Note: scaling.
- Higher efficiency (lower losses create more high-frequency noise)
- Size and cost constraints (resonances may not be sufficiently suppressed)

PDN Design Process

Worst-case PDN noise calculation





Worst-case peak-to-peak transient:

Vpp = 2*Vp - VDC

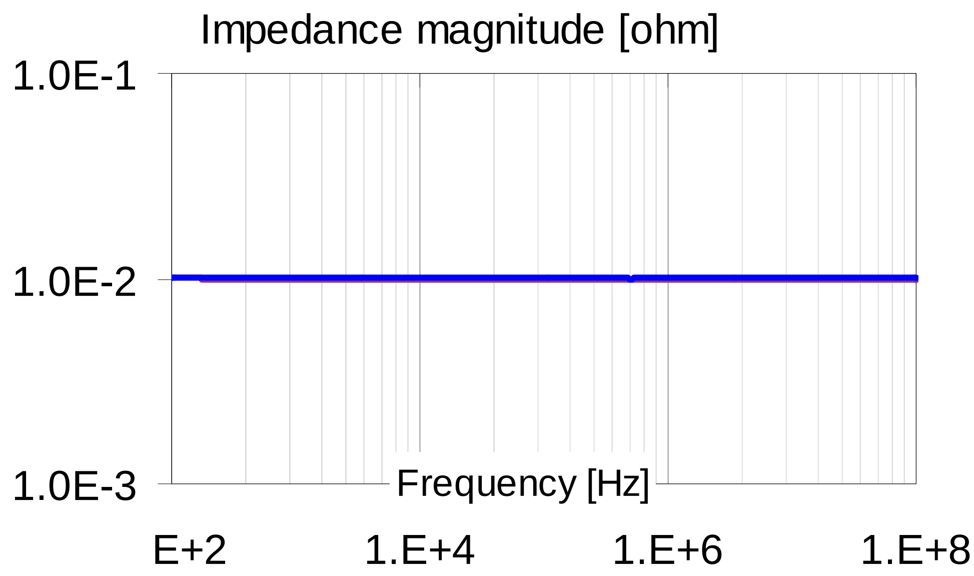
Drabkin, et al, "Aperiodic Resonant Excitation of Microprocessor power Distribution Systems and the Reverse Pulse Technique," Proc. of EPEP 2002, p. 175

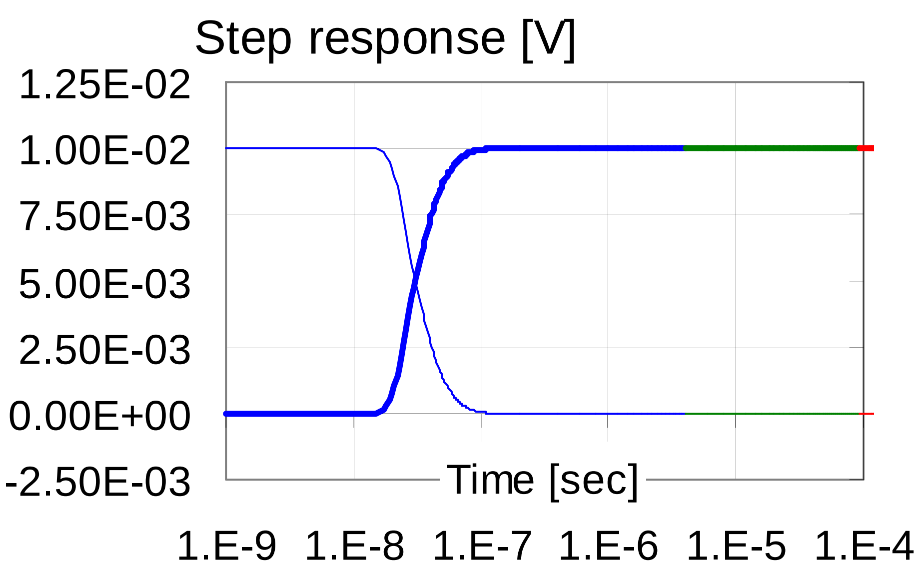
PDN Design (1)

Ideal response

Worst-case peak-to-peak transient:

10mVpp/A





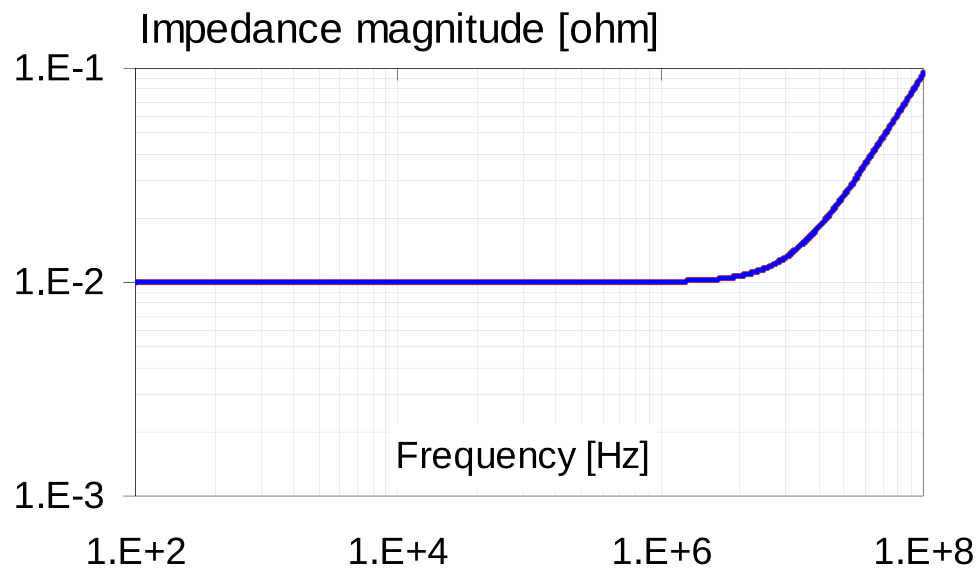
	C [uF]	ESR [ohm]	L [nH]
R	-	0.01	-

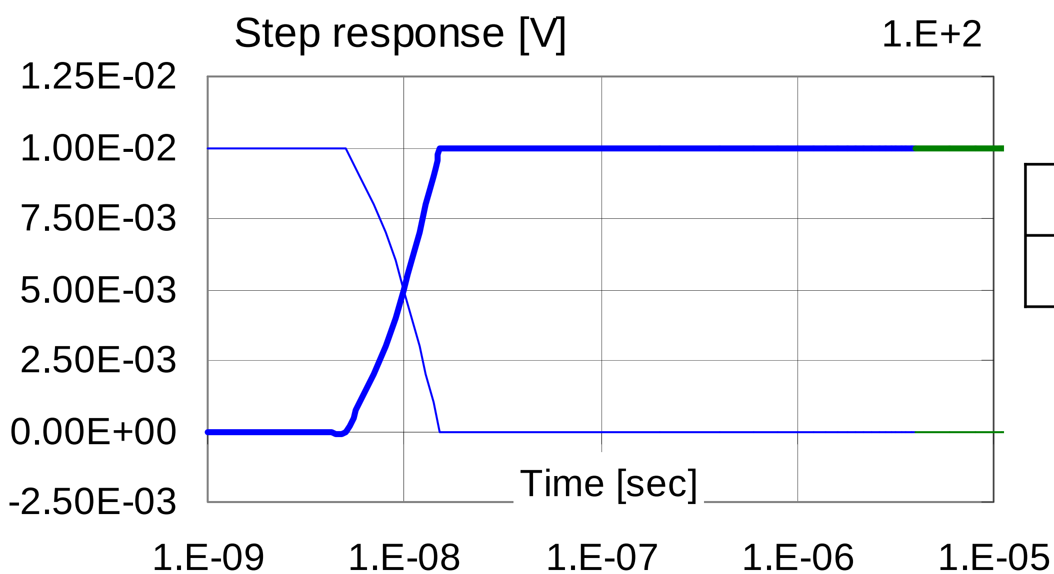
PDN Design (2)

The practical best: R-L

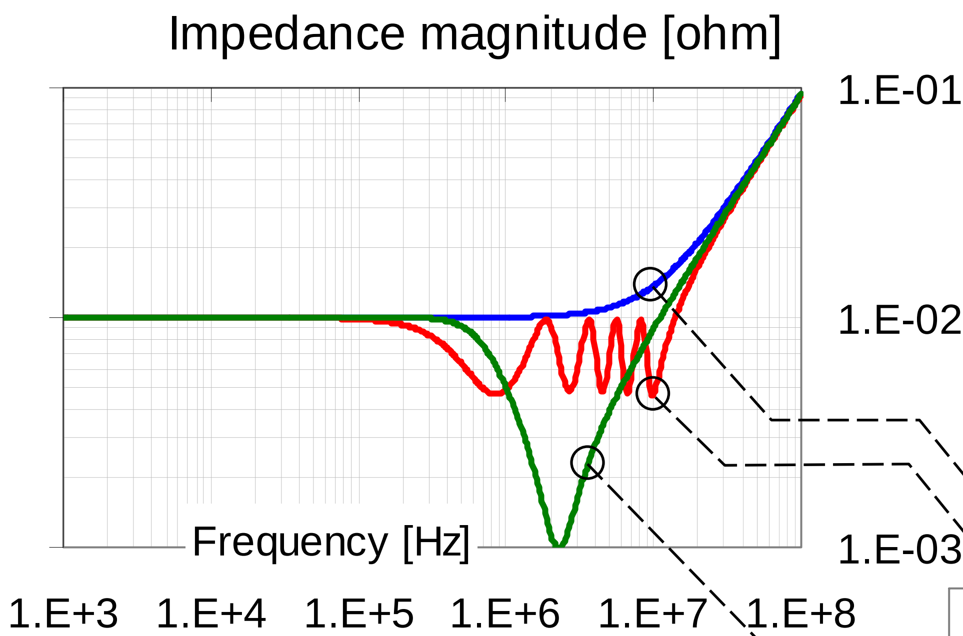
Worst-case peak-to-peak transient:

10mVpp/A



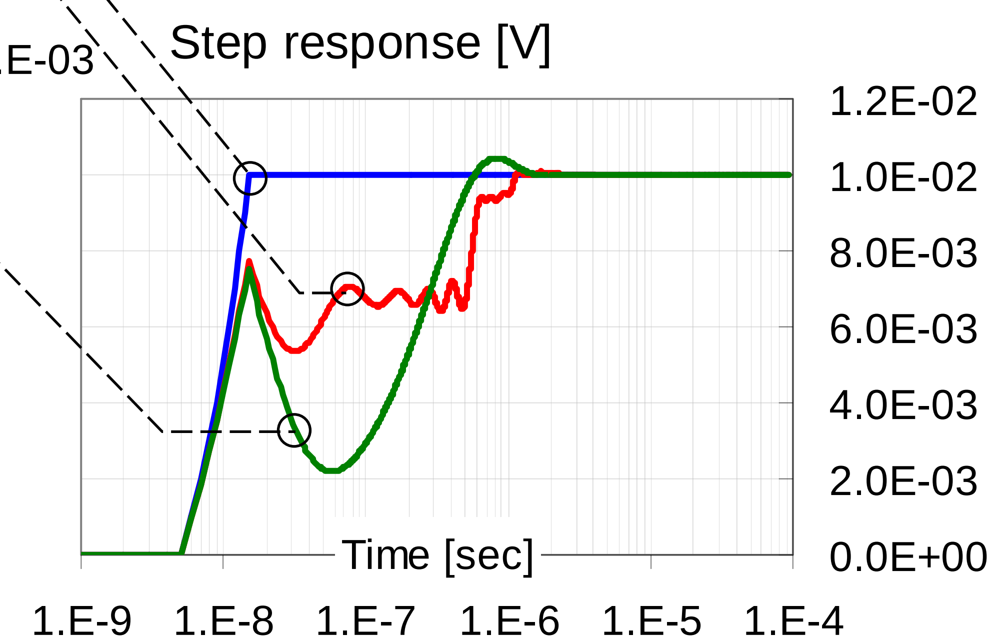


	C [uF]	ESR [ohm]	L [nH]
R-L	-	0.01	0.15



PDN Design (3)

PDN comparison with voltage positioning



Worst-case peak-to-peak transient:

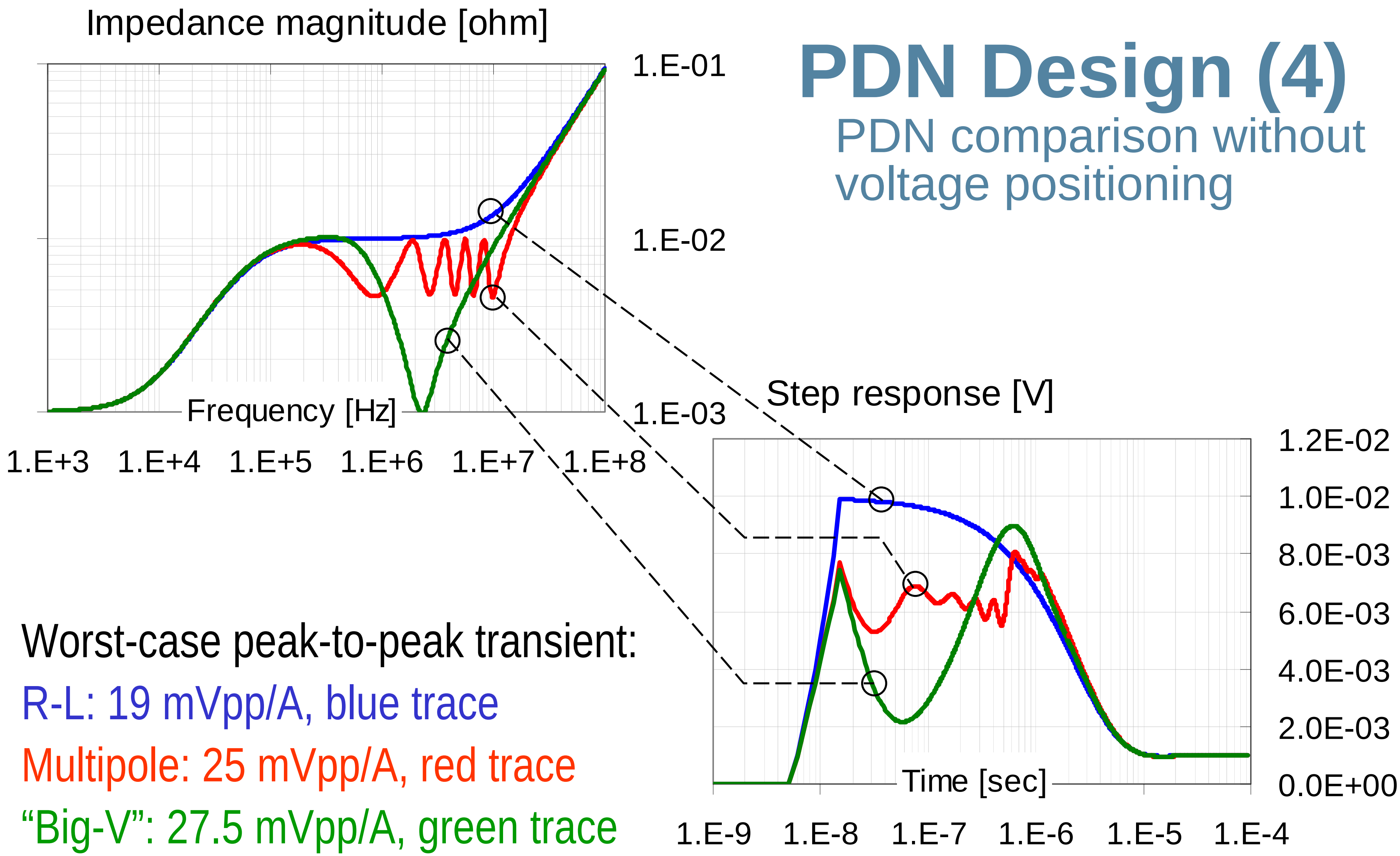
R-L: 10 mVpp/A, blue trace

Multipole: 15.7 mVpp/A, red trace

“Big-V”: 21.4 mVpp/A, green trace

PDN Design (4)

PDN comparison without voltage positioning



Worst-case peak-to-peak transient:

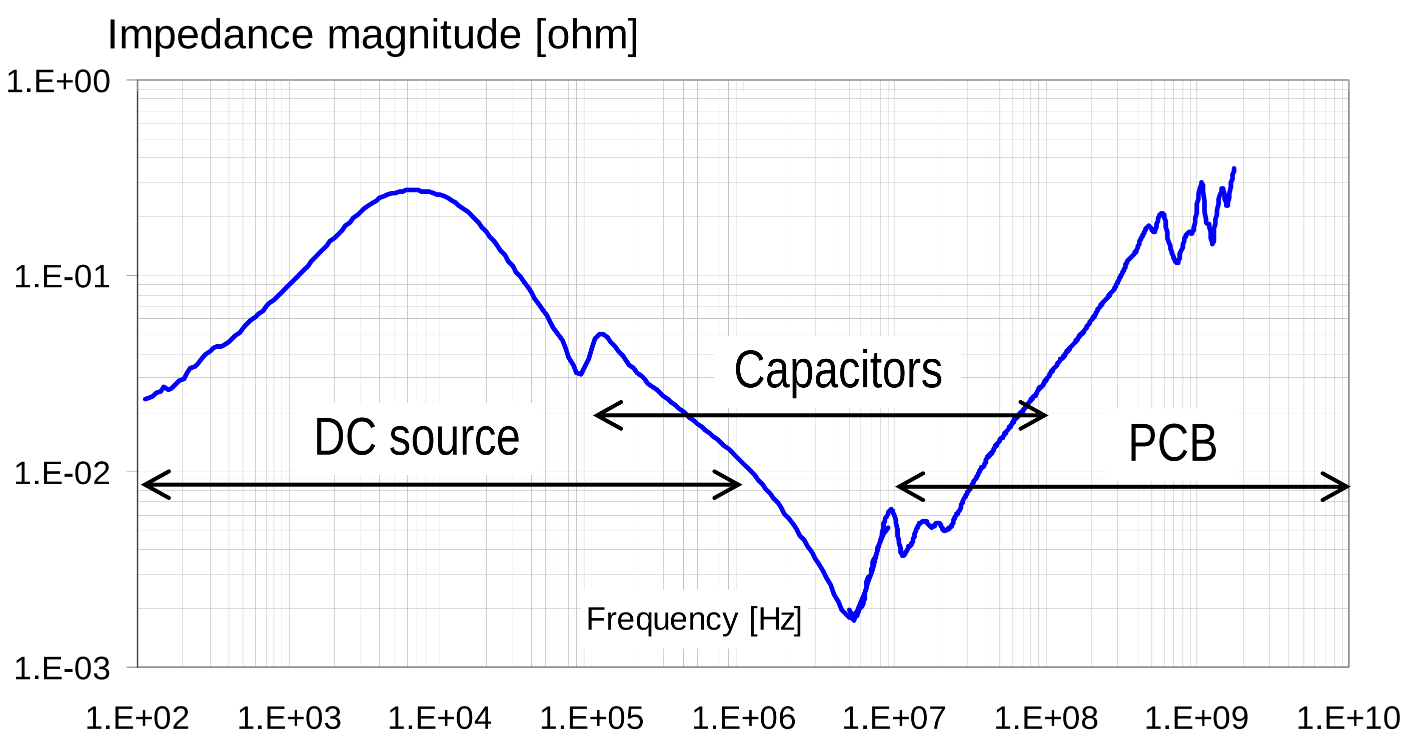
R-L: 19 mVpp/A, blue trace

Multipole: 25 mVpp/A, red trace

“Big-V”: 27.5 mVpp/A, green trace

PDN in the Frequency Domain

- DC sources: low frequency
- Bypass capacitors: mid frequency
- PDN planes, board and chassis features: high frequency

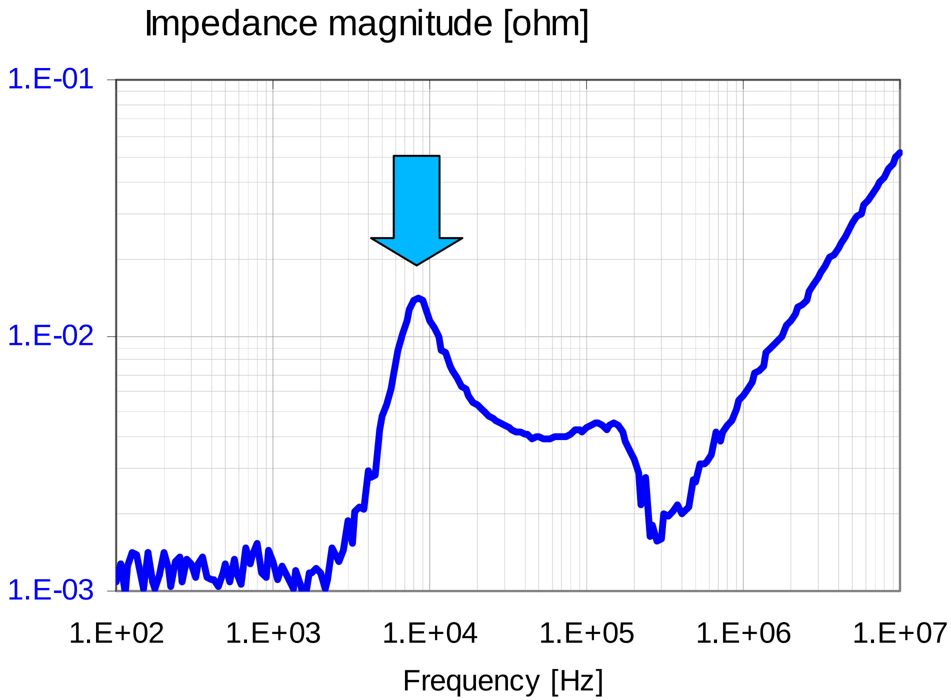


Potential PDN Resonances

- DC sources
  - Peaking due to improper loop design
  - High-frequency ringing due to switch parasitics
- Peaking between DC source and bulk capacitors
- Peaking between capacitor banks
- Peaking between capacitors and planes
- Structural resonances of PDN planes
- Structural resonances of boxes, enclosures

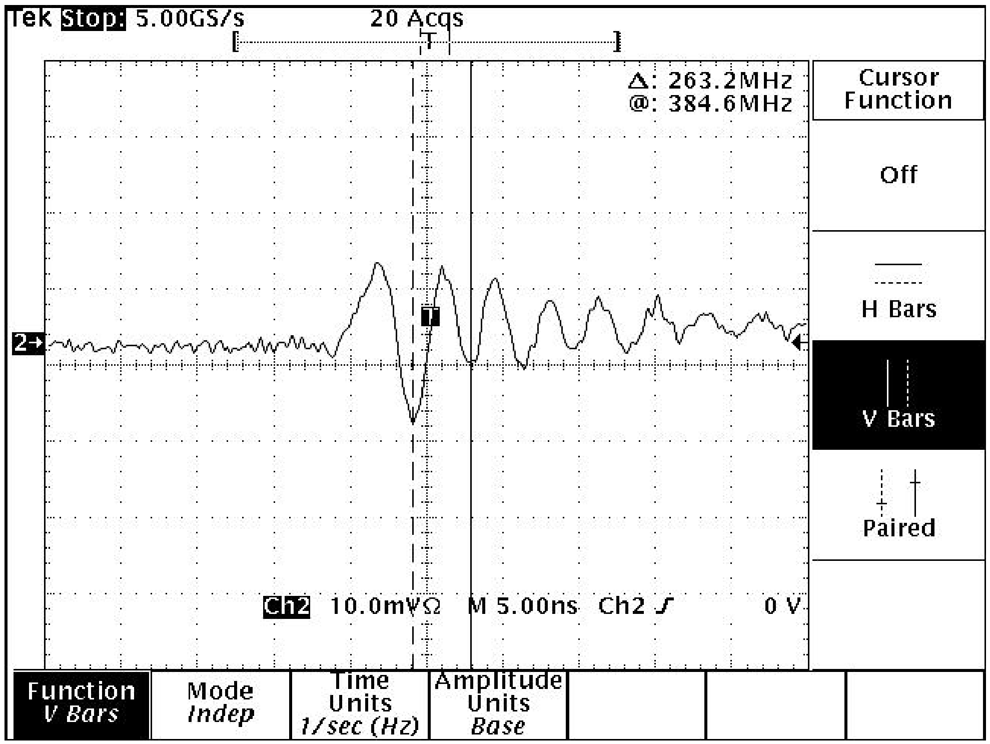
DC-source Resonance due to Loop

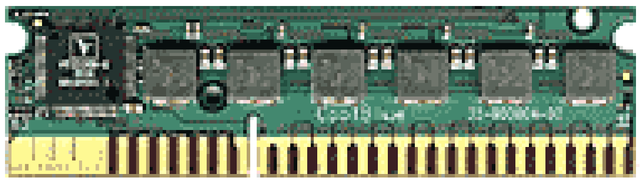
- Typical switching frequency is in the 0.1-1MHz range
- Typical loop peaking is in the tens of kHz range
- No EMI concern, primarily a PI issue



Converter Ringing

- Typical ringing frequency is in the 50 – 500 MHz range
- High-current converters may switch 100+ A
- Sensitive clock signals run on a few mA
- 80+ dB ratio
- *EMI and SI risk*

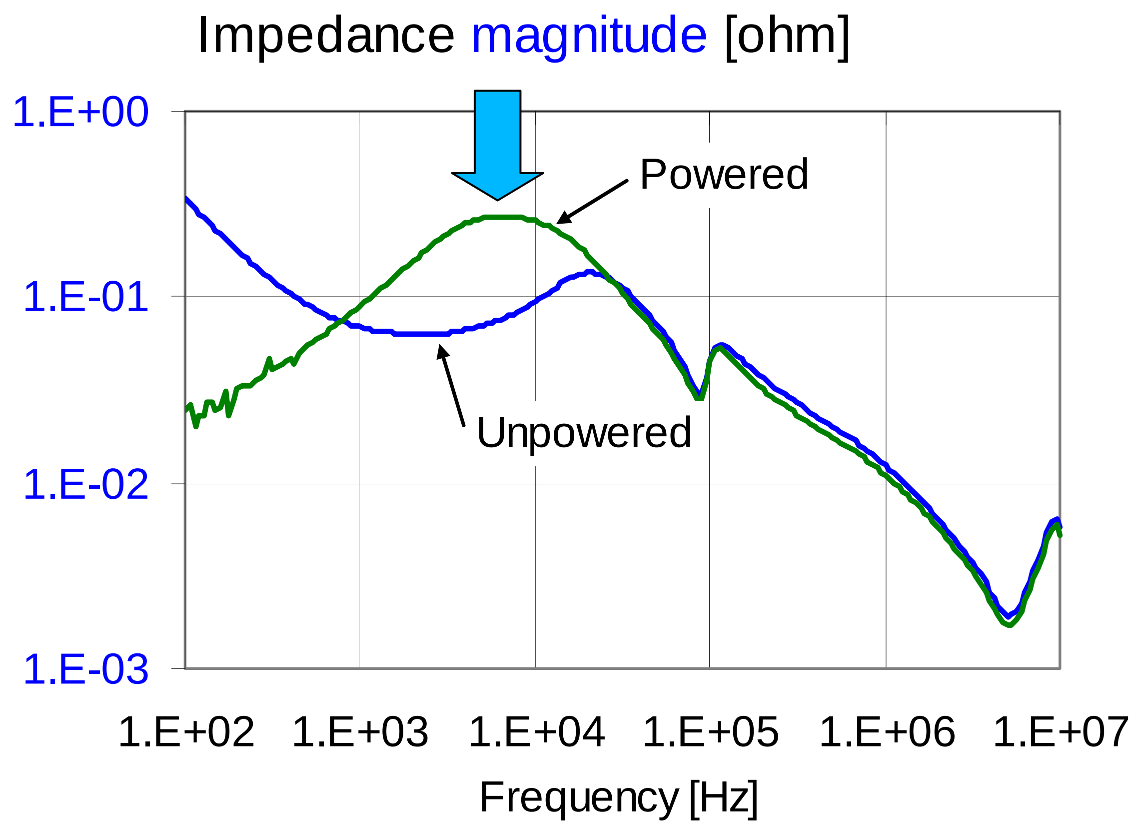




100A @ $1.3V_{OUT}$

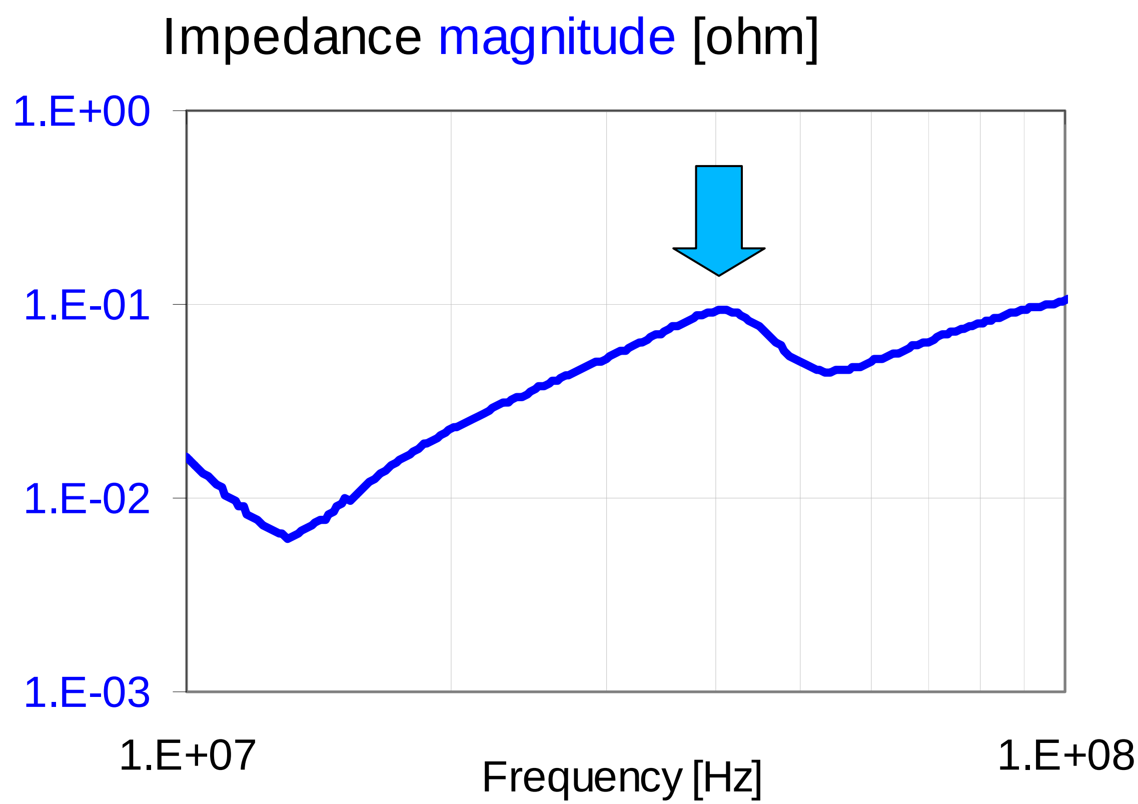
Peaking Between DC Source and Bulk

- Low-frequency peaking
- PI concern, no EMI risk



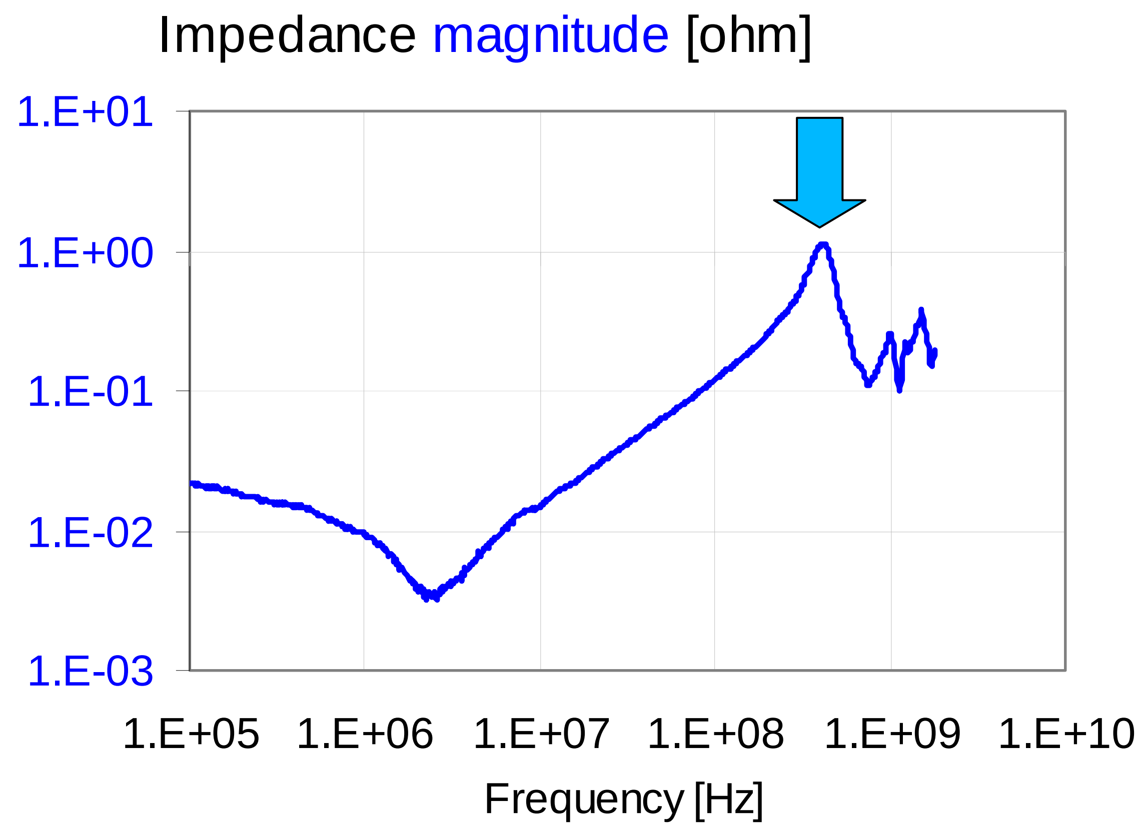
Peaking Between Capacitor Banks

- Low-frequency peaking
- PI concern, no EMI risk



Peaking Between Capacitors and Plane

- High-frequency peaking
- PI *and* EMI risk

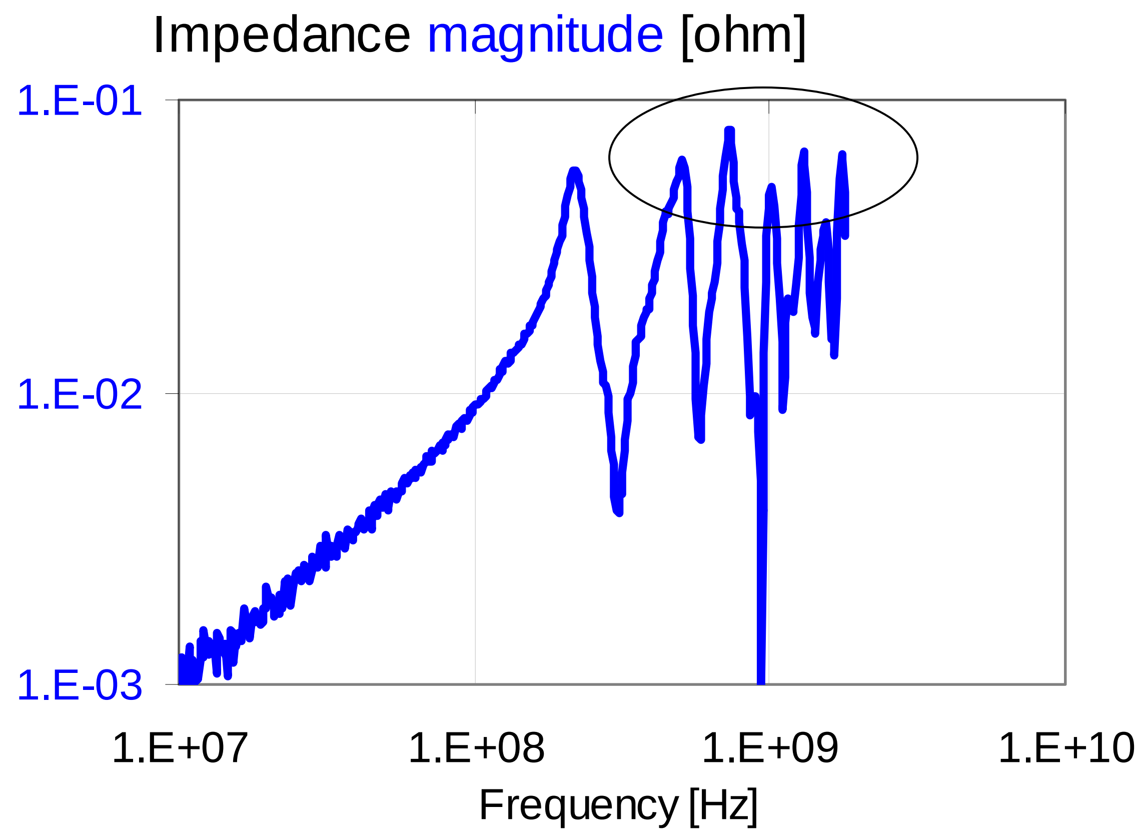


Peaking Between Capacitors and Plane: How to Solve

- Matched termination
- Area capacitors
- Hardest peaking to suppress

Structural Plane Resonances

- High-frequency peaking
- PI *and* EMI risk



Structural Plane Resonances: How to Solve

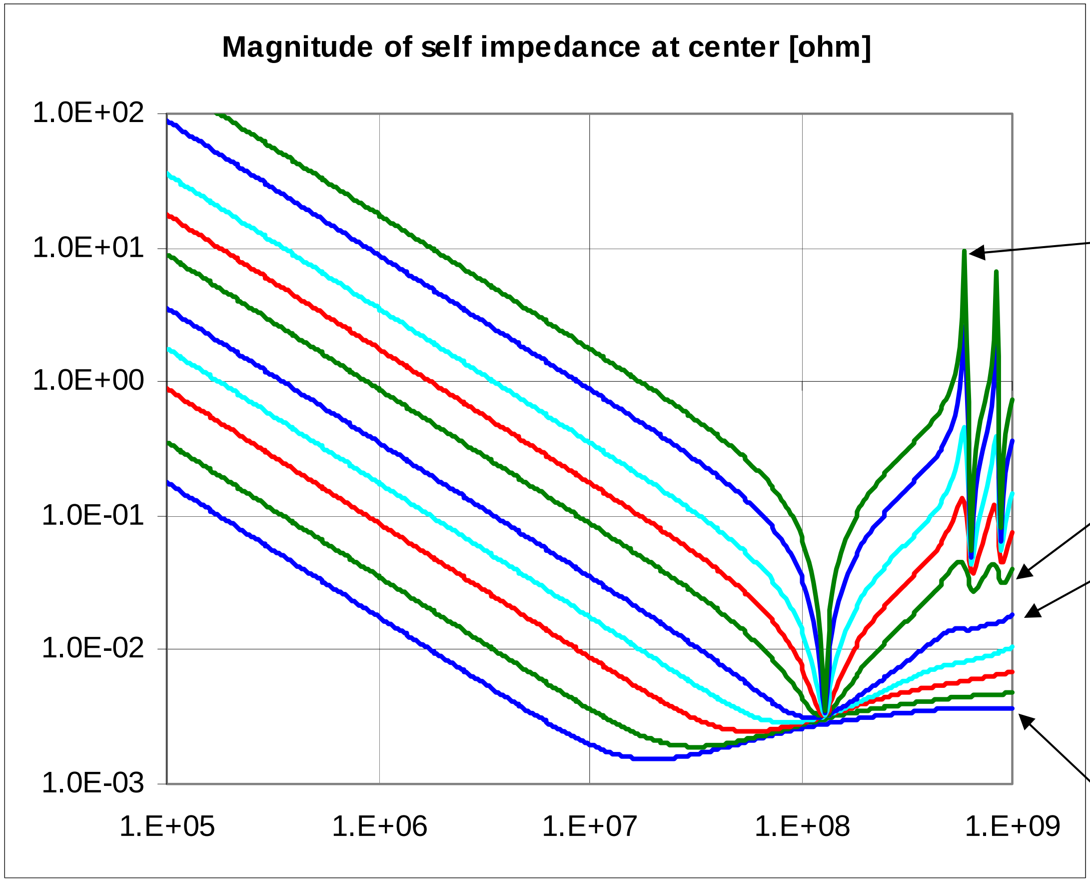
Options:

- Thin laminates
- Resistive termination
- Area capacitors

Structural Plane Resonances: Thin Laminates (Self-Z)

Thin laminates:

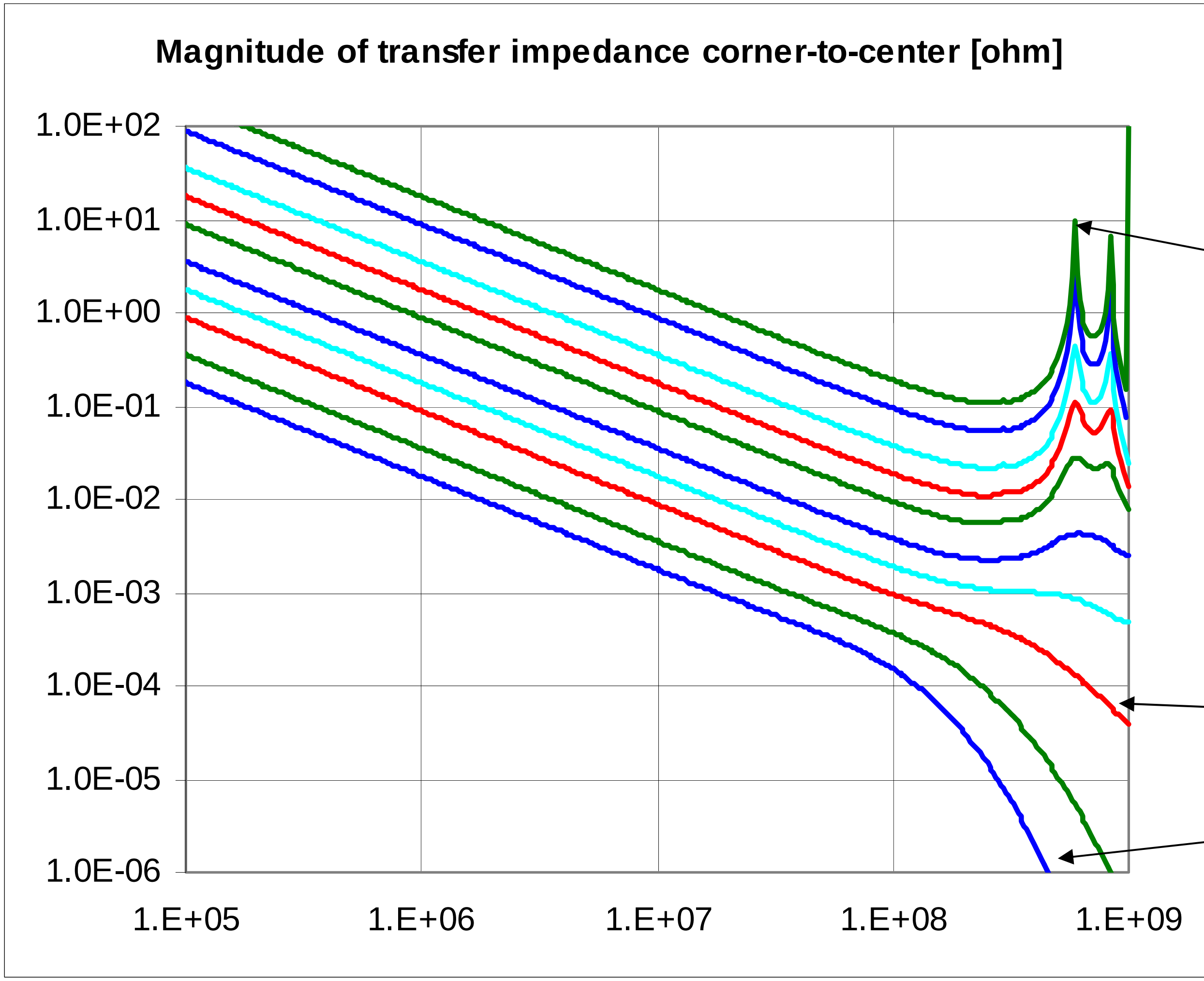
- Dampen structural resonances
- Make it harder to suppress plane-capacitor resonances



10”x10” planes
Bare board
Simulated, t =

- 10-mil
- 5-mil
- 2-mil
- 1-mil
- 0.5-mil
- 0.2-mil
- 0.1-mil
- 0.05-mil
- 0.02-mil
- 0.01-mil

Structural Plane Resonances: Thin Laminates (Transfer-Z)



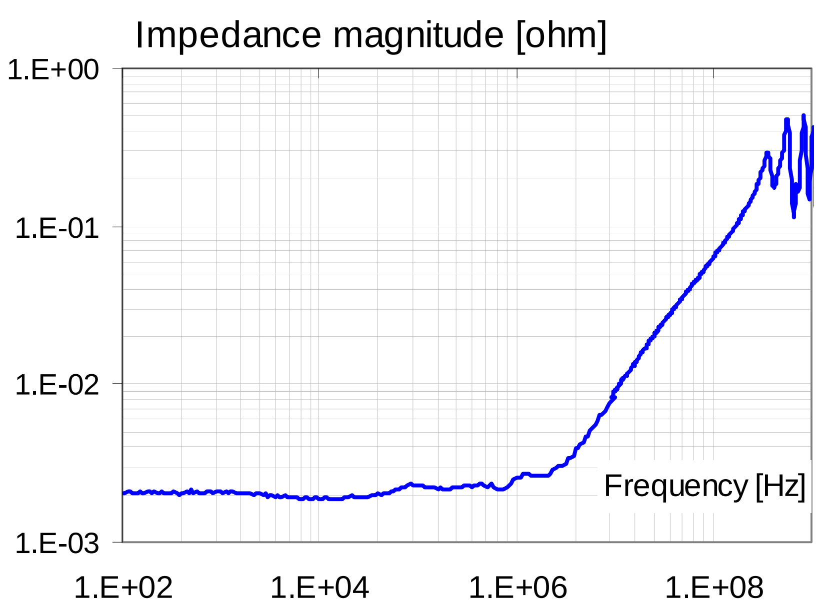
10”x10” planes
Bare board
Simulated, t=

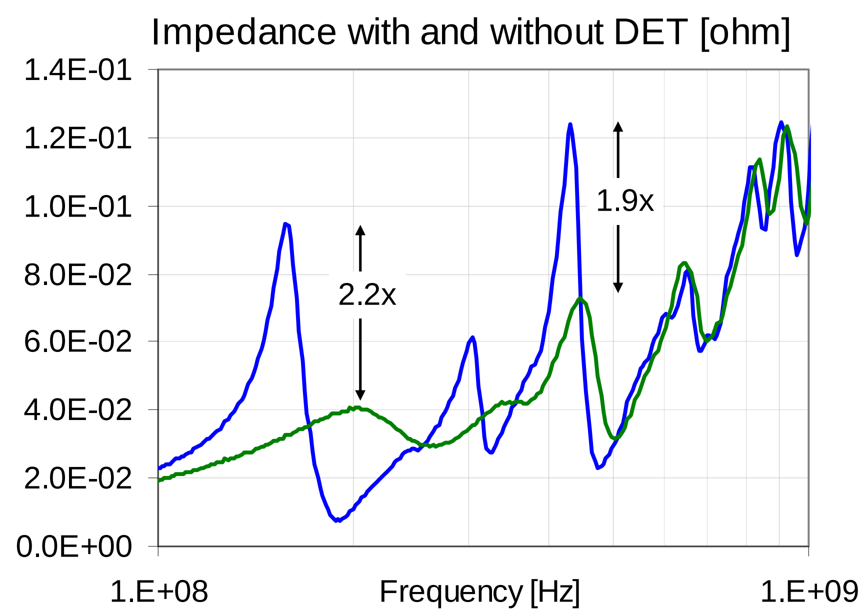
- 10-mil
- 5-mil
- 2-mil
- 1-mil
- 0.5-mil
- 0.2-mil
- 0.1-mil
- 0.05-mil (1.2um)
- 0.02-mil
- 0.01-mil

Structural Plane Resonances: Resistive Termination

Implementation options:

- Discrete R-C
- Embedded R
- Controlled-ESR capacitors

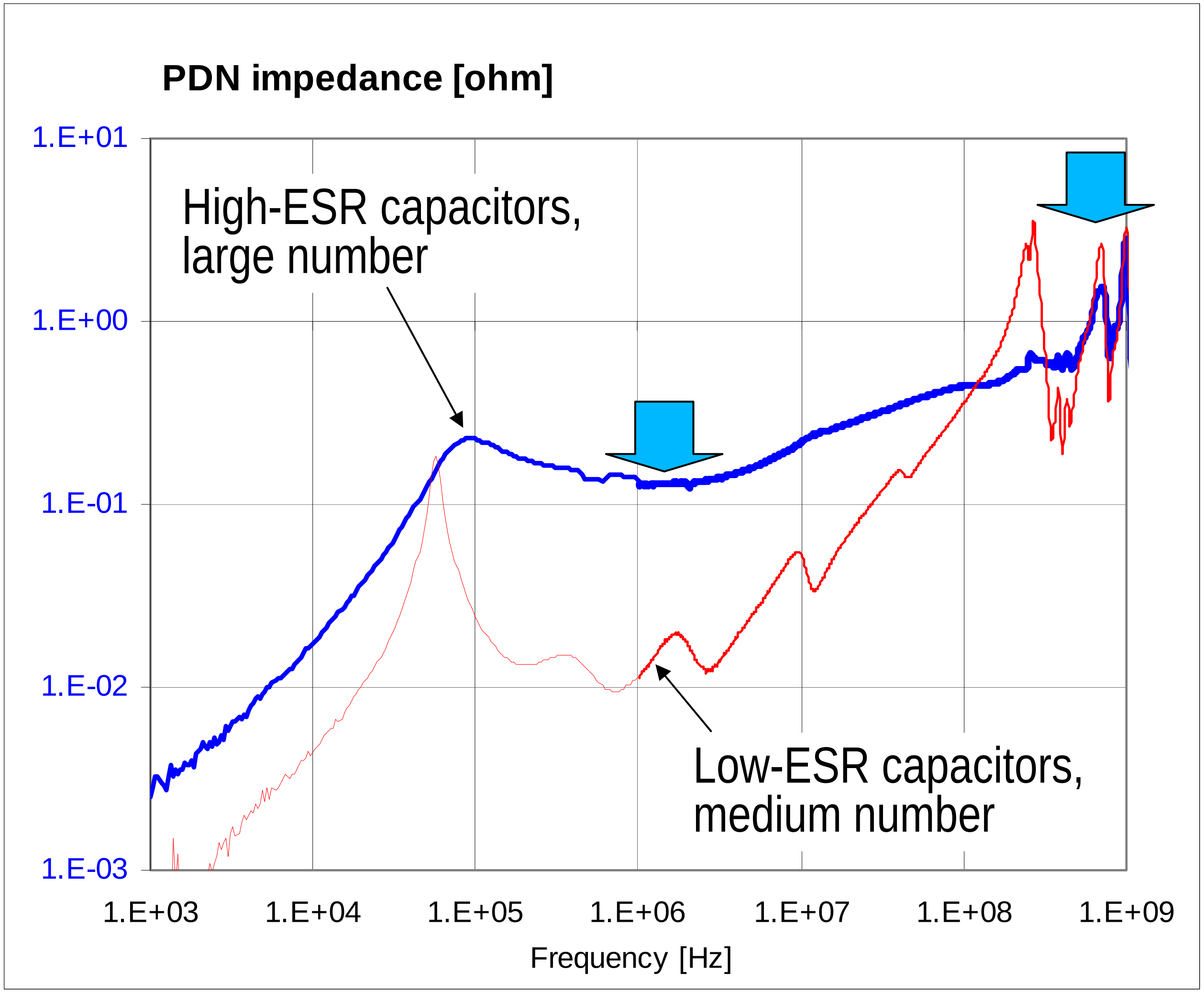




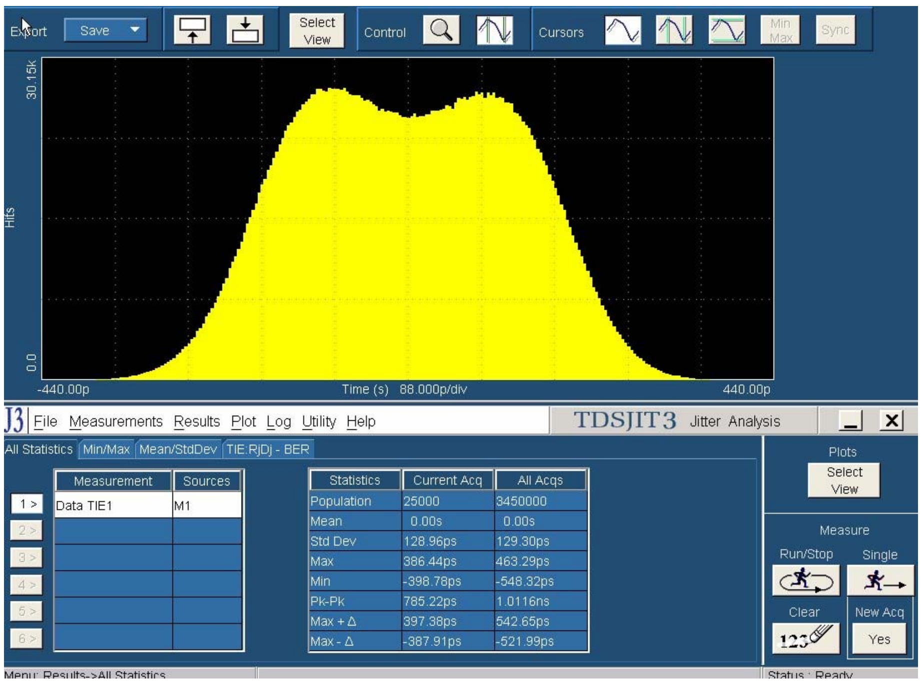
T2000 CPU module
High-current rail

Structural Plane Resonances: High-ESR and/or Area Capacitors

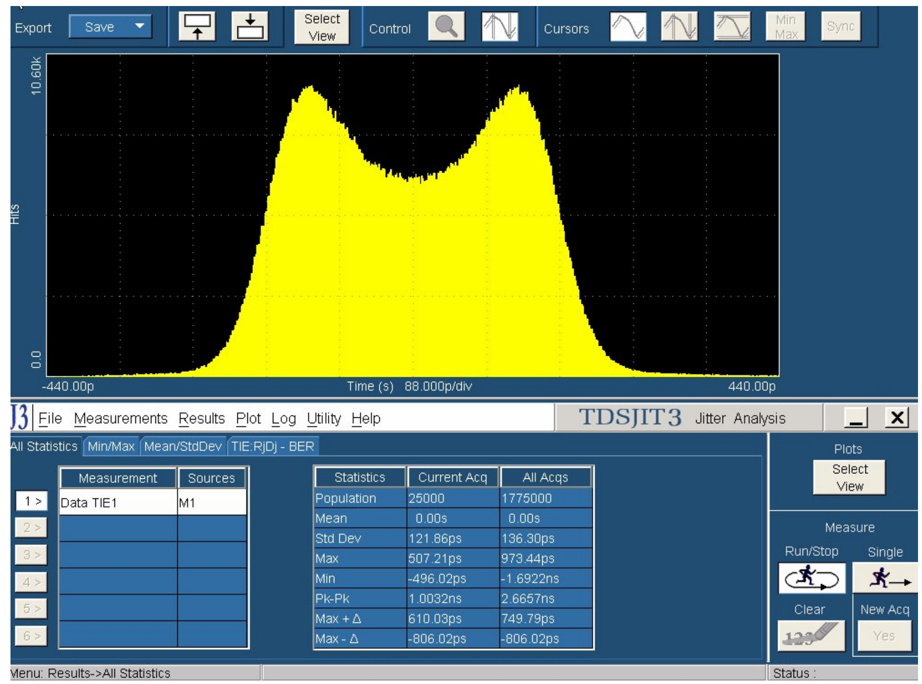
- Thin laminates require more capacitors
- Number of parts is proportional to plane area



EMI from AC-DC Source



With PSU #1



With PSU #2

Only the AC/DC power supply was changed

Conclusions

- High-frequency PDN resonances adversely affect EMI
- High-frequency PDN resonances may occur
  - Inside AC-DC and DC-DC converters
  - Between capacitors and planes
  - In PCB structures
  - In board and chassis features
- Best defence
  - Not to excite resonances ($F_{source} < F_{resonances}$)
  - Minimise loop sizes and coupling areas
  - Suppress resonances by impedance matching
  - Suppress resonances with area capacitors

THANK YOU

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