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Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination

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Abstract:
Power and ground planes are required to have low impedance over a wide range of frequencies. Parallel ground and power planes in multilayer printed-circuit boards exhibit multiple resonances, which increase the impedance and also the radiation from the edge of the board. Resistive termination along the board edges reduces the resonance peaks. Simple and straightforward design expressions, simulated self and transfer impedances, as well as measured impedance plots are presented for power-ground planes.

Index terms: Computer system design, Simultaneous switching noise, Decoupling capacitors, Power-ground planes, Resonance, Simulation, Impedance measurement, Impedance matching

I. Introduction

For many years of digital electronic designs, a +5V supply voltage for TTL and CMOS logic, and /or a -5.2V supply for an ECL logic was common. With the constant need to decrease power dissipation by reducing supply voltage, and due to submicron silicon feature sizes, which limits the breakdown voltage of the silicon at below 5V both in the core and in the I/O area, the supply voltages are on the fall. At the same time, the growing demand for higher data throughputs results in wider buses and higher clock rates. To avoid the runaway of total current requirements of the wider buses, and to reduce the potential EMI risk, too, the signaling voltage drops steadily from generation to generation.

Because in every new generation new functionality is added, the growth of the number of I/O lines usually outweighs the decrease of current in one I/O, therefore the net supply current demand is still on the rise. The lower signaling voltage calls for a lower value of tolerable noise on the supply rails, which together with the higher current consumption dramatically reduces the impedance that should be provided by the power-distribution network [1]. The faster bus signaling also comes with faster edges and transients, requiring a proportionally wider bandwidth in the power-distribution network. A high-end system today with single-ended signaling may have 10A total transient current in the signal-return paths of buses, and may require 50mV maximum ripple on the power-distribution network. This converts into 5 milliohms of required power-distribution impedance. With a 0.6 … 0.3nsec signal transition time, the necessary bandwidth for the 5 milliohm power-distribution impedance is 500-1000MHz.

The transient current entering the planes have two sources: a) crow-bar current spikes resulting from the switching activity of the silicon core and I/O cells, and b) signal return current associated with the signals through the system interconnects (Fig. 1). While the first kind of transient current may be reduced and decoupled from the planes by adding capacitance locally to

the silicon and/or making use of the package power-pin inductances, the return current of the high-speed single-ended signals is always present on the planes. To avoid excessive simultaneous switching noise, the power-distribution network (the power-distribution planes) must exhibit low enough impedance over the full bandwidth of signals.

This paper deals with the power distribution planes. First, the bare-plane impedances are given, and simulated self and transfer impedances of bare planes are shown. Second, a Dissipate Edge Termination (DET) is described which suppresses resonances and reduces radiation from the edge of the board. Simulated impedance plots are presented to show the insensitivity of the DET to component tolerances. Finally measured impedance plots are compared against simulated impedance curves.

II. Characterization of power-ground distribution

For digital electronics below the MHz clock-frequency range, individual traces or metal bus bars were sufficient to distribute ground and power. In the MHz range, the ground traces were gradually replaced by a solid copper layer in the multilayer board, while the power distribution many times still relied on individual traces rather than solid planes. With a solid ground plane, impedance-matched traces also became common. A solid ground plane serves to distribute power and to carry the return currents of signal traces. With low trace density, the ground plane behaves like an ideal ground. With increasing speeds and trace densities, the inductive and resistive drops along the ground plane have to be considered [2]. In recent years, signal speeds and trace densities reached values such that the return current required solid power planes as well, forming a pair of parallel planes in the Power Distribution System (PDS).

If the two planes are placed closer, the static capacitance between them is increased, which helps local bypassing, at the same time the return current travels a shorter distance from one plane to the other, such reducing the inductive voltage drop in the PDS. As for signal traces as well, the above lumped approximations, which start out with the static capacitance and loop inductance, are accurate only as long as the dimensions are much shorter (say ten times smaller) than the shortest wavelength of the signals. Signal transition times in high-speed digital systems today are one nsec or less. In FR4 dielectric, the bandwidth of a one nsec transition time signal corresponds to an approximate wavelength of 50 cm. Therefore boards bigger than 5cm in size, with digital signals faster than a nanosecond, the distributed nature of power-ground planes must be considered.

Power and ground planes in a multilayer PCB may be considered as two-dimensional transmission lines, where both the x and y dimensions are longer than one tenth of the shortest wavelength of interest (Fig. 2). Throughout this paper we assume that the h separation of the planes along the Z axis is still negligible compared to the shortest wavelength.

II.1. Analytical expression of power-ground plane impedances

In contrast to signal traces where the signal travels along the axis of signal conductor, the wave generated by an injected signal between the planes launches a radially expanding wave. Two-dimensional transmission lines are therefore also referred to as radial transmission lines. The self and transfer impedances of radial transmission lines with rectangular or circular shapes can be analytically calculated. Impedances of circular discs are derived in [3]. Impedances of

square-shaped parallel planes are widely analyzed in the literature for printed antennas. Analytical formulation is given, e.g. in [4], [5].

Assuming infinitesimally small port sizes, and open boundaries at the edges, the generalized transfer impedance between ports i and j (at coordinates x_i, y_i, and x_j, y_j, respectively) of a pair of parallel, rectangular planes with side dimensions w_x and w_y along the x and y axes, with plane separation (dielectric height) of h along the z axis, can be written as:

$$Z_{ij}(w) = jwmh\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{c_{mn}^{\ 2}}{w_x w_y\left(k_n^{\ 2}-k^2\right)}\cos\left(\frac{2mp\ x_i}{2w_x}\right)\cos\left(\frac{2np\ y_i}{2w_y}\right)\cos\left(\frac{2mp\ x_j}{2w_x}\right)\cos\left(\frac{2np\ y_j}{2w_y}\right)$$

Where $\omega=2\pi f$ is the angular frequency

μ is the permeability of dielectric ($\mu=\mu_0=4\pi 10^{-7}$)

$$k_n^{\ 2} = \left(\frac{mp}{w_x}\right)^2 + \left(\frac{np}{w_y}\right)^2$$

$$c_{mn} = 1 \text{ for } m=0 \text{ and } n=0;\ \sqrt{2} \text{ for } m=0 \text{ or } n=0;\ 2 \text{ for } m\neq 0, n\neq 0$$

$$k = w\sqrt{em} = w\sqrt{e_r e_0 m_0} = \sqrt{e_r}\,\frac{w}{c}$$

c is the speed of light, and for lossless structure

The above expression of $Z_{ij}(\omega)$ lends itself well to numerical calculations, but it is not well suited for circuit simulations, where the power-ground planes have to be simulated together with the connected electronics. For circuit simulations, either a macromodel can be generated [6], or an electrical equivalent circuit of the pair of planes is formed.

II. 2. Model for simulation power-ground plane impedances with grid equivalent circuit

A pair of parallel planes can be simulated by an equivalent circuit of a grid of transmission lines, as described in e.g., [7], [8]. The low-frequency equivalent components of the planes can be derived from a quasi-static model. We assume a pair of rectangular planes with dimensions of w_x and w_y. First we define the w_u size of the square unit grid cell (Fig. 3), which should be equal to or less than 10% of the shortest wavelength of interest. The w_u cell size is selected such that we have an integer Nx and Ny number of cells along the x and y axes, respectively.

For every unit square of the planes with side dimensions of w_u, plane separation (dielectric height) of *h*, the C_u static plane capacitance and t_{pd_u} propagation delay along the edge are:

$$Z_{0u} = \frac{t_{pd\_u}}{C_u} = 120p\,\frac{h}{w\sqrt{e_r}}, \quad L_u = Z_u t_{pd\_u} = m_0 h$$

From the capacitance and delay, an equivalent Z_{0u} characteristic impedance and L_u inductance of the unit cell can be calculated:

$$C_u = e_0 e_r \frac{w_u^{\,2}}{h}, \qquad t_{pd\_u} = \frac{w_u \sqrt{e_r}}{c}$$

In the above expressions, all input and output parameters are in SI units; c = $3x10^8$ [m/sec] is the speed of light in vacuum, $\mu_o = 4\pi 10^{-7}$ [H/m] is the permeability of vacuum. The unit cells are replaced by four transmission lines along the edges of unit cells, each transmission line representing the same delay but only one quarter of the area, thus having an impedance of $4Z_{0u}$. Inside the equivalent grid, where the sides of unit cells touch, two transmission lines are connected in parallel, reducing the characteristic impedance to $2Z_{0u}$. Along the outer edges, the unit-cell transmission lines are standing alone (Fig. 4). The parameters for the edge (Z_{0e}, t_{pde}) and grid (Z_{0g}, t_{pdg}) transmission lines are:

$$Z_{0g} = \frac{2}{\sqrt{2}} Z_{0u}, \; t_{pdg} = \frac{1}{\sqrt{2}} t_{pdu} \qquad Z_{0e} = \frac{4}{\sqrt{2}} Z_{0u}, \; t_{pde} = \frac{1}{\sqrt{2}} t_{pdu}$$

The sqrt(2) correction factor is used to match the equivalent circuit's delay and impedance along the x and y axes (see e.g., [10]). Alternative equivalent circuits may use lossless LC ladder [9] or lossy transmission lines [10] representation of each transmission-line segment. For all simulations presented in this paper, lossless transmission line grids were used. Note that the grid takes the effect of edge discontinuity into account to some extent by using twice the characteristic impedance of transmission lines along the edges. While this provided reasonable match between measured and simulated values for the DUT dimensions used in this paper, more sophisticated models may be necessary to model other geometries.

II.3. Simulated impedances of bare power-ground planes

The steady-state impedances of parallel ground-power planes of different dimensions were simulated with SPICE, using a swept-frequency current source of 1A. The entire impedance profile was simulated by moving the current source through all of the $(N_x+1)*(N_y+1)$ nodes, and recording the voltages for all of the cases at all of the nodes. The Z_{ii} self and Z_{ij} transfer impedances are then calculated as:

$$Z_{ii} = \frac{V_i}{I_i}, \; Z_{ij} = \frac{V_i}{I_j}$$

To illustrate the self and transfer impedances of bare planes, simulation results are shown on a 9" by 4" pair of planes separated by 2 mil of FR4 dielectric. The unit-cell grid size was 0.5 inches (Fig. 5), which results in N_x=18, N_y=8. The equivalent circuit is valid up to about 1GHz. Figure 6 shows two self and two transfer impedance plots. The self impedance plots exhibit the first minimum at a frequency where the distance from the probe location to the open boundary corresponds to one quarter of the wavelength. Due to the lossless assumption, the impedance is purely reactive, either capacitive or inductive. Below the lowest resonance frequency, the self impedance is capacitive. Above the lowest resonance frequency, the self impedance is mostly inductive. The transfer impedances show a similar structure: purely reactive impedance, and

alternating minima and maxima beyond the lowest resonance frequency. To illustrate the surface distribution of impedances, Fig. 7 shows the self and transfer impedances at 400MHz. The impedance plots follow the standing wave pattern over the planes. The transfer impedances are shown with the 1A excitation at location x=6, y=3, corresponding to the peak on the imaginary transfer impedance plot. Note that due to resonances, transfer impedances at remote plane locations may be higher than the self impedance at the source. This indicates that noise voltage gets amplified at certain locations and certain frequencies as it travels on the bare planes.

Besides of the resonance peaks of impedance profiles, the open-edge parallel-plane structure is also prone to higher radiations [11], [12], which raises EMI/EMC concerns.

III. Reducing plane resonances with Dissipative Edge Termination (DET)

The simultaneous switching noise on PDSs, including the resonances of power planes is described extensively in the literature, see e.g., [13], [14], [15], [16], [17]. To make use of the low-inductance bypass capacitance formulated by the PCB planes, but at the same time reducing the concerns of standing waves and edge radiation, different techniques can be used to suppress the resonances. The inherent dielectric losses together with the copper DC and skin losses reduce the resonances to some extent [5]. In other solutions highly lossy dielectric materials are used ([18], [19]). The standing waves can also be reduced by selecting a proper reactive (capacitive) [20], or dissipative (resistive) termination scheme along the PCB edges ([21], [22], [23]).

III.1. Design steps of Dissipative Edge Termination

By using the one-dimensional transmission-line analogy, one can reduce the reflected waves from the planes' open boundaries by putting resistive termination along the edges. For instance, Dissipative Edge Termination (DET) can be implemented by connecting discrete termination resistors of $R_t = 2*Z_{ou}$ value at every w_u spacing along the board edges, or to implement a distributed buried resistive strip between the planes' edges. As we see later, the value of termination resistance is not critical.

Since power and ground planes carry different DC voltages, a C_t DC blocking capacitor is also required in series of the termination resistance. In the discrete implementation, the L_t mounted inductance of the R_t and C_t components should also be considered. To achieve effective termination up to a predefined f_0 frequency limit, we must ensure that the w_u spacing between the termination components along the edge is set to the smaller of the following two limits:
a) the discrete terminations will approximate a continuous termination network as long as the w_u spacing is less than 10% of the wavelength at the highest (f_0) frequency of interest, and
b) the ωL_t inductive reactance does not exceed R_t at the highest (f_0) frequency. Note that L_t is fixed and determined by the via and pad pattern, while R_t increases as the w_u spacing is reduced, thus making it possible to meet the goal over a wide range of input parameters.
Once R_t and their w_u spacing are determined, the C_t DC blocking capacitor can be selected such that their corner frequency is lower than the lower self-resonance frequency of the planes.

III. 2. Simulation of power-ground plane impedance with DET

To illustrate the self and transfer impedances of a pair of planes with DET, simulation results are shown on the same 9" by 4" pair of planes separated by 2 mil of FR4 dielectric. The unit-cell

grid size was 0.5 inches (Fig. 5), which results in N_x=18, N_y=8. The equivalent circuit is valid up to about 1GHz. The transmission lines had Z_{0g}=0.983 ohm, and Z_{0e}=1.97 ohm characteristic impedances inside the grid and along the edges, respectively. All segments had 64.9 psec delay. The termination resistors were set to $R_t = 2Z_{0u} = 2*\text{sqrt}(L\_u/C\_u) = 1.39$ ohms, placed at every grid node along the periphery. Figure 8 shows the self impedances at the center and corner, as well as the transfer impedances from the center to the midx and midy nodes. By comparing to the corresponding graphs of Figure 6, the major difference is the smoother impedance profiles. At low frequencies self impedances anywhere on the planes equal the parallel sum of all of the termination resistors, while at higher frequencies the self impedance becomes partly inductive, but never capacitive. To illustrate the surface distribution, Figures 9 and 10 show the self and transfer impedance surface profiles at 400MHz, assuming an ideal zero-inductance connection of the termination components to the planes. The effects of mounted inductance and resistor tolerance are considered later in section III.3. The variation of impedance is reduced compared to bare planes. However, because of the resistive termination, the plane impedance is not purely reactive any more.

Because with proper resistive edge termination the self impedance is inductive at any frequency and at any location on the planes, it is convenient to define an equivalent inductance of the planes as $L_{eq} = \text{Im}\{Z\}/\omega$. Figure 11 shows the real part of the impedance and the equivalent inductance of the planes as a function of frequency at the four representative locations. At low frequencies, the real part of the self impedance follows the parallel sum of the termination resistor values. However, above the lowest modal resonance frequency, the real part increases with an approximately 20dB/decade rate. The equivalent inductance at 100MHz at the corner, midx, midy, and center locations are 124pH, 51pH, 64pH, and 22.3pH, respectively. Note that the equivalent inductance of the parallel planes is μ_0*h=63.8pH for 2 mils separation. With dissipative edge termination, the self impedance has approximately twice of this inductance at the corners, and approximately 40% of this inductance at the center.

III. 3. Effect of mounted inductance and resistor tolerances on DET

III.3.1 Effect of mounted inductance

The inductive impedance in series to bypass capacitors limits their effectiveness at high frequencies [24]. To see how DET is affected by the mounted inductance of DET components, a series of simulations were performed on the equivalent circuit of 9” by 4” pair of planes. The termination resistance was kept at its nominal value, and the inductance in series to every termination resistor was varied through 10pH, 100pH, 300pH and 100pH values. Figure 12 shows the magnitude of self impedances at the four representative locations. The 10pH value corresponds to an ideal connection, probably achievable with embedded components directly attached to the planes [25]. The 300pH mounted inductance is an aggressive value, achievable with multiple vias. 1000pH represents a ‘bad’ pad and via geometry. Note that up to 300pH mounted inductance there is hardly any deterioration in the DET performance.

III.3.2. Effect of resistance tolerance

Figure 13 shows the insensitivity of DET to resistor tolerances. A pair of 8” by 8” square parallel planes with 2 mil FR4 separation was simulated. The edge of the structure was nominally terminated at every inch with 0.695 ohms resistance. The four charts correspond to infinite, twice the nominal resistance, nominal resistance, and half the nominal resistance

termination values. Note that there is very little difference in the DET performance between half the nominal value and the nominal value. This insensitivity lends itself to implementations with integrated passives, which offer low mounted inductance at a price of higher tolerances.

IV. Measurement results

To correlate simulated and measured impedances, a ten inch by ten inch square pair of planes was selected with 31 mil FR4 dielectric material. As shown in Figure 14, at every inch along the board periphery, surface-mount resistors were soldered to implement DET. Self and transfer impedances were measured with HP4396B and HP8720D vector-network analyzers in the 100kHz-1.8GHz, and 50MHz-5GHz range, respectively. The probe connections, calibrations, conversions from S parameters to impedances were according to [12] and [23]. To improve the measurement accuracy at low impedance readings, two-port S21-based self-impedance measurement was used. The S21 parameter readings were converted to self and transfer impedance values by the Z=25*S21 approximative formula. It was found that up to 1GHz, corrections for the probe-connection discontinuities were not necessary. For the simulations, the transmission-line grid size was set to one inch, and lossless Tlines models were used. Figure 15 shows the measured and simulated self impedances at the corner on bare planes and planes with DET. Figure 16 shows the measured and simulated transfer impedances from the corner to the center on bare planes and planes with DET.

V. Conclusions

Power-ground planes in multilayer printed-circuit boards with open edges behave like radial transmission lines, and exhibit multiple resonance frequencies. Dissipative Edge Termination (DET) along the board periphery reduces the resonances, and provides smooth impedance profile. The smooth impedance profile is maintained over at least a 2:1 variation of termination resistance values. The real part of the input impedance of terminated planes follows the DC termination resistance up to about the lowest modal resonance frequency, above which it rises with a rate of 20dB/decade. The equivalent inductance of the terminated plane is a weak function of frequency. The equivalent inductance is lowest in the middle of the planes, and rises to about five times higher values at the corner. The geometric mean of equivalent inductances at the corner and in the middle is close to the value of low-frequency unit-cell plane inductance.

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Figures:

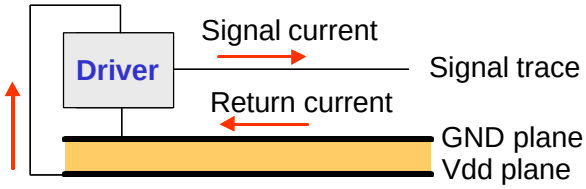


Figure 1: Signal and return currents of a single-ended driver powered from a pair of power-ground planes. Even if the signal trace references only the ground (or only the power) planes, the signal's return current crosses the power terminals at the driver point.

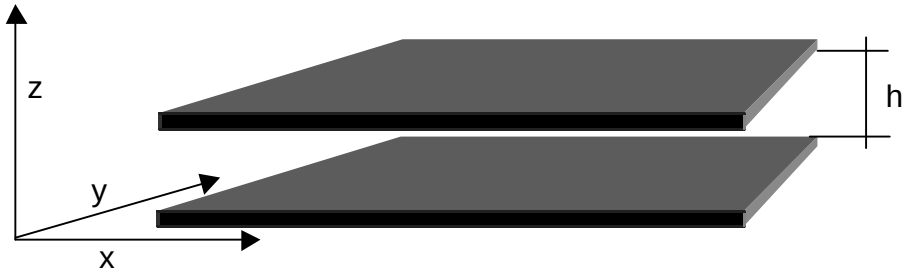


Fig. 2: A pair of parallel conductive planes in the x-y direction, where the h separation of planes is negligible compared to the shortest wavelength.

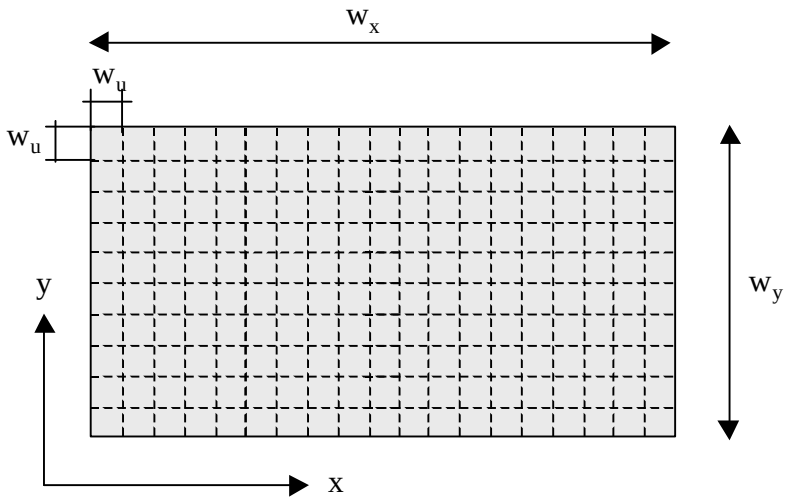


Fig. 3: Top view of a pair of rectangular planes with the overlaid grid that defines the transmission lines of the equivalent circuit.

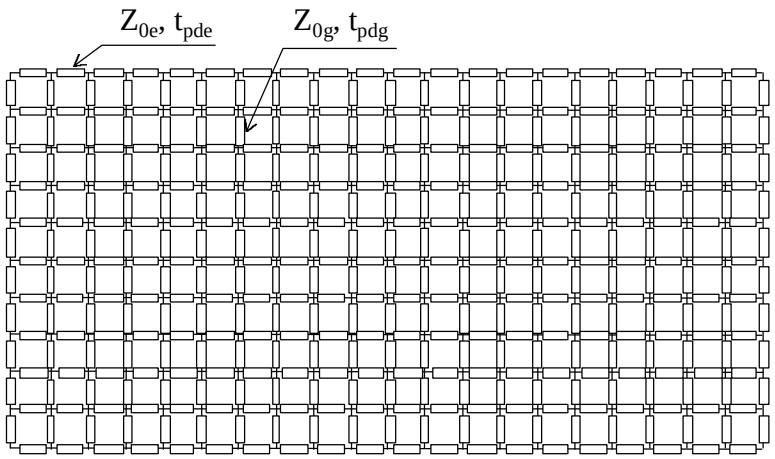


Fig. 4: Equivalent circuit representation of parallel conductive planes with a rectangular grid of transmission lines.

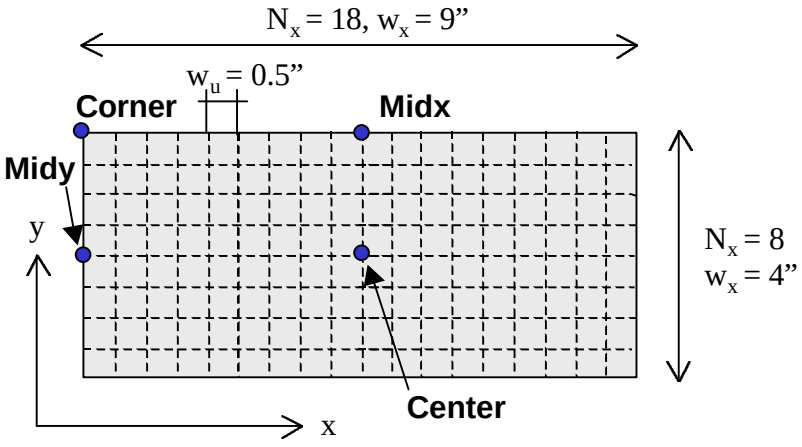
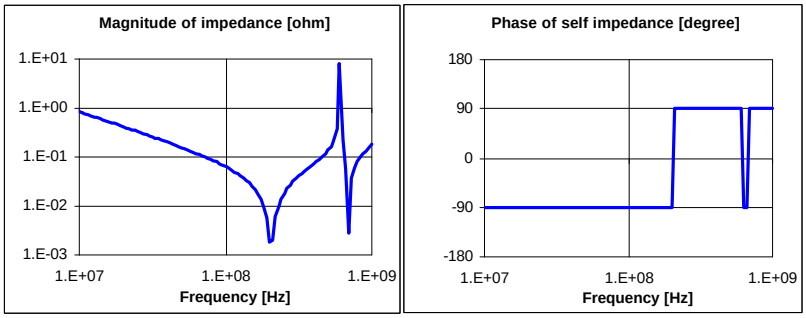
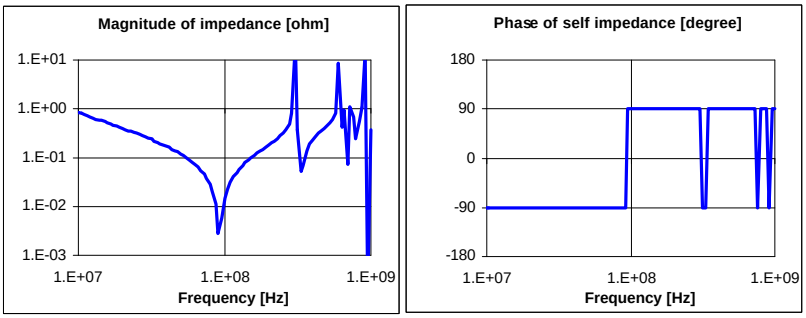


Fig. 5: Top view of a pair of parallel conducting planes with plane separation of h=2 mil.

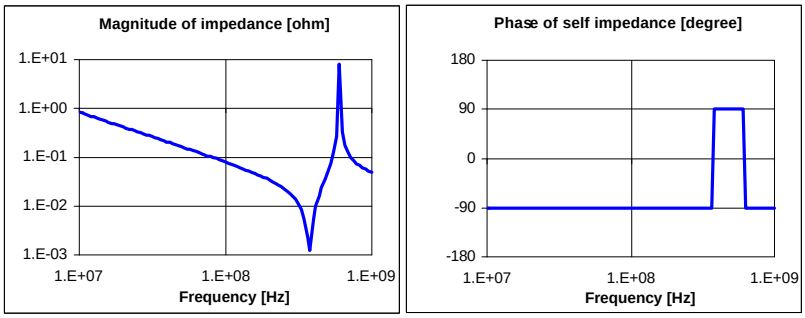
a)



b)



c)



d)

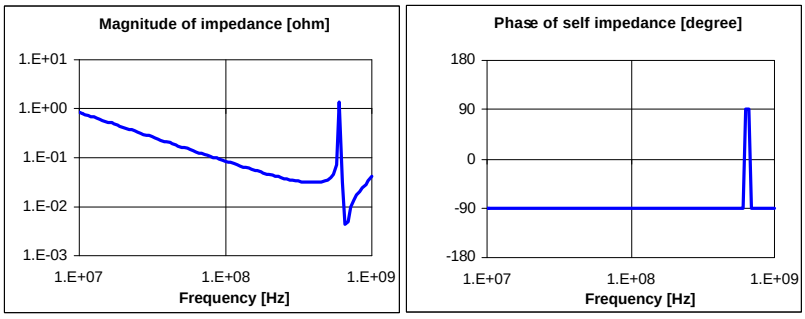
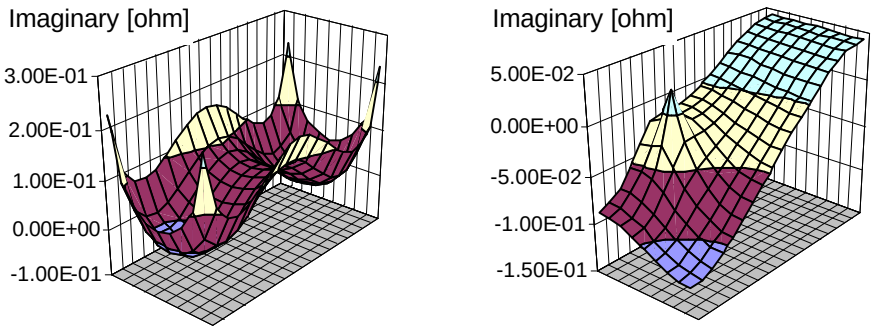


Figure 6: Impedances of a pair of 9” by 4” bare planes separated by 2 mil FR4 dielectric. Figs 6.a, b, c, and d show the self impedance at the center, self impedance at the corner, transfer impedance from center to midx, and transfer impedance from center to midy.



a) b)

Figure 7: Self impedance (a) and transfer impedance (b) of a pair of 9" by 4" bare planes separated by 2 mil FR4 dielectric, shown at 400MHz. Transfer impedance is shown from location x=6, y=3. The grid on the charts' floor shows the grid points where the impedance values were simulated.

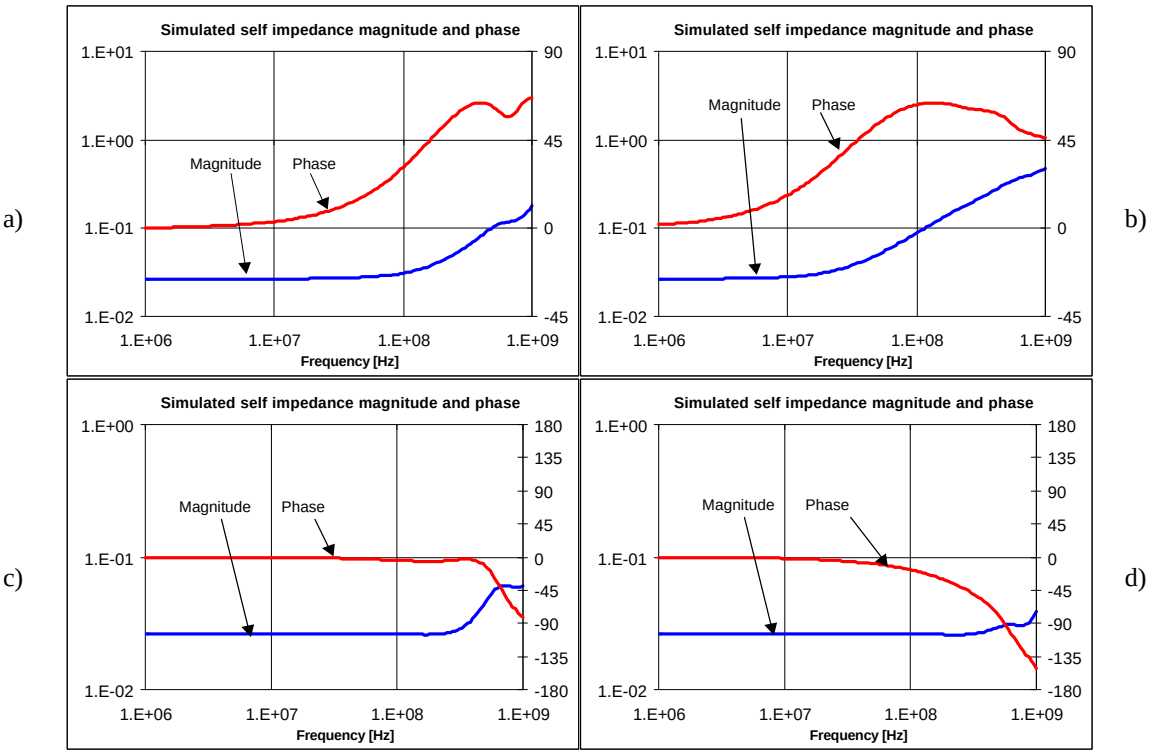


Fig. 8. : Impedances of a pair of 9" by 4" planes separated by 2 mil FR4 dielectric with 1.39 inch resistive termination at every half inches along the edges. Figs 8.a, b, c, and d show the self impedance at the center, self impedance at the corner, transfer impedance from center to midx, and transfer impedance from center to midy, respectively. On all graphs the left axis is for magnitude in ohms, right axis is for phase in degrees.

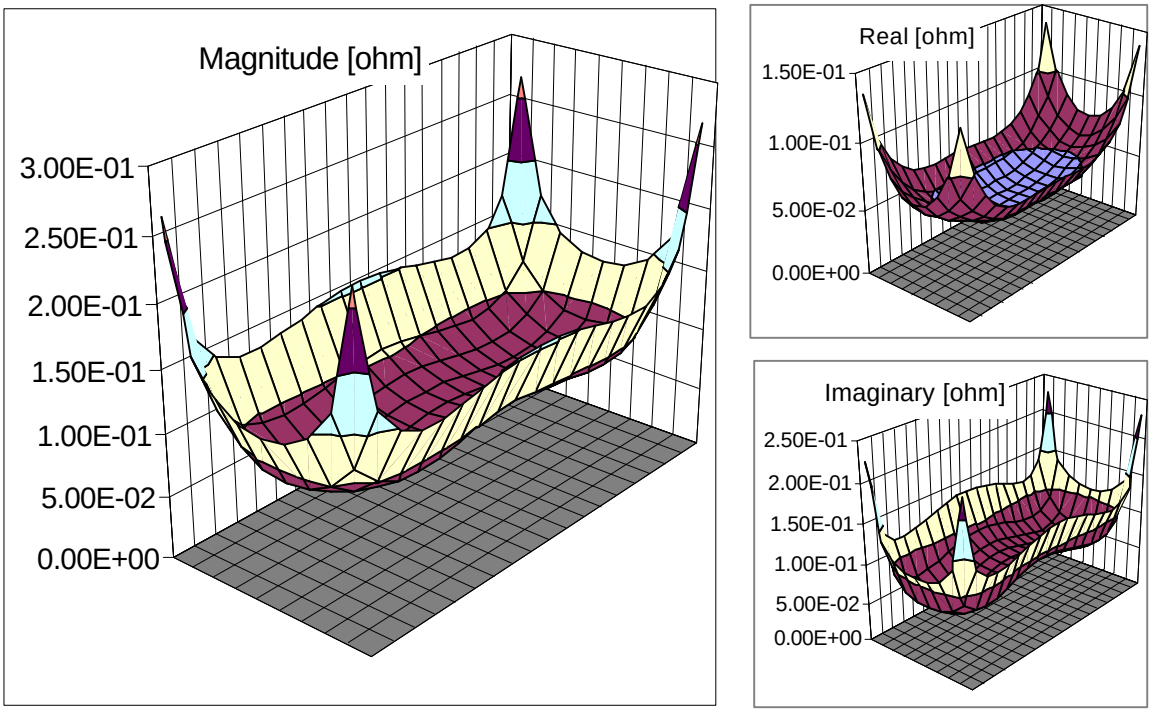


Figure 9: Self impedances of a pair of 9" by 4" planes separated by 2 mil FR4 dielectric, with 1.39 ohms resistive termination along the edges at every half inches, shown at 400MHz. The grid on the charts' floor shows the grid points where the impedance values were simulated.

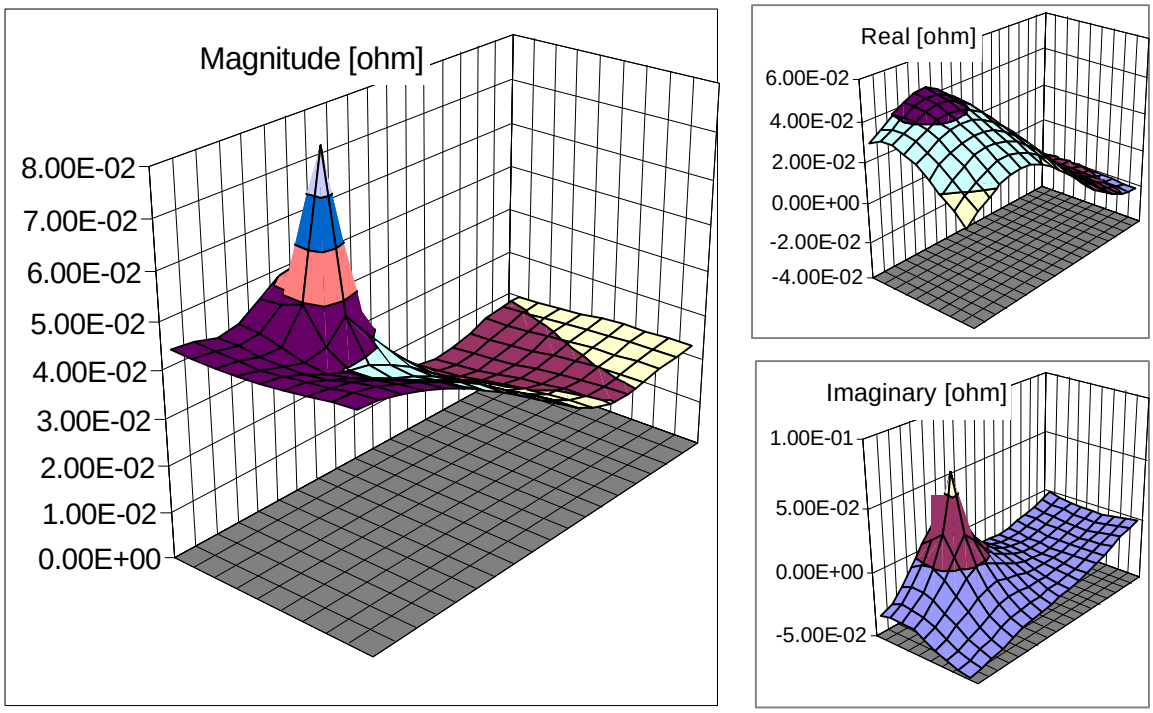


Figure 10: Transfer impedances of a pair of 9" by 4" planes separated by 2 mil FR4 dielectric, with 1.39 ohms resistive termination along the edges at every half inches, shown at 400MHz, from grid node x=6, y=3. The grid on the charts' floor shows the grid points where the impedance values were simulated.

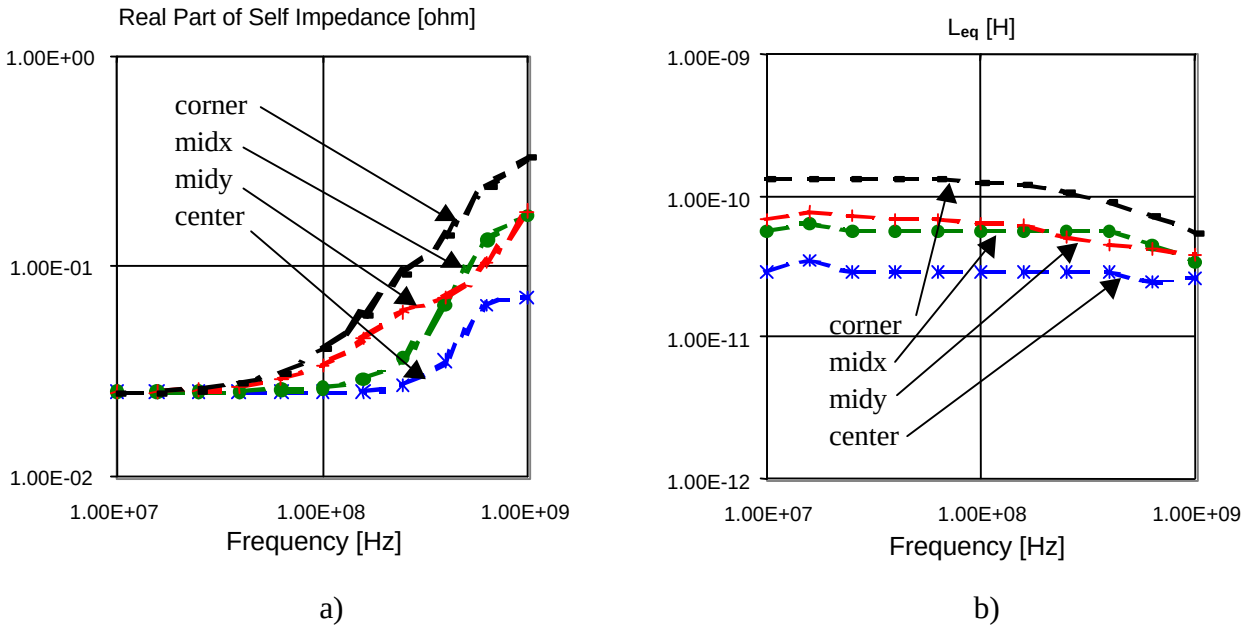


Fig.11: Simulated real part of self impedance (a) and equivalent inductance (b) of a pair of 9" by 4" pair of planes with 2 mil FR4 dielectric separation, and DET at every half inches along the periphery.

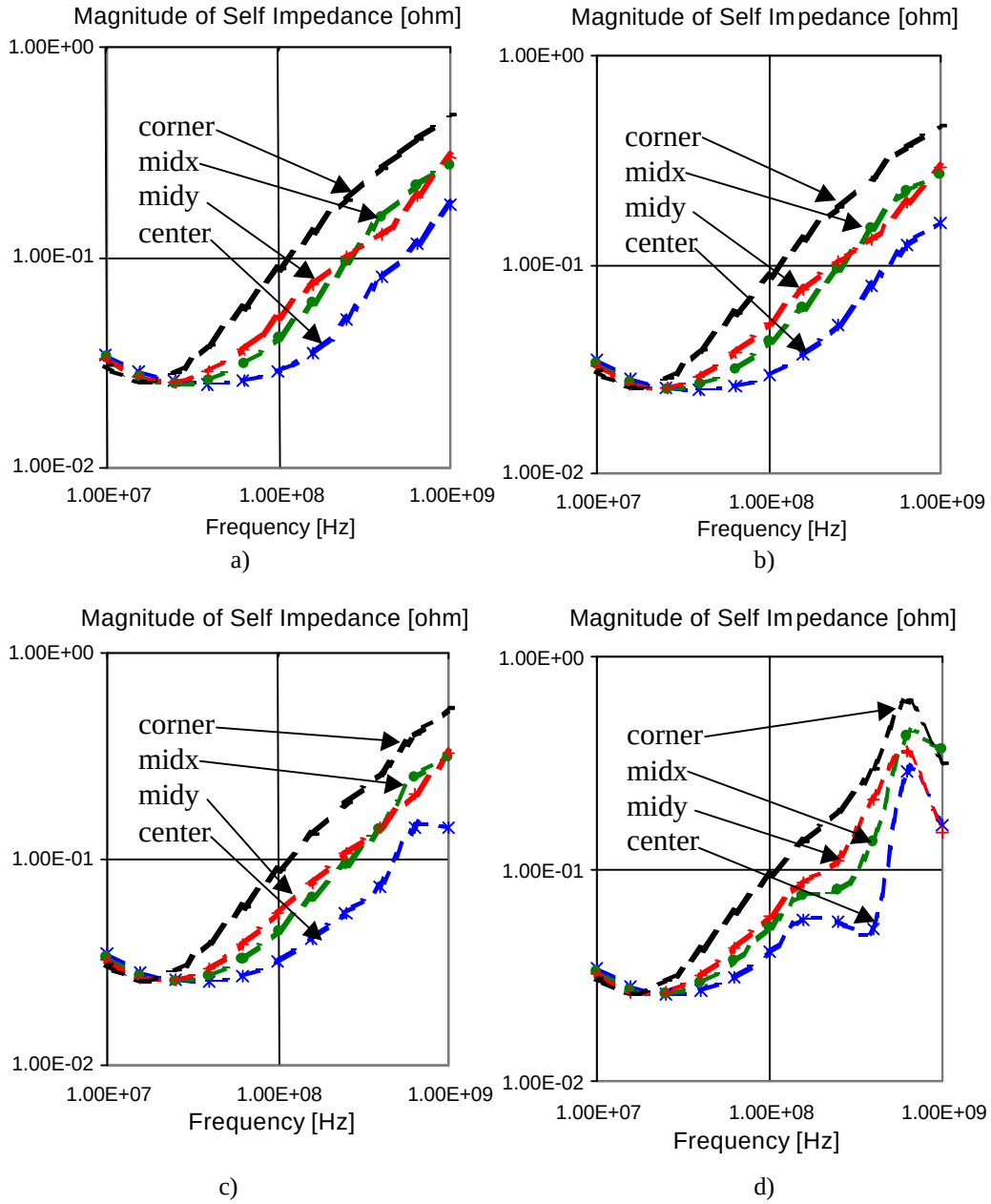


Fig. 12: Effect of mounted inductance on the self impedance of planes with DET, on a pair of 9" by 4" planes with 2 mil FR4 dielectric, with DET at every half inches. The mounted inductance for case a), b), c), and d) is 10pH, 100pH, 300pH, 1000pH, respectively.

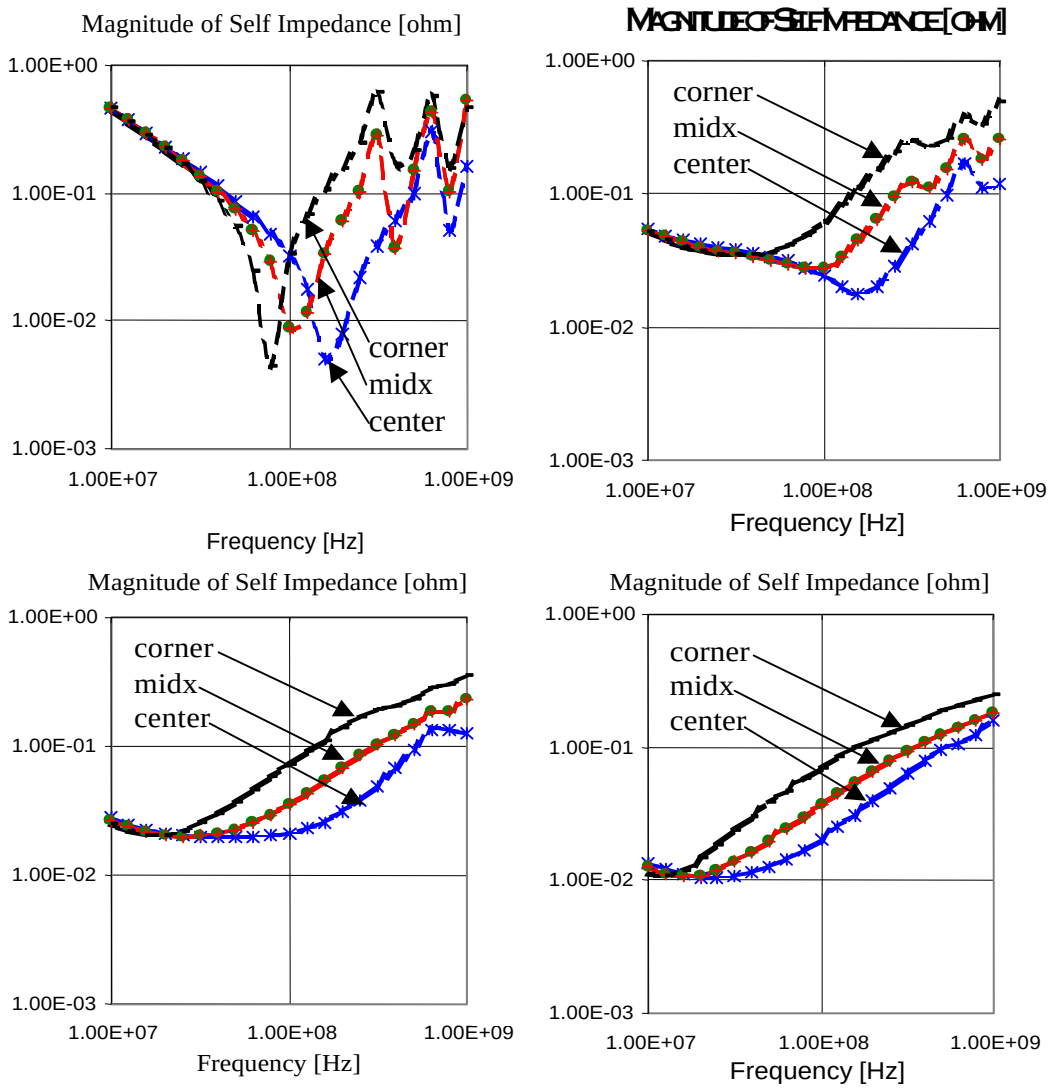


Fig. 13: Variation of self-impedances of a pair of 8" by 8" square planes with 2 mil plane separation, with different values of DET. The termination resistance from left to right, from top to bottom, in case a), b), c) and d) is infinite, twice the nominal value, nominal value, half the nominal value, respectively.

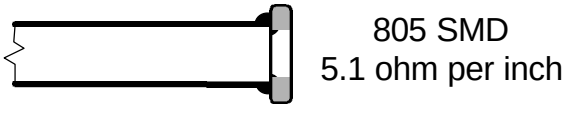
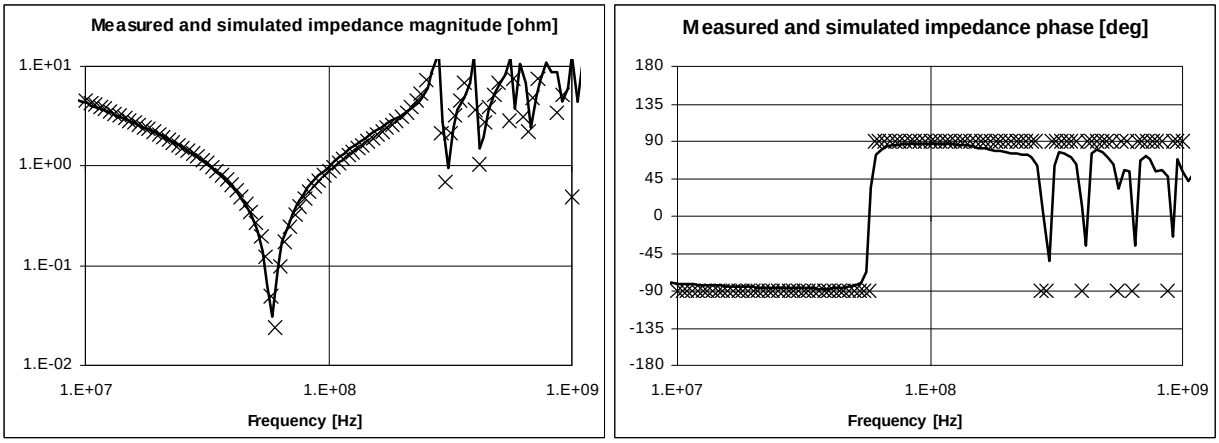
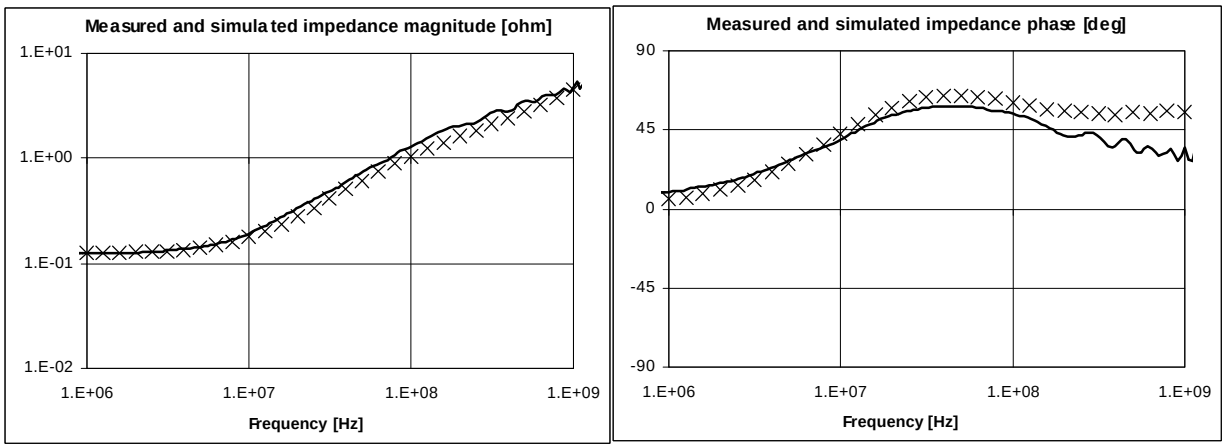


Figure 14: Side view of the connection of the DET components to the 10" by 10" 31 mil FR4 DUT.

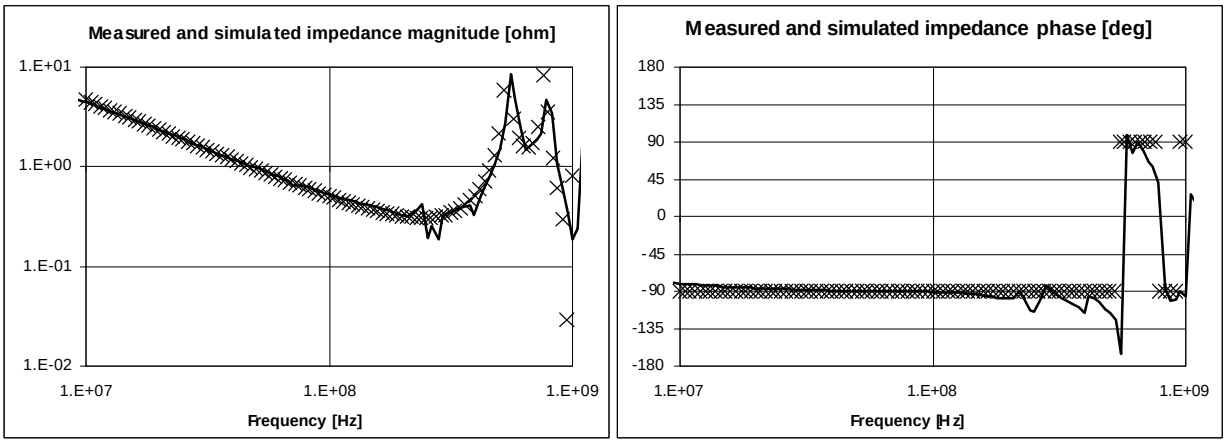


a)

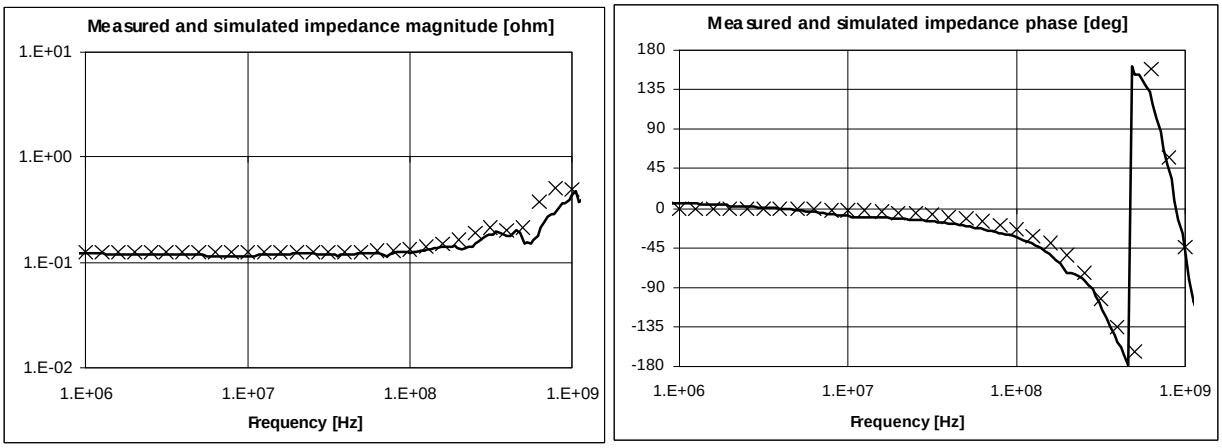


b)

Figure 15: Correlation of measured and simulated self impedances at the corner of a pair of 10” by 10” planes with 31 mil FR4 dielectric, with bare boards (a) and DET at every inch along the periphery (b). Solid line: measured, crosses: simulated.



a)



b)

Figure 16: Correlation of measured and simulated transfer impedances from the corner to the center of a pair of 10" by 10" planes with 31 mil FR4 dielectric, with bare boards (a) and DET at every inch along the periphery (b). Solid line: measured, crosses: simulated.