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TecForum HP-TF2

Thin PCB Laminates for Power Distribution How Thin is Thin Enough ?

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Abstract

The purpose of this TecForum is to bring together representative OEMs, PCB fabricators, and material suppliers to answer these questions: how thin is thin enough; when will these thin laminates be needed; and will the industry be ready.

The TecForum will start with an introduction summarizing the definition and classification of thin laminates, followed by some illustrative comparisons of measured data on test boards with various thin laminates. The speakers will answer frequently asked questions, prepared in advance, and may also present a short paper to expand on specific details. This will be followed by a panel discussion and an opportunity for questions and answers.

During the TecForum we will provide some details of physical and electrical attributes of thin laminates; get an overview of the requirements and the perceived design opportunities as viewed by some OEMs; disseminate the latest mechanical, processing, yield and capacity, and reliability and test information from the fabricators and material suppliers on thin laminates and PCBs incorporating these laminates; estimate cost and availability.

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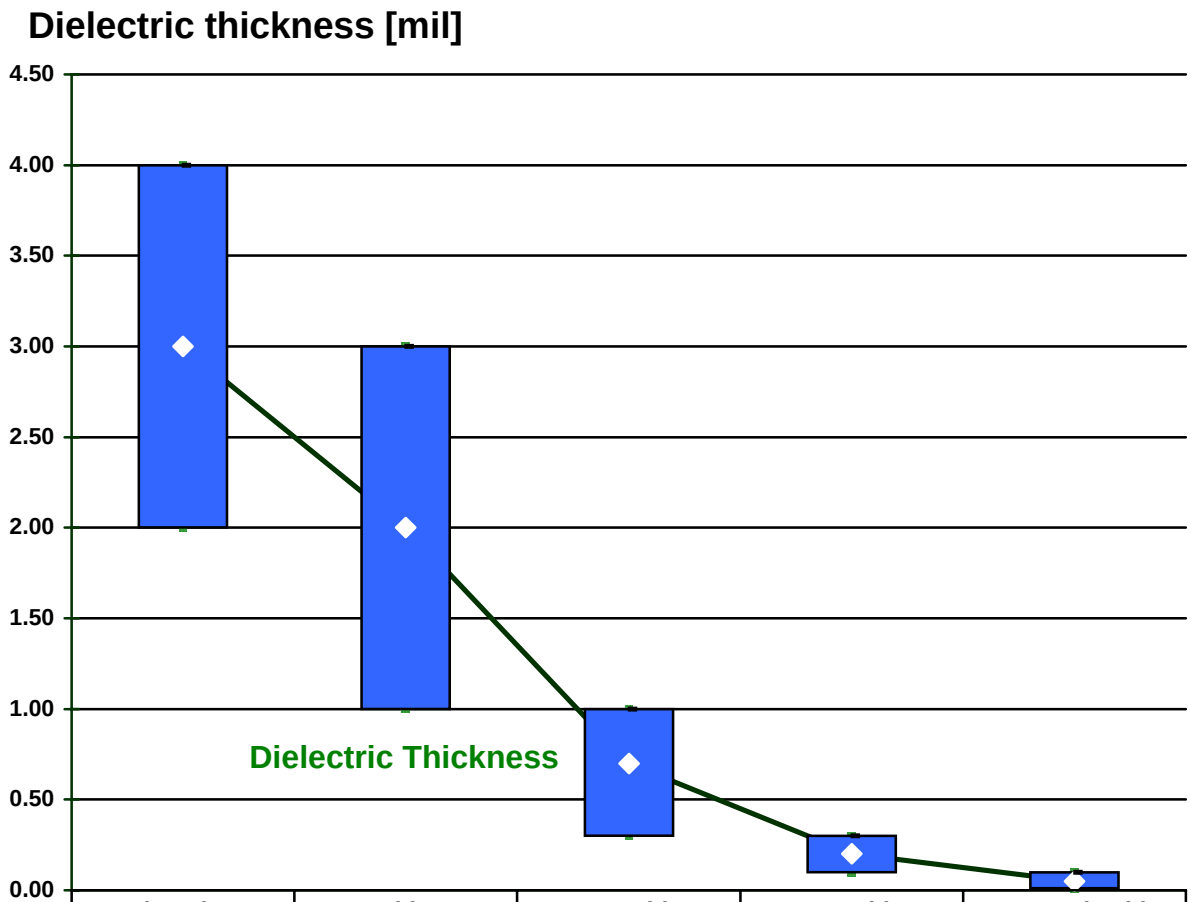
I. Introduction

Laminate thickness nomenclature



	Fine Line	Thin	Very Thin	Utra Thin	eXtremely Thin
Min	2.00	1.00	0.30	0.10	0.01
Nom	3.00	2.00	0.70	0.20	0.05
Max	4.00	3.00	1.00	0.30	0.10

Frequently Asked Questions for Original Equipment Manufacturers (blank template)

Current applications with <= .002” P/G cores
- Key driver(s)
- Nominal dimensions and tolerances
- Benefits

Any active (very, ultra, extremely) thin core projects ?
- Describe
- Key driver(s)
- Perceived benefits
- Constraints to implementation
- Dielectric Strength (Withstanding Voltage) requirement?
- Cost budget or tolerance for cost premium
- Alternatives

List desired physical attributes:

List desired electrical attributes:

If available, within cost budget, use would be:
- Pervasive
- Frequent
- Occasional

Schedule; desired time to:
- Samples / Engineering / Verification
- Proto-Circuits
- Volume Circuits

Future Requirements: Roadmap?

Frequently Asked Questions for Printed Circuit Board Materials Suppliers (blank template)

Describe (very, ultra, extremely) thin core product
- Physical
- Electrical

Experience
- Volumes run to date
- Yield data
- Lessons learned
- Obstacles to implementation

Key schedule milestones

Availability; Time to:
- Samples / Engineering / Verification
- Small runs
- Volume

Anticipated cost per square foot (delivered price to PCB fabricator)
- Near future
- Intermediate
- Longer term

Reliability testing results (materials)

Agency or regulatory approvals
- Necessary
- Complete

Frequently Asked Questions for Printed Circuit Board Fabricators (blank template)

Current production with <= .002” P/G cores
- Some
- Considerable
- High volume

Describe “typical” product from above
- (e.g; # layers; BGA ?? mm pitch / ?? leads; thickness …)

Any current (very, ultra) thin core projects ?
- Describe
- Customer driven or independent development ?
- Requirements
- Key schedule milestones

Experience
- Equipment (DES, AOI, ET, etc. ..)
  - In Place
  - Planning
  - TBD
- Volumes run to date
- Yield data
- Lessons learned
- Obstacles to implementation

Anticipated cost to implement
- (as a percentage of current P/G layer cost, e.g; 2.5X)

Reliability testing results (PCBs)

Agency or regulatory approvals
- Necessary
- Complete

II. Prior Art

II. 1 NCMS Embedded Decoupling Capacitance Project

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Introduction

Electronic products are increasing rapidly in component packaging density and speed. These advances are placing increasing demands on the interconnect structure to provide not only higher wiring capacity, but also better electrical performance. The printed wiring board (PWB) structure itself is becoming increasingly more important in achieving good signal integrity and meeting standards for radiated emissions.

The need for power-ground decoupling capacitance is nearly universal in electronic circuits. Today, this need is satisfied through discrete chip capacitors. However, as circuit designs increase in speed, the effective use of decoupling capacitors is becoming more difficult to achieve. The parasitic inductance associated with the circuit connections of the decoupling capacitors decreases their effectiveness at higher frequencies. Furthermore, few designers or engineers understand, with any rigor, how many decoupling capacitors are required, how much capacitance they should have, and where to locate them on the circuit. Decoupling capacitors also require valuable amounts of PWB surface area, consuming up to 50% of the total board area.

The increasing packaging densities are creating a desire to free up valuable surface real estate currently occupied by discrete capacitors. New capacitive materials, physically and chemically compatible with standard fire retardant grade 4 laminate (FR-4) material, are being developed as one potential solution to this challenge.

Consequently, in 1998, NCMS and Storage Technology Corporation (StorageTek) initiated and organized the Embedded Decoupling Capacitance (EDC) Project, aimed at advancing the technology of embedded components. Specific areas of interest were the use of embedded capacitance to reduce the number of surface-mounted capacitors used for power supply decoupling and electromagnetic compatibility (EMC).

Project Goal

The goal of the EDC Project was to evaluate the performance of distributive embedded capacitance in circuit boards for power supply decoupling and electromagnetic interference (EMI) suppression and to compare the results with standard surface mount technology (SMT). To achieve this goal, it was necessary to demonstrate that available EDC materials are manufacturable, that they have the physical properties to electrically perform as discrete capacitors do, and that PWBs containing them are reliable.

It was also important to understand power supply decoupling, and to develop the ability to predict how and when embedded capacitance will work for a given circuit design. The project took some of the first steps towards the realization of embedded passives in organic substrates.

Organization Structure

The 30-month EDC Project effort was co-sponsored by the Department of Defense (DOD) Commercial Technologies for Maintenance Activities (CTMA) Program. CTMA is a partnership between the NCMS and the DOD.

The objective of the CTMA program is to bring advanced commercial technologies to bear on the operations and problems of the DOD logistics activities. Under this agreement, NCMS and its member companies co-sponsor technology development, deployment, and validation with the DOD and its organic maintenance activities.

The current focus is the use of manufacturing technologies to reduce the costs associated with maintenance and rebuild of weapons systems as an element of the overall maintenance strategy. By partnering with NCMS members, the organic maintenance activities are able to quickly assess and apply the benefits of new manufacturing technologies in their own facilities while working side-by-side with industry leaders in solving manufacturing problems through collaboration.

The EDC Project was organized to encompass the entire electronics manufacturing chain, from materials suppliers to the original equipment manufacturers (OEMs). During the formation of the project, it was recognized that the most important deliverable would be an improved understanding of decoupling capacitance—especially if that understanding could be presented in formats that would be useful to circuit designers and circuit fabricators. This approach is reflected in the membership of the project and in the project plan.

The initial project organizational meeting drew representatives from some 40 organizations, indicating widespread interest within the North American electronics industry. Ultimately, 17 highly reputable and diverse organizations formed the consortium to conduct the project.

The consortium comprised the following categories of members:

- OEMs:
  - StorageTek
  - Delphi Automotive Systems
  - Raytheon Systems Company
- Material Suppliers:
  - 3M
  - DuPont
  - Polyclad Laminates, Inc.
  - AlliedSignal
- PWB fabricators:
  - HADCO
  - Merix
  - Raytheon Systems Company
  - Litton Interconnect Technologies
- Contracted Services:
  - Pennsylvania State University (Penn State)
  - University of Missouri–Rolla (UMR)

- Government Agencies:
  — National Institute of Standards and Technology (NIST)
  — Tobyhanna Army Depot
- Program Administration:
  — NCMS.

Figure i is a photograph of the consortium team taken at the first project industry workshop held in Tempe, Arizona, in February 2000.

This collaboration was implemented via a Project Agreement executed by the OEMs and NCMS, supplemented by separate Provider Agreements with individual materials suppliers and board fabricators and subcontracts with universities. This model for collaboration worked effectively to achieve the objectives of the EDC project and to deliver significant benefit to all project participants.

The total estimated program value is $1,345,000. The industry participants and CTMA shared these program costs: a cost share ratio of some 7:1 industry to DOD was achieved.

Project Plan

The primary objective was to evaluate embedded capacitance materials in circuit boards for power supply decoupling and EMI suppression and to compare the results with standard SMT design practices. The secondary objective was to develop preliminary design guidelines for use with selected technologies.

Each capacitive material was provided in sheet form with 1-oz copper cladding on each side. Each material was sent to two or more board fabricators for incorporation into multilayer PWB. Each fabricator also made boards with FR-4 materials to provide points of comparison should problems or unexpected issues arise during fabrication or testing. The resulting boards were sent to Delphi for reliability testing and to the University of Missouri–Rolla for measurements of power bus noise and radiated emissions, and modeling. Additional EMI testing was done at StorageTek. The embedded capacitance materials were also sent to Penn State and NIST for materials characterization.

Separate test vehicles were designed for reliability testing, electrical testing, and high-frequency performance. The reliability test vehicle had structures designed for materials characterization below 10 GHz as well as for reliability testing. The electrical test vehicle was built with several different stack-ups to permit the evaluation of the relative importance of shielding and decoupling. The microstrip test vehicle was developed to determine high-frequency performance above 10 GHz.

Figure i. Photo of EDC Project Consortium Team Members
(Not available for photo: Charles Grasso, StorageTek; Phil Bowles, Delphi; and Jim Reed, Raytheon)

Conclusions

The project developed the processes required to embed thin materials into FR-4 to form a high-capacitance layer between power and ground planes. The project measured the physical and electrical properties of the embedded materials, and determined their effectiveness in suppressing noise between power and ground, at frequencies up to the microwave. The project also determined the reliability of planar capacitance.

Using the physical and electrical properties measured, and the noise suppression characteristics, a model was developed that allows engineers to understand, in advance, the effectiveness of embedded capacitance and the need (or lack of need) for discrete chip capacitors. It is anticipated that, in many

cases, this understanding, plus the use of embedded capacitance, will result in lower system life cycle cost. It is also anticipated that, in almost all cases, the noise suppression characteristics of embedded capacitance will be superior to those of discrete capacitors especially at high frequencies.

The Embedded Decoupling Capacitance Project has demonstrated that embedded capacitance technology is an effective alternative to the use of discrete decoupling capacitors for power supply decoupling. Many benefits to design and assembly activities will be realized as this technology evolves.

The major conclusions of the project are as follows.

Materials

Materials characterization testing produced very useful data regarding the physical properties of the embedded capacitance materials. The work resulted in determining the performance over a wide temperature and frequency range. A new test method for measuring time domain reflectometer (TDR) response of embedded capacitance materials was developed. The overall results were favorable enough to encourage continued development work by the materials suppliers.

Fabrication

Board fabrication efforts showed that embedded capacitance materials can be used successfully to build PWBs. Only minor modifications to board fabrication processes were required. However, special design considerations must be met.

Reliability

All the embedded capacitance materials demonstrated equivalent or better reliability performance compared to FR-4 materials. Specifically, plated-through hole integrity was not compromised by the presence of embedded capacitance materials in the test vehicles.

Electrical Performance

All of the embedded capacitance materials exhibited sufficient loss to dampen power bus resonances. At frequencies above 1 GHz, embedded capacitance continued to dampen power bus resonances while discrete capacitors were shown ineffective. Further, embedded capacitance boards exhibited the same or lower radiated emissions than FR-4 boards with discrete capacitors.

Modeling and Design Considerations

Project data was used to validate electrical models of power bus structures at UMR. A set of preliminary design considerations was developed.

Materials Selection and Test Vehicle Design

Embedded decoupling capacitance (EDC) test boards were assembled in several configurations by multiple fabricators. The boards were used to characterize various EDC materials, assess the effects these materials have on printed wiring board (PWB) reliability, and compare the electrical performance of EDC technology to that of surface-mounted discrete capacitors.

Embedded Capacitance Materials

Like traditional copper-clad laminates, EDC materials consist of two copper planes separated by a layer of dielectric material. By applying power to one plane and ground to the other, an internal planar capacitor is created that can release stored energy to system components just as discrete surface mount technology (SMT) capacitors do. Five EDC materials, detailed in Table 1-1, were evaluated in this study.

These EDC materials have thinner dielectric layers than conventional circuit board laminates, and some of them are brittle due to the lack of a support structure within the dielectric layer. Also, the composition

and thickness of the dielectric layer depend on the supplier. These characteristics raise three main concerns for circuit boards containing EDC materials:

1. Failures in EDC materials may be difficult to locate and characterize.
2. EDC materials may adversely affect plated-through-hole (PTH) reliability by virtue of differing coefficient of thermal expansion (CTE) properties.
3. The EDC materials may require fabricators to use non-standard processes to incorporate them into circuit boards. The EDC consortium members carefully considered these concerns while designing this evaluation.

Test Vehicles

The test vehicles utilized in this evaluation are test vehicle 0 (TV0), high-frequency test vehicle (HF-TV), and test vehicle 1 (TV1). TV0 was designed to evaluate EDC material characteristics and circuit board reliability concerns. HF-TV was designed to evaluate EDC material characteristics at high frequencies. TV1 was designed to evaluate the electrical performance of the EDC materials in various build scenarios.

Description of Test Vehicle 0

TV0 (see Figure 1-1) is a four-layer circuit board (3.3 in. x 4.8 in.; 0.062-in. thick) with special areas devoted to reliability testing and dielectric characterization of EDC materials. Layers 1 and 4 are signal layers, Layer 2 is the power plane, and Layer 3 is the ground plane. The power and ground planes are solid copper, interrupted only by antipads located at each PTH. For baseline fire retardant grade 4 laminate material (FR-4) circuit boards, the dielectric thickness between the power and ground planes was specified at 0.004 in. For the EDC materials, this separation depended on the material used (see Table1-1).

Table 1-1. Evaluated EDC Materials

Material	Supplier	Dielectric Composition	Dielectric Thickness, mils
BC2000™	Polyclad	FR-4 epoxy/glass	2.0
EmCap®	Polyclad	Unsupported epoxy; ceramic powder filled	4.0
Kapton® HiK	DuPont	Unsupported polyimide; ceramic powder filled	1.6
C-Ply	3M	Unsupported epoxy; ceramic powder filled	0.2
XBC-1CC	AlliedSignal	Unsupported epoxy; ceramic powder filled	1.2

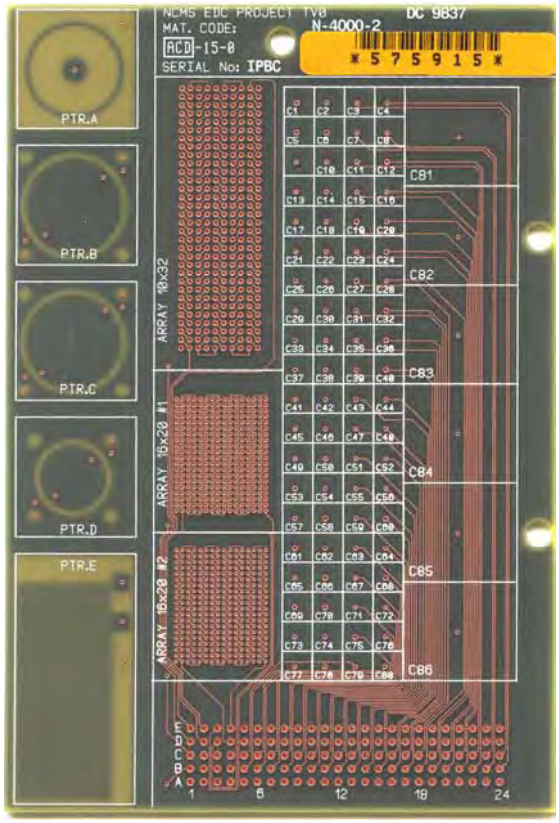


Figure 1-1. Test Vehicle 0

Delphi Automotive Systems provided the design concept for the reliability testing area. The National Institute of Standards and Technology (NIST) provided the design concept for the dielectric characterization area. Tobyhanna Army Depot used these design concepts to create the layout for TV0.

PTH Reliability Testing

Three areas of the test card were set aside for PTH reliability testing. This included three daisy chain pairs of PTHs connected to a through-hole connector (see Table 1-2).

Table 1-2. TV0 Daisy Chain Specifications

Daisy Chain Pair	Drilled Hole / Pitch	Antipad Size	Hole Array
DC 1 and DC 2	20 mils / 50 mils	40 mils	10 x 32
DC 3 and DC 4	13.5 mils / 35 mils	N/A*	16 x 20
DC 5 and DC 6	10 mils / 35 mils	30 mils	16 x 20

*These chains had a 0.560-in. x 0.700-in. opening in the copper planes on Layers 2 and 3 instead of antipads.

Embedded Capacitor Reliability Testing

TV0 contains two capacitor arrays; an array of 80 small capacitors (C1–C80) and an array of 6 slightly larger capacitors (C81–C86), for a total of 86 embedded capacitors. Each capacitor has the power terminal routed to the connector by means of a PTH at the center of the capacitor. For the 1 x 6 array, a 13.5-mil hole was drilled with an antipad of 33.5 mils in Layer 3. For the 4 x 20 array, four hole sizes and four antipad annuli in the ground plane were used in 16 hole/ annulus combinations to investigate their impact on reliability. The four hole sizes were 10, 13.5, 16.5, and 20 mils, and the four annular radii were 6, 8, 10, and 12 mils.

The connector selected for TV0 was a 120-pin, 2-mm pitch Robinson–Nugent product. It was rated to 125°C and was procured in both press-fit and wave solderable versions. The drilled holes were 31 mils in diameter and the antipads in Layers 2 and 3 were 51 mils in diameter. Half of the connectors used were press-fit and half were wave soldered.

Delphi Automotive Systems performed five reliability tests on the TV0 test vehicles:

1. Resistance to soldering heat
2. Thermal cycling
3. Operating life
4. Electrostatic discharge (ESD)
5. Dielectric withstanding voltage.

Dielectric Characterization Area

As listed in Table 1-3, the dielectric characterization area contained five test patterns, A through E, designed to characterize the dielectric properties of the EDC materials at frequencies from approximately 200 Hz to 500 MHz. Pattern A was designed as a termination for a coaxial connector for frequencies to 2.5 GHz. Patterns B, C, and D represented a parallel plate capacitance for frequencies below 100 MHz. Pattern E was designed to assess electro-migration resulting from the residual charge impurity levels at the surface and within the EDC materials. Guard surface circuitry in patterns B, C, and D minimized the effect of the fringing field and can be used to measure the surface leakage current. Patterns A, B, and D were used to make capacitor density measurements over the desired frequency range. Pattern C was a perforated pattern used for water absorption tests. Pattern E was also used to evaluate crosstalk on the EDC material surface.

Table 1-3. TV0 Material Characterization Test Patterns

Characterization Test	**Applicable Test Pattern**
Dielectric Constant, Dielectric Loss (Z, X–Y)	A–D
Capacitance Density	A–D
Electro-migration (Z and X–Y)	E
Moisture Absorption and Materials Reliability	C, E
Insulation Resistance	B–D

Description of the High-Frequency Test Vehicle

The HF-TV, shown in Figure 1-2, was used to evaluate EDC material properties at frequencies from 95 MHz to 5 GHz. It is a two-layer board consisting of micro strip lines, resonators, and co-planar terminations arranged in three sections, A, B, and C, having line widths of 400, 200, and 125 μm, respectively. In addition, there are five time-domain-reflectometer (TDR) sections for measuring permittivity based on a technique specifically developed for thin materials.

NIST developed the design concept for HF-TV. Raytheon's Electronics Systems Division performed the layout.

Description of Test Vehicle 1

TV1 (see Figure 1-3) is a set of circuit boards designed to evaluate the effectiveness of different EDC materials in various configurations. It was specially designed to produce noise levels that mandate the use of bypass decoupling capacitors. StorageTek provided the TV1 design concept, and Raytheon's Electronic Systems Division provided the layout.

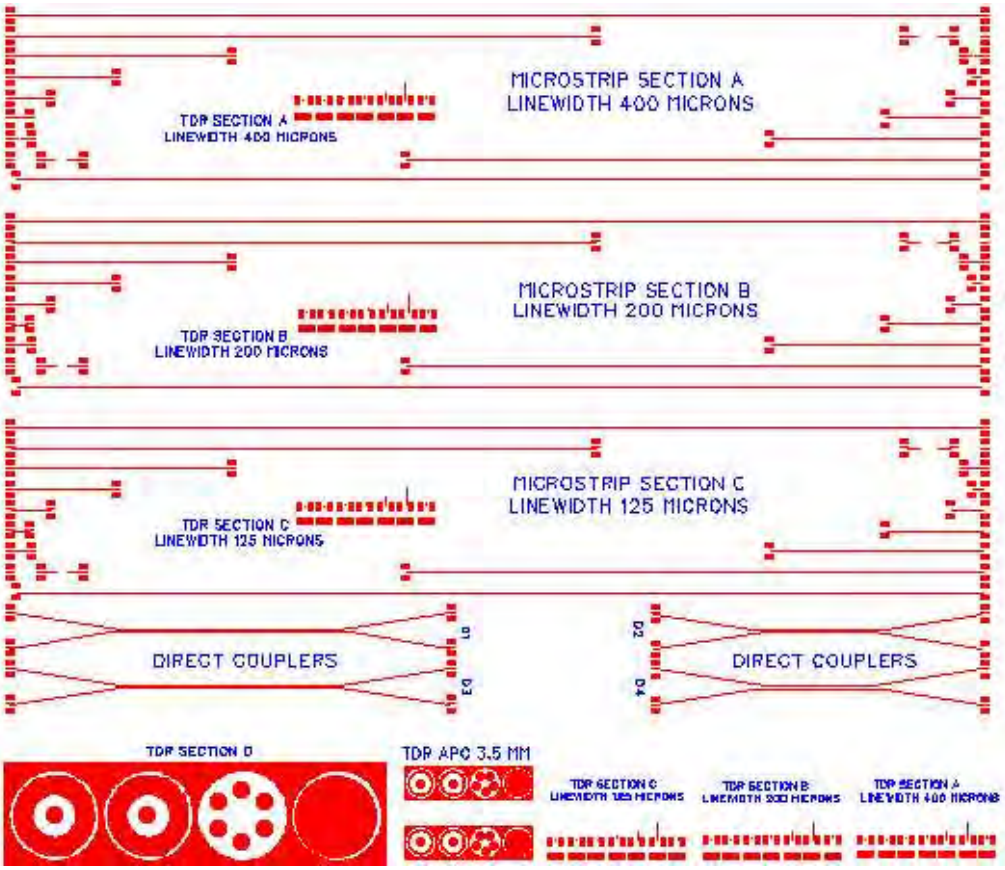


Figure 1-2. High-Frequency Test Vehicle Layer 1 Artwork

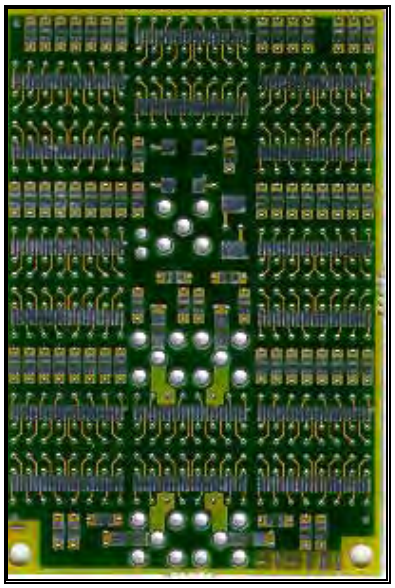


Figure 1-3. Test Vehicle 1

TV1s were fabricated using four of the five EDC materials used to build TV0. (The XBC-1CC material was omitted for the TV1 part of this evaluation by consensus of the consortium members due to handling issues). Three different layer stack-ups were used to build these boards. Also, three different layouts corresponding to three different board sizes were fabricated.

The nomenclature to identify the build configuration of a given test board was “TV1-X-Y,” where “X” indicates the layer stack-up used, with a value of 1, 2, or 3, and “Y” indicates the layout and board size, with a value of 1, 4, or 12.

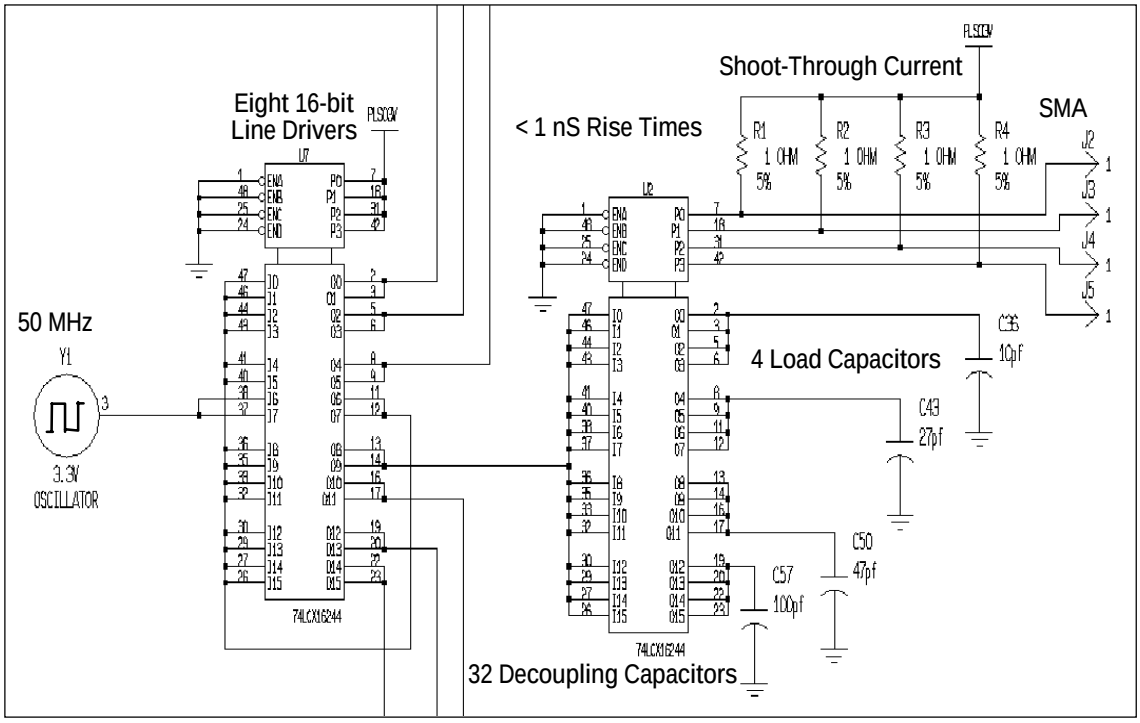


Figure 1-4. TV1 Partial Electrical Schematic

Electrical Schematic

The core circuitry of TV1 is based on a Philips 74LCX16244 integrated circuit (IC) and is shown in Figure 1-4. Each IC consists of 16 line driver buffer amplifiers. The ICs are interconnected, forming an asynchronous output. The supply voltage is 3.3 V, provided by an external power

supply. The input to the circuit is a square waveform running at a 50-MHz clock rate. The output pins of each IC are connected to a capacitor and terminated to ground. Standard 0.01 F decoupling capacitors are used on all IC power supply pins (32 total). One 22- F tantalum capacitor is used for power supply bulk decoupling. The circuit board power and ground planes are connected to a centrally located surface mount attach (SMA) connector. Load resistors and SMA connectors are also used to measure shoot-through current.

Stack-Ups

Three different stack-ups were used to fabricate TV1s, as shown in Figure 1-5. As with TV0, the copper planes of the EDC materials served as power and ground planes for each version of TV1.

Stack-up TV1-1-Y is a six-layer circuit board with the power and ground planes located on Layers 3 and 4, respectively.

Stack-up TV1-2-Y is the control stack-up, a six-layer circuit board built only with high Tg FR-4 epoxy materials and power and ground planes located on Layers 2 and 5, respectively.

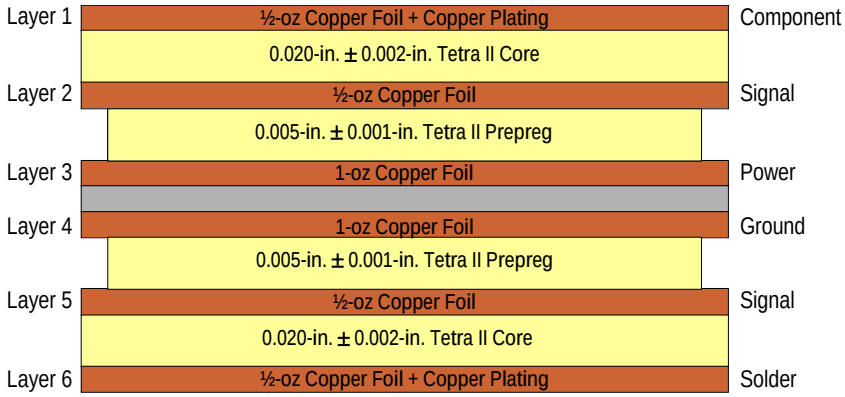
Stack-up TV1-3-Y is a seven-layer circuit board with a power plane on Layer 2, and ground planes located on Layers 3 and 6. Though atypical, the TV1-3-Y stack-up allows investigation of the effects of EDC material placement within a circuit board as well as the effect of shielding the signal layers between planes.

Layouts — Component Placement on TV1 Test Boards

Each of three different board layouts, Figures 1-6, 1-7, and 1-8, corresponds to a different board size. TV1-X-1 was a 1-up circuit board measuring 2 in. x 3 in. TV1-X-4 contained four copies of the 1-up board on a 4.1-in. x 6.1-in. panel area. Although each of the four circuits operated independently, the power and ground planes were solid throughout the panel as if there were only one large board on the panel. Solid planes were also used for TV1-X-12, which contained 12 copies of the 1-up board on an 8.6-in. x 9.3-in. panel area. These layouts allowed for the evaluation of increased circuit board size on embedded capacitance performance.

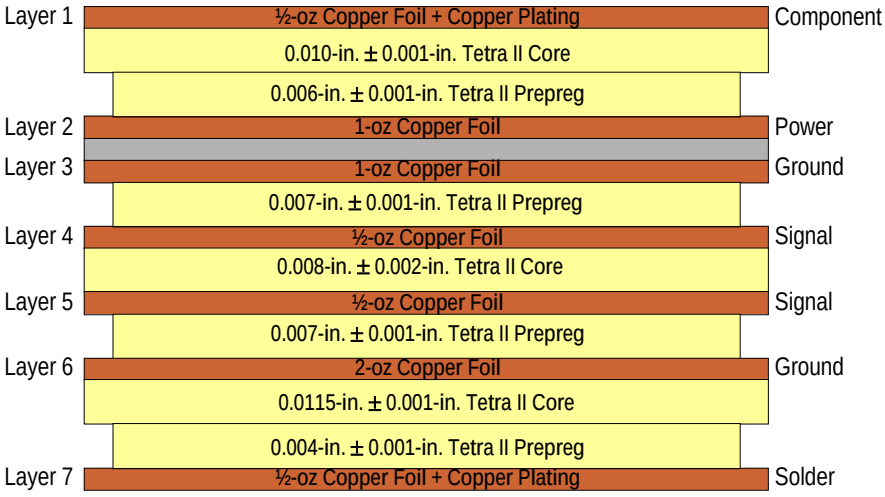
Tests were conducted on bare, partially populated and fully populated test vehicles. Partially populated boards applied only to the TV1-X-4 and TV1-X-12 versions, where only one of the one-up copies was populated with components. Fully populated boards had components placed at every available site.

For each 1-up board or copy on a 4-up or 12-up board, the components placed were an oscillator, a bulk decoupling capacitor, eight ICs, and a number of load capacitors. Components were mounted on the top side and a coaxial SMA connector was mounted on the back side of each TV1 board to measure the voltage on the power and ground planes.



a) TV1-1-Y: Six-layer Stack-up

b) TV1-2-Y: Six-layer Control Stack-up



c) TV1-3-Y: Seven-layer Stack-up

Figure 1-5. TV1 Stack-ups

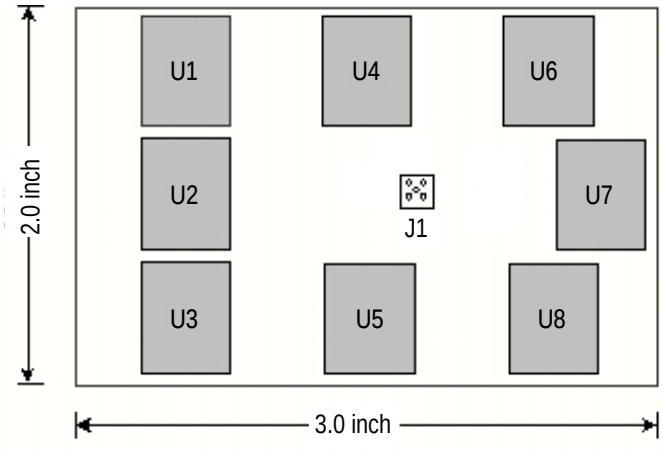


Figure 1-6. TV1-X-1 Layout

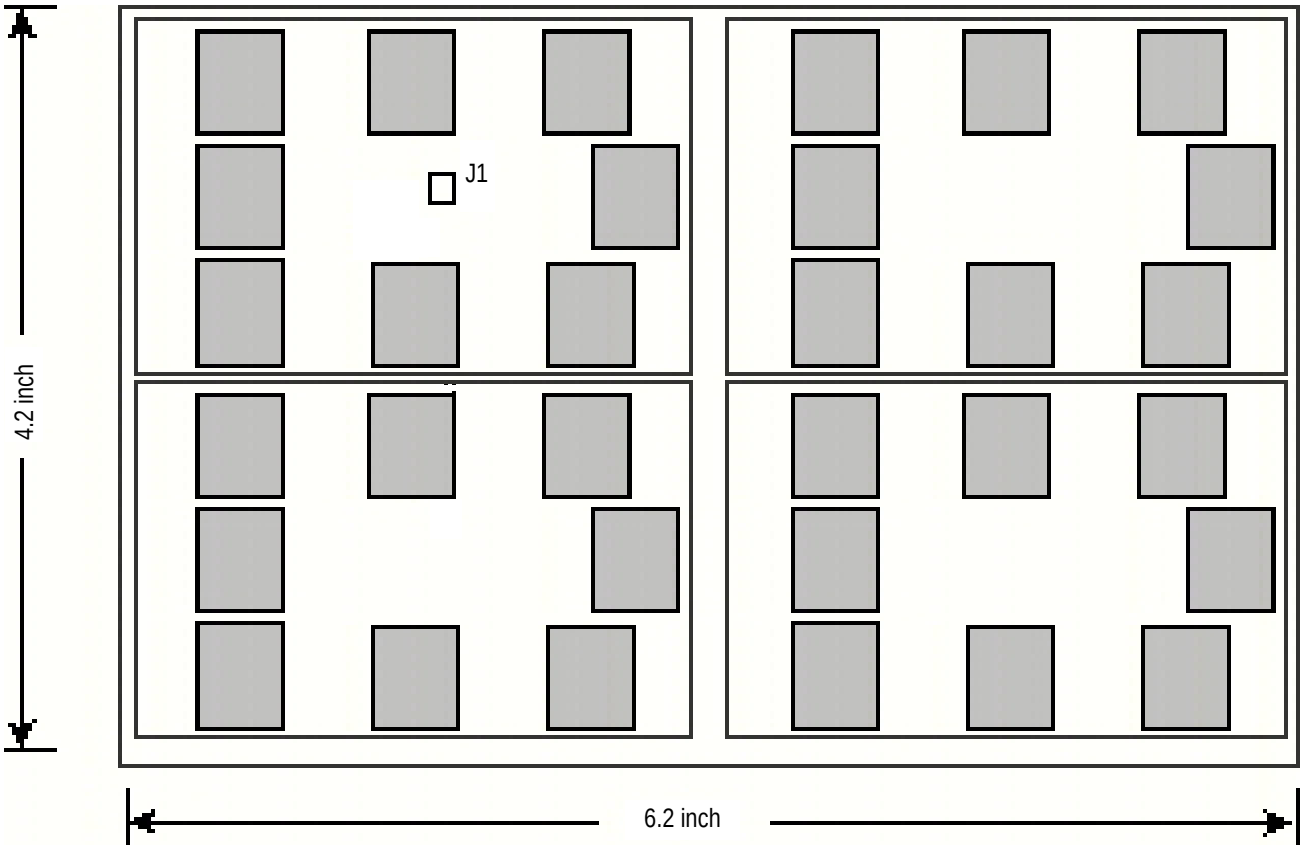


Figure 1-7. TV1-X-4 Layout

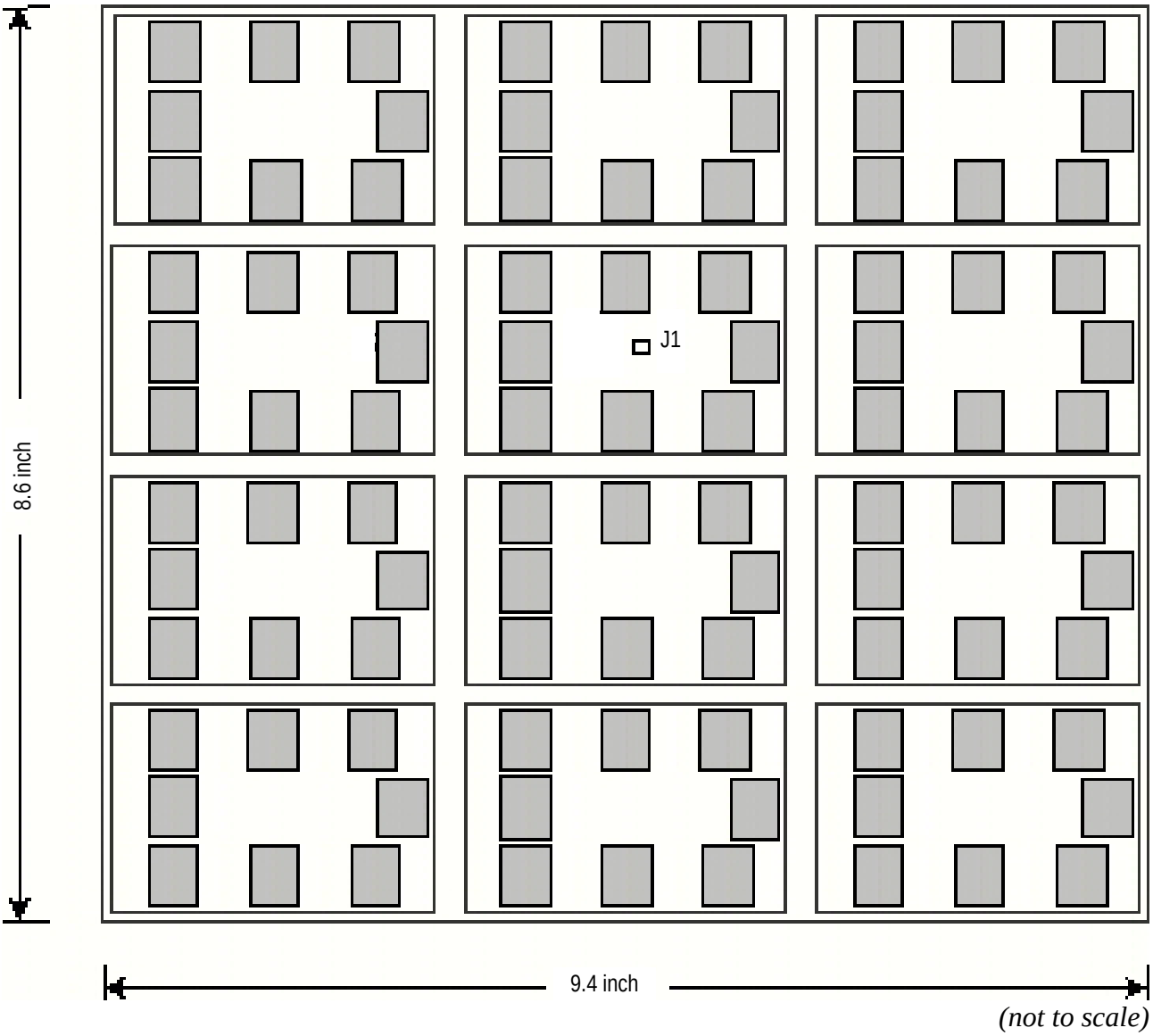


Figure 1-8. TV1-X-12 Layout

Electromagnetic Interference Evaluation

This section presents the results of work performed at StorageTek in Louisville, Colorado. The purpose of the work was to assess the effectiveness of various embedded capacitance materials for power supply decoupling. Two experiments were performed to measure power supply noise (power bus ripple) and radiated emissions using simple test methods. The experimental data and discussion of the results follow.

Power Bus Ripple

Description of Experiment

A 50-MHz oscillator drives an octal clock driver that generates a constant and repeatable square-wave output with a defined period and rise time. The dock driver drives six additional clock drivers that drive a number of capacitive loads to simulate a highly populated printed wiring board (PWB). Thus, high-frequency current is drawn from the power bus, creating a voltage ripple between the power and ground planes. The circuit was powered with a 3.3-V direct current (DC) external power supply.

Although a surface mount attach (SMA) connector was provided for measurement purposes, measurements were first taken using a high-impedance P6246 field-effect transistor (FET) probe for comparison. The data compared very favorably and all test data presented here has been taken using the SMA connector, cable, and a Tektronix TDS754C 500-MHz oscilloscope. Test data was taken on test vehicle 1 (TV1) in the 1-up and 4-up configurations.
Figure 2-1 shows the test equipment configuration for the peak-to-peak voltage measurements.

Figure 2-1. Test Setup for Peak-to-peak Voltage Measurements

Experimental Results

Figure 2-2 shows an example of the data taken for evaluation of the peak-to-peak voltage for the different PWB materials. The value of the reported peak-to-peak measurement is highlighted within the box. Channel 1 data is taken using a coaxial cable connected to an SMA connector on the test vehicle. Channel 2 data was taken using a P6246 high-impedance FET probe for comparison and calibration. As can be seen

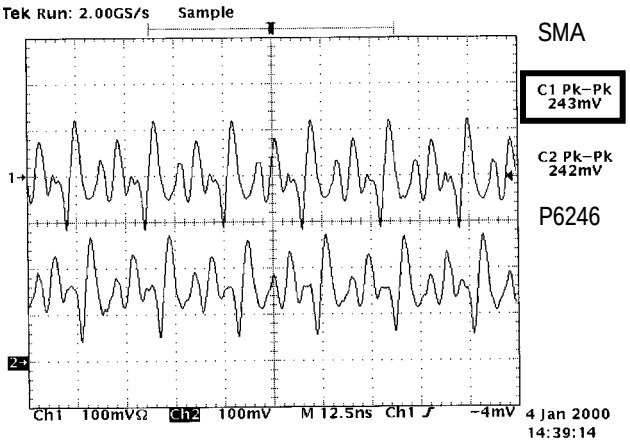


Figure 2-2. Peak-to-peak Ripple Voltage

from the data, the results are identical and all subsequent data was taken using the SMA measurement setup. The full result set is reported and summarized in Figures 2-3 and 2-4. At 50 MHz, the boards are small with respect to a wavelength, so standing waves should not be a factor in the results. The horizontal bar indicates a commonly acceptable threshold limit for power supply noise (i.e., 10% Vcc).

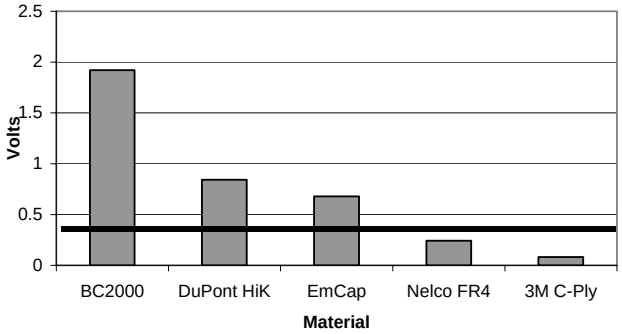


Figure 2-3. Peak-to-peak Voltage Between Vcc and Ground in 1-up Configuration

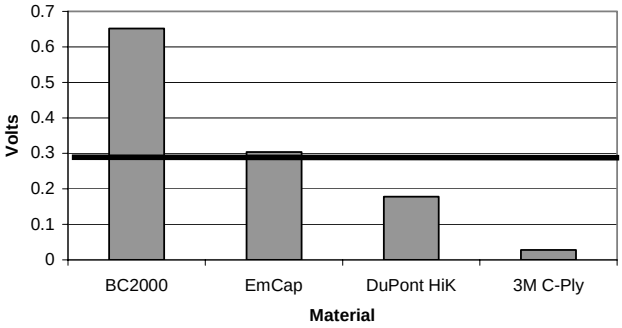


Figure 2-4. Peak-to-peak Voltage Between Vcc and Ground in 4-up Configuration

Results Discussion

An examination of the results reveals some interesting observations:

1. As a general trend, as the capacitance of the board increases, the measured peak-to-peak voltage decreases. This observation is also seen when the data from the 4-up and 1-up boards is compared. As the board physically becomes bigger, the peak-to-peak voltage falls.
2. The 1-up (Nelco) fire retardant grade 4 laminate material (FR-4) with decoupling capacitors had more available capacitance and exhibited lower peak-to-peak voltages than BC2000, HiK, and EmCap. Boards of this size built with BC2000, HiK, and EmCap may require additional decoupling capacitors to meet low-frequency current demands. It should be noted that the test vehicle made from BC2000 materials only had *half* the normal capacitance value, since BC2000 boards are usually built with two embedded capacitance layers. Even so, the BC2000, assuming a linear scaling, would have had the highest voltage in the 1-up case and about the same voltage as EmCap in the 4-up case.
3. The 1-up C-Ply had the lowest peak-to-peak voltage and was a factor of three lower than the benchmark. All C-Ply samples exhibited less than 100 mV of ripple.

Radiated Emissions

Description of Experiment

The evaluation of the radiated emissions performance of these materials presented some unique challenges:

1. The effects of differences in the materials had to be isolated.
2. The experiment had to be simple.
3. There had to be sufficient dynamic range to detect “subtle” changes.

The test setup for this experiment (Figure 2-5) was designed to measure the amount of common-mode current induced on a cable attached to the board. This current is often the dominant source of radiated electromagnetic interference (EMI) from small products at frequencies below a few hundred megahertz. The circuit was powered with a 3.3-V DC power supply via approximately 1 m of coaxial cable, which served as the power source and the attached cable for this measurement. This simple experiment had a number of logistical advantages since it did not require a special test facility (open area test site [OATS], anechoic chamber, etc.) but was performed on a bench top. An F33 5Ω current probe was placed around the coaxial cable and connected to an Anritsu MS2601A Spectrum Analyzer.

Figure 2-5. Test Setup for Common-mode Noise Measurements

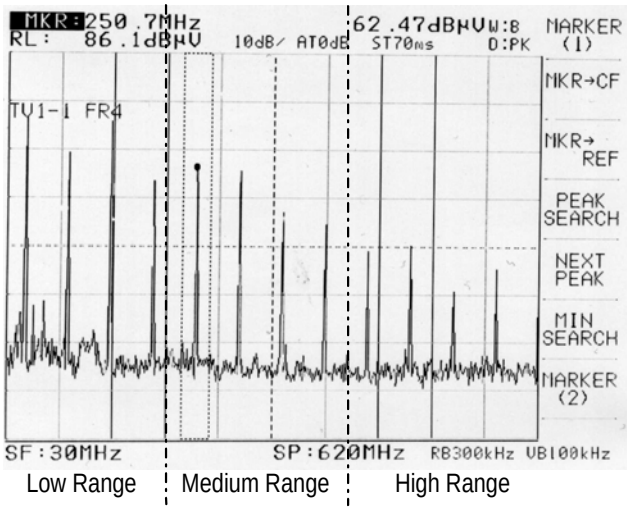


Figure 2-6. Common-mode Noise Swept Response

Experimental Results

Figure 2-6 is an example of the data taken for evaluation of the common-mode current induced by printed wiring boards made with different materials. Each peak corresponds to a harmonic of the basic clock frequency. The measurement bandwidth was 650 MHz, starting at 30 MHz. The data was difficult to interpret in this form, because different boards exhibited resonances at different frequencies. In the end, it was decided to split the frequency band into three regions: low, medium, and high. Then, after calculating the total power, comparisons could be made among the materials, as presented in Figures 2-7 and 2-8.

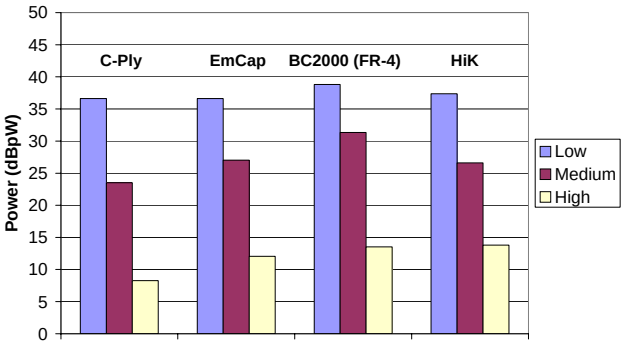


Figure 2-7. Comparison of Common-mode Noise on TV1-1-1 With No Decoupling Capacitors

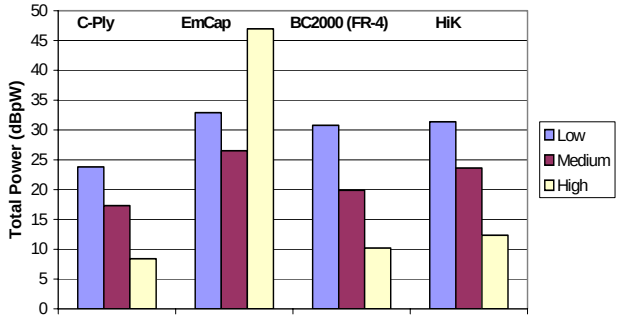


Figure 2-8. Comparison of Common-mode Noise on TV1-4-1 With No Decoupling Capacitors

Results Discussion

An examination of the results reveals some interesting observations:

- Overall, the C-Ply exhibited the best performance.
- In the low range, all materials exhibited similar performance.
- Materials tended to differentiate themselves in the mid to high ranges.
- As the board size increased, emissions levels decreased.
- Dramatic changes in power bus ripple did not affect the emissions profile to the same degree.

Experimental Conclusions

It can be concluded that within the constraints of these experiments, the embedded capacitance materials significantly reduced power supply noise. However, they had little effect on the radiated emissions. The results confirm that reductions in the peak-to-peak voltage between Vcc and ground do not necessarily result in the same level of reduction in radiated emissions. Finally, one of the embedded capacitance materials performed better than test cards with surface-mounted decoupling capacitors.

III. Original Equipment Manufacturers

III. 1 Frequently Asked Questions for Original Equipment Manufacturers: Answers from AMD

Ben Beker received a Ph.D. in electrical Engineering from the University of Illinois at Chicago in 1988. After graduation he spent 12 years on the faculty of the ECE Department at the University of South Carolina working in the areas of millimeter wave integrated circuit and electronic package modeling and analysis. In May of 2000, he joined AMD as a Senior Member of Technical Staff, where he works on the design of microprocessor and chipset packages, specializing in power distribution. ben.beker@amd.com, (tel): 512-602-2904

Current applications with <= .002" P/G cores

Power plane pair impedance control:

- potentially lower dominant ("LC") resonance frequency
- lower Q's of higher order, high-frequency resonances

Improved power plane pair de-coupling:

- increased plane pair capacitance
- lower equivalent series inductance from the power supply to package interconnect
- shorter PTH via length for discrete capacitor connections
- possible reduction of discrete components

Possible reduction of discrete components leads to more routing space in high-density I/O designs

Thinner cores should lead to more P/G plane pairs in the same board thickness:

- lower resistance at the dominant ("LC") resonance
- more plane P/G plane pairs implies lower DC resistance and higher current handling capability

Possibility of extending this technology to thinner cores in organic packages

Any active (very, ultra, extremely) thin core projects?

None at this time

If available, within cost budget, use would be:

Frequent

Schedule; desired time to:

Samples / Engineering / Verification:	Mid 2002
Proto-Circuits:	Late 2002 or early 2003
Volume Circuits:	Late 2003 or early 2004

Future Requirements: Roadmap?

This is cost, volume, and availability driven – none of which are known now.

Utility of Thin Power/Ground Cores in Power Delivery Applications

Benjamin Beker
Advanced Micro Devices, Inc.
5204 E. Ben White Blvd.
Austin, TX 78741

AMD

Thin layers help achieve:

- Power plane pair impedance control:
  - potentially lower dominant (“LC”) resonance frequency from the regulator to package
  - lower Q’s of higher order, high-frequency resonances
- EMI control/reduction
- Improved power plane pair de-coupling:
  - increased plane pair capacitance
  - lower equivalent series inductance from the power supply to package interconnect
  - shorter PTH via length for discrete capacitor connections
  - possible reduction of discrete components

AMD

Thin layers help achieve:

- Possible reduction of discrete components leads to more routing space for signals in high-density I/O designs and cost reduction
- Thinner cores should lead to more P/G plane pairs in the same board thickness:
  - lower resistance at the dominant (“LC”) resonance and within a bandwidth near the resonance
  - more P/G plane pairs in same board thickness implies lower DC resistance and higher current handling capability
  - better current handling capability helps in the design of thermal solution
- Possibility of extending this technology to thinner cores in organic packages

AMD

III. 2 Frequently Asked Questions for Original Equipment Manufacturers: Answers from COMPAQ Computer Corp.

John Grebenkemper, Compaq NonStop Division. Dr. Grebenkemper received a BSEE from Tufts University and MSEE and PhD degrees from Stanford University. He has worked in a number of diverse areas including X-ray and radio astronomy, microwave receiver design, and satellite communications systems. He joined Tandem in 1982, and has managed the Signal Integrity group since 1991. He has published more than a dozen papers and received six patents.
john.grebenkemper@compaq.com, (tel): 408-285-5809

Current applications with <= .002" P/G cores

Key driver(s)	Reducing dI/dt noise on power planes
Nominal dimensions and tolerances	Standard
Benefits	Lower noise on power planes, greater capability of providing transient current requirements, increased high frequency capacitance, faster damping of high frequency power plane noise

Any active (very, ultra, extremely) thin core projects ?

Describe	Loaded dielectrics
Key driver(s)	High capacitance, 10 nF per square inch
Perceived benefits	Increased high frequency capacitance
Constraints to implementation	PWB manufacturing yield loss
Cost budget or tolerance for cost premium	Contingent on board size, assume $100/layer pair
Alternatives	ZBC, Kapton
List desired physical attributes:	High manufacturing yield
List desired electrical attributes:	High capacitance

If available, within cost budget, use would be:

Pervasive, almost all products would use this technology

Schedule; desired time to:

Samples / Engineering / Verification	Immediate
Proto-Circuits	6 months
Volume Circuits	1 year

Future Requirements: Roadmap ?

We will adopt the thin layer technologies that become available and meet the following requirements:

- Available from multiple manufacturers
- Available with no increase in PWB manufacturing times
- Available with no decrease in reliability
- Certified to all safety agency requirements
- Will pay a reasonable price premium

III. 3 Frequently Asked Questions for Original Equipment Manufacturers: Answers from SUN Microsystems, Inc.

Valerie St.Cyr is the Supply Base Development Manager for Printed Circuit Boards and Backplanes for Sun Microsystems. She has been with Sun for 3 years in technology development, new product introduction, and supply chain management roles. Prior to joining Sun, Valerie was with Digital Equipment Corp. for 10 years where she was a Principal Manufacturing Engineer responsible for VAX systems' PCBs, and later the Acquisition Program Manager for Digital's StorageWorks line. Before that Valerie worked in the industry for over 12 years having departmental management responsibility for materials, lamination, mechanical CNC operations, and soldermask. Valerie holds a degree in Business Management and is a Certified Purchasing Manager (National Association of Purchasing Management). valerie.st.cyr@sun.com, (tel): 781-442-0982

Istvan Novak is signal-integrity senior staff engineer at SUN Microsystems, Inc. Besides of signal-integrity verification of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks, bypassing and decoupling of packages and printed-circuit boards for workgroup servers. He creates simulation models, and develops measurement techniques for power-distribution networks. Istvan has more than twenty years of experience with high-speed digital, RF, and analog circuit and system design. He is Fellow of IEEE for his contributions to the signal-integrity and RF measurement and simulation methodologies. Istvan holds a masters degree and PhD in Electrical Engineering. istvan.novak@sun.com, (tel): 781-442-0340

Current applications with <= .002" P/G cores: Yes

Key driver(s): Reducing dI/dt noise on power planes

Nominal dimensions and tolerances: see below

Benefits: Reduced noise across planes due to lower plane inductance,
reduced radiation,
reduced overall board thickness

Any active (very, ultra, extremely) thin core projects? Yes

Describe: Very thin (.001" cores) being tested in current production parts
Ultra Thin (.0003" cores) have very limited engineering part samples
eXtremely Thin (.00003") have lab samples

Key driver(s): same as above

Perceived benefits: same as above, plus
reducing/eliminating plane resonances

Constraints to implementation:
modeling and verification data
availability;
cost (raw materials)
cost (fabricated)

Dielectric Strength (Withstanding Voltage) Requirement?
250V/mil

Cost budget or tolerance for cost premium:
modest cost premium as an early adopter
expecting cost/value parity after not more than 2 yrs.

Alternatives: Use different system partitioning to reduce the amount of high-speed current entering the PCB planes: reduce current/line, reduce number of lines simultaneously switching, increase transition time, divert current from entering PCB planes by using capacitors on silicon and/or package

List desired physical attributes:
large panel form (=> 18 x 24")
copper clad thickness options
thickness range one-sided: thickness not to exceed .001". etc.

List desired electrical attributes:
Low inductance,
resonance-free self-impedance,
low-pass transfer impedance

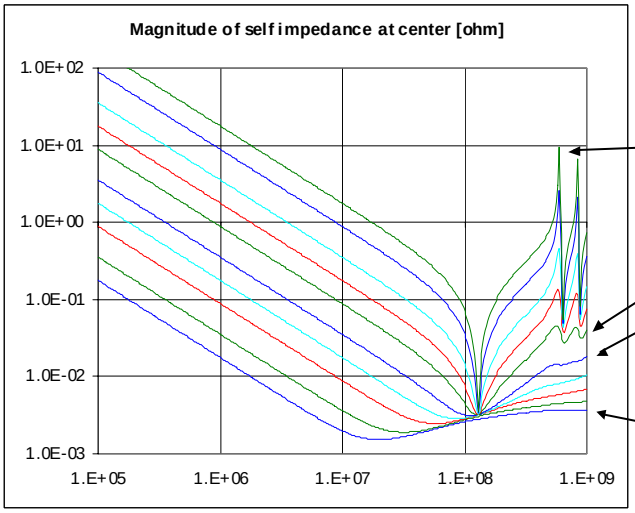
If available, within cost budget, use would be: Pervasive

Schedule; desired time to:	.001"	.0003"
Samples / Eng/ Verification:	Now	Now
Proto-Circuits:	Now	6 - 9 months
Volume Circuits:	6 months	12 - 15 months

Thin Laminate Electrical Benefits

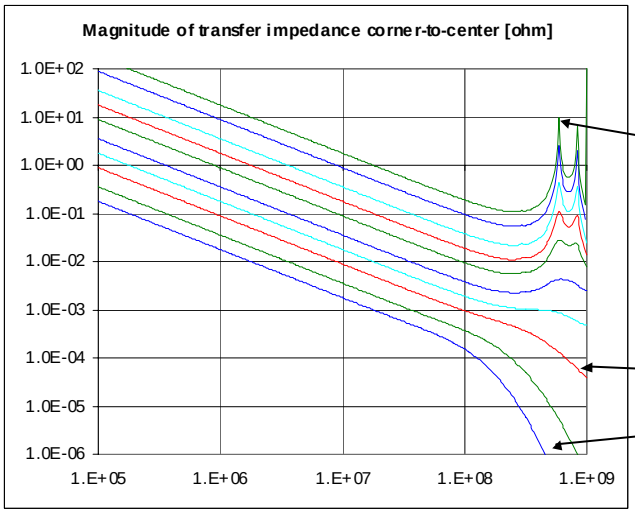
- Inductance (L) is proportional to thickness (t)
- dV=L*dI/dt: SSN is less if L is lower
- Plane resonances are suppressed if t<0.3 mils
- Low-pass noise propagation if t<1um
- Radiation is less from thinner laminates
- Dielectric constant increases static capacitance, but L is unchanged

Resonance-Free Planes for t<0.3mils



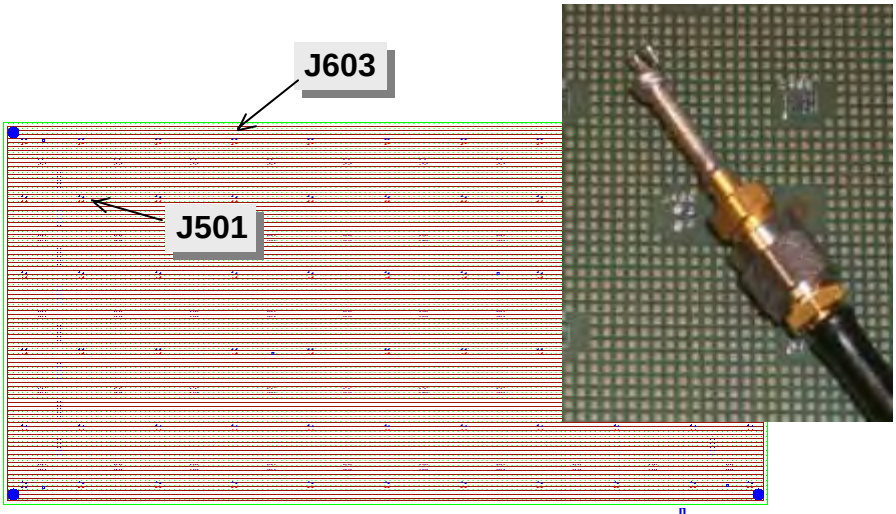
10”x10” planes
Bare board
Simulated, t=
- 10-mil
- 5-mil
- 2-mil
- 1-mil
- 0.5-mil
- 0.2-mil
- 0.1-mil
- 0.05-mil
- 0.02-mil
- 0.01-mil

Low-pass Transfer for t<1um

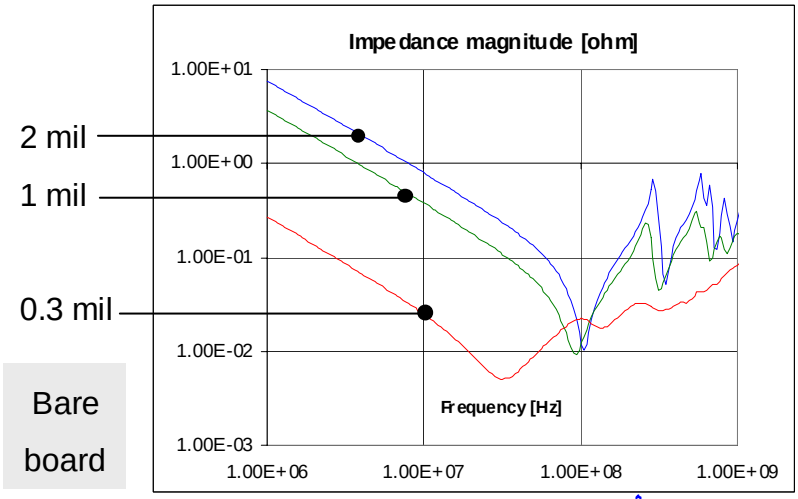


10”x10” planes
Bare board
Simulated, t=
- 10-mil
- 5-mil
- 2-mil
- 1-mil
- 0.5-mil
- 0.2-mil
- 0.1-mil
- 0.05-mil (1.2um)
- 0.02-mil
- 0.01-mil

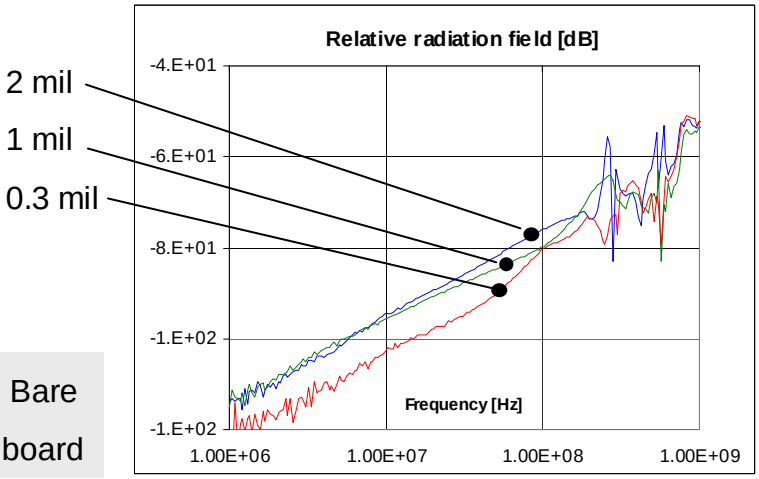
10”x5” Test Board



Measured Self Impedance

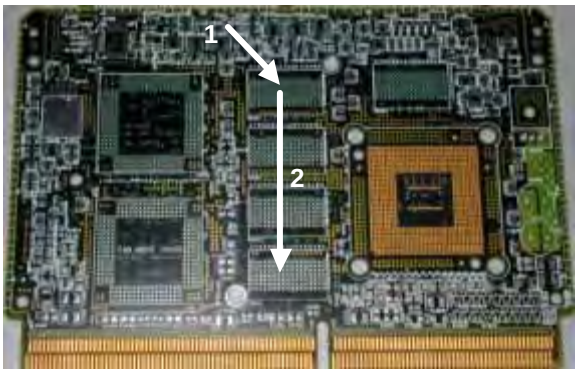


Measured Close-Field Radiation



Impedance on Small Board

Geometry



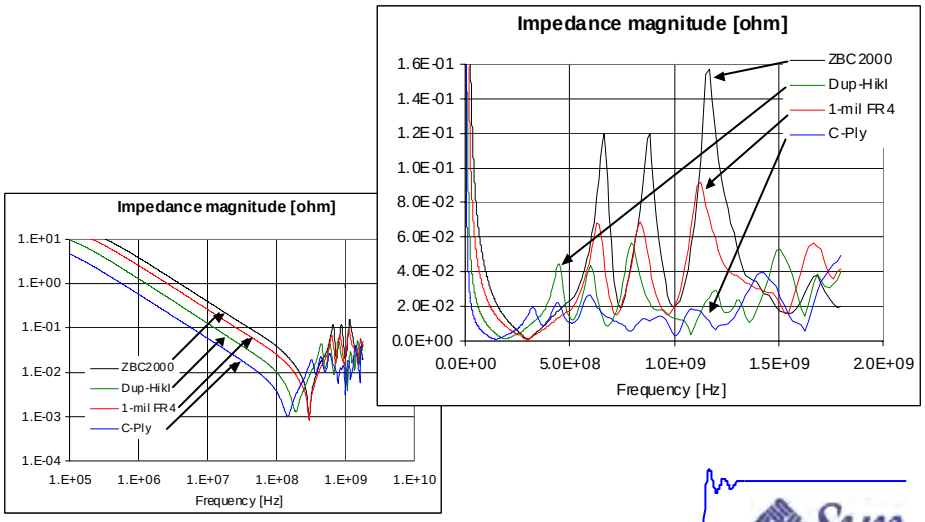
Paralleled plane pairs

Bare board

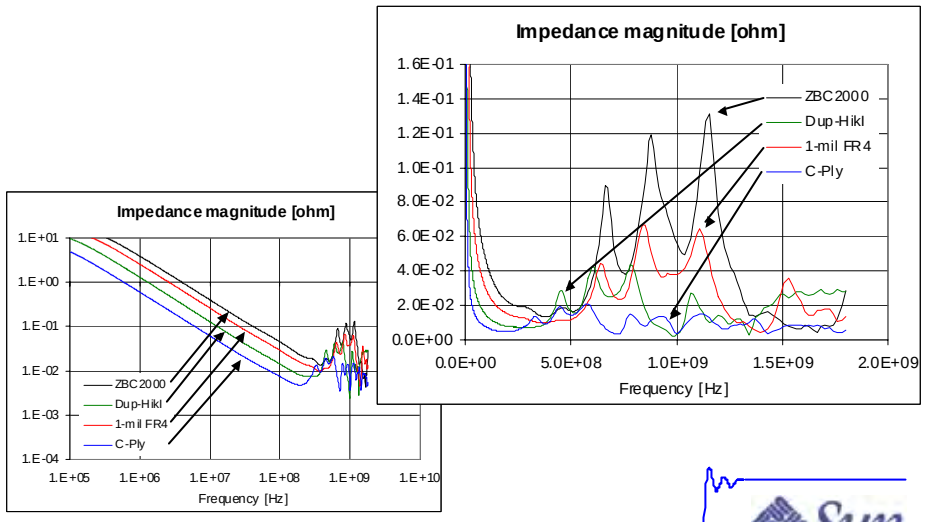
Same construction, with

- Aromat 2-mil FR4 BC2000
- DuPont 1-mil HiK
- Aromat 1-mil FR4
- 3M 0.3-mil C-Ply

Impedance on Small Board
Self-impedance at (1)



Impedance on Small Board
Transfer-impedance (2)



III. 4 Frequently Asked Questions for Original Equipment Manufacturers: Answers from Nortel

Rob Sheffield, Member of scientific staff at Nortel Networks, been with Nortel for 35 years. He has always been associated with the technology group providing a materials perspective to the electronics groups. Much of his time has been spent addressing the issues of level 2 and level 3 packaging along with electrical and optical interconnect. Rob has been team leader on the NIST AEPT consortium for the last 3 years investigating the potential of embedded passives. Rob graduated from Reason University in metallurgy. chefbrd@nortelnetworks.com

Current applications with <= .002" P/G cores	Yes
Key driver(s)	Speed
Nominal dimensions and tolerances	50 microns @+/- 20%
Benefits	Possibly cost, lower parasitics

Any active (very, ultra, extremely) thin core projects? Yes

Describe	NIST AEPT Program
Key driver(s)	Speed and cost
Perceived benefits	Lower induction lower total capacitance required
Constraints to implementation	Supplier availability
Dielectric Strength (Withstanding Voltage) Requirement?	50 Volts
Cost budget or tolerance for cost premium	Break even or better
Alternatives	non evident
List desired physical attributes:	Defect free Peel strength > 4 lbs/in. Tg >180 deg. C Warp < 0.005"/inch. Compatible with FR4 fabrication Withstand lead free solder temp. 280 deg. C < 1 micron rms surface roughness

List desired electrical attributes:

Frequency Capability 20GHz
<3.0 db total path loss
<-12 db return loss
Zo Variation Total system +/-5%
< 0.001 loss tangent
< 3 low K (Er) for delay
> 20 High K (Er) for High capacitance density
30 pF to 10 μF capacitance range
(Ranked not necessarily in importance of above listed attributes)

If available, within cost budget, use would be: Frequent

Schedule; desired time to:

Samples / Engineering / Verification	Now
Proto-Circuits	3-6 months
Volume Circuits	Mid to end of 2002

Future Requirements: Roadmap?

We would like to see an increase in the capacitance density for the future running at speed up to 40 GHz. Lead free assembly and components will be a must so that the assembly temperatures will increase. The most popular solder for replacement of Pb/Sn is a Sn/Cu/Ag eutectic.

IV. Material Suppliers

IV.1 Frequently Asked Questions for Original Equipment Manufacturers: Answers from DuPont iTechnologies

David R. McGregor received a Bachelor of Science degree in Mechanical Engineering from North Carolina State University in Raleigh, North Carolina and joined DuPont in 1974. Before moving into DuPont's electronics business unit in 1983, he held a variety of positions in process engineering, product development, and quality control in the fields of Dacron® polyester, and Chromium Dioxide magnetic tape manufacture. Within the electronics business unit Dave has worked on equipment design and process and product development, making use of statistically designed experiments. He has been involved with product development of solder mask and primary imaging photoresists. He is currently development team leader for DuPont's embedded planar capacitor laminate materials.
david.r.mcgregor@usa.dupont.com, (tel): 919-248-5064

DuPont Very Thin Laminates

Attributes	**Interra™ HK 9**
• Physical	• 25 micron thick ceramic filled polyimide dielectric. • ED Copper thicknesses: 0.5 ounce - typical. 1.0 ounce - typical. Any weight ≤ 1.0 ounce. • Thickness uniformity, % +/- 5 • Peel strength, nominal 6 pli • Tensile Strength MD, MPa 105 • Tensile Strength TD, MPa 95 • Elongation MD, % 18 • Elongation TD, % 11 • Elastic modulus, MPa 4700 • Moisture absorption, % 1
• Electrical	• Dielectric Constant 9 • Capacitance Density, pF/in^2 2,000 • Dissipation Factor, 1 MHz 0.01 • Breakdown Voltage, V/mil 2800 • Surface resistivity, ohm/square E14 • Volume resistivity, ohm-cm E14
Experience	
• Volumes run to date	• 200,000 ft^2.
• Yield data	• Insufficient data.

• Lessons learned	• No significant difference from standard polyimide manufacturing. • DuPont has vast experience manufacturing filled polyimide films. • All systems are in place to manufacture and supply - well established supply chain. • Can be imaged double sided and is compatible with PWB processes. • Applicable for both rigid and flex designs. • Fabricators in each of the 3 major geographical regions have successfully built boards.
• Obstacles to implementation	• Fabricator experience with processing very thin laminates. • OEM reluctance to test and implement. • Lack of standards for embedded passives.
Key schedule milestones	
	• Third large scale confirmation run completed - December '01. • Qualified applications - now.

Availability; Time to:	
• Samples	• Available now.
• Small runs	• Available now.
• Volume	• 1 Q 02
Anticipated cost per square foot (delivered price to PCB fabricator)	
• Near future	• < $\$15/ft^2$, volume dependent.
• Intermediate	• Volume dependent.
• Long term	• Volume dependent.
Reliability Testing Results (materials)	
	• Stable capacitance with frequency - 100 Hz to 15 GHz • Stable capacitance and loss tangent with temperature - 30 to 180°C • Through-hole reliability equal to FR-4. • Stable capacitance during thermal cycling, -55 to 125°C
Agency or regulatory approvals	
• UL 94V-0	• Complete.
• UL 746 E	• Pending

Attributes	Interra™ HK 4 - 25
• Physical	• 25 micron thick polyimide dielectric. • ED Copper thickness range: 0.25 ounce - 3.0 ounce. • Thickness uniformity, % +/- 10 • Peel strength, nominal > 8 pli • Tensile Strength, MPa > 345 • Elongation, % > 50 • Elastic Modulus, MPa 4800 • Glass Transition (Tg), C 195 • Moisture absorption, % 0.8
• Electrical	• Dielectric Constant 3.5 • Capacitance Density, 1 MHz pF/in^2 800 • Dissipation Factor, 1 MHz 0.003 • Breakdown Voltage, V/mil 6000 • Surface Resistance, ohm/square > E16 • Volume Resistivity, ohm-cm E16
Experience	
• Volumes run to date	• Sufficient.
• Yield data	• Acceptable - commercial, full scale product.
• Lessons learned	• No significant difference from standard polyimide manufacturing. • All systems are in place to manufacture and supply - well established supply chain. • Double sided imaging and compatible with PWB processes - very robust. • Applicable for both rigid and flex designs.
• Obstacles to implementation	• Fabricator experience with processing very thin laminates. • OEM reluctance to test and implement. • Lack of standards for embedded passives.
Key schedule milestones	
	• Qualified applications - now.
Availability; Time to:	
• Samples	• Available now.
• Small runs	• Available now.
• Volume	• Available now.
Anticipated cost per square foot (delivered price to PCB fabricator)	
• Near future	• < $10, volume dependent.
• Intermediate	• Volume dependent.
• Long term	• Volume dependent.

Reliability Testing Results (materials)	
	• Stable dielectric constant and loss tangent with frequency - 1 MHz to 10 GHz • Highly stable in thermal aging, thermal cycling and temperature/humidity testing.
Agency or regulatory approvals	
• UL 94V-0	• Complete.
• UL 746 E	• Complete.

Attributes	Interra™ HK 4 - 18
• Physical	• 18 micron thick polyimide dielectric. • ED Copper thickness range: 0.25 ounce - 3.0 ounce. • Thickness uniformity, % +/- 10
• Electrical	• Dielectric Constant 3.5 • Capacitance Density, 1 MHz pF/in^2 1,100 • Dissipation Factor, 1 MHz 0.003 • Breakdown Voltage, V/mil 3600
Experience	
• Volumes run to date	• 25,000 ft^2.
• Yield data	• Insufficient data.
• Lessons learned	• No significant difference from standard polyimide manufacturing. • All systems are in place to manufacture and supply - well established supply chain. • Double sided imaging and compatible with PWB processes - very robust. • Applicable for both rigid and flex designs.
• Obstacles to implementation	• Fabricator experience with processing very thin laminates. • OEM reluctance to test and implement. • Lack of standards for embedded passives.
Key schedule milestones	• Evaluation programs - now.
Availability; Time to:	
• Samples	• Available now.
• Small runs	• 1 Q 02.
• Volume	• 2 Q 02.
Anticipated cost per square foot (delivered price to PCB fabricator)	
• Near future	• Volume dependent.
• Intermediate	• Volume dependent.
• Long term	• Volume dependent.
Reliability Testing Results (materials)	
	• Anticipated to be equal to Interra™ HK 4 - 25
Agency or regulatory approvals	
• UL 94V-0	• Pending.
• UL 746 E	• Pending.

Attributes	Interra™ HK 4 - 12
• Physical	• 12 micron thick polyimide dielectric. • ED Copper thickness range: 0.5 ounce - 2.0 ounce. • Thickness uniformity, % +/- 10
• Electrical	• Anticipated to be equal to HK 4 - 18.
Experience	
• Volumes run to date	• Limited.
• Yield data	• Insufficient data.
• Lessons learned	• No significant difficulty anticipated in making thin polyimide film. • All systems are in place to manufacture and supply - well established supply chain.
• Obstacles to implementation	• Fabricator experience with processing very thin laminates. • OEM reluctance to test and implement. • Lack of standards for embedded passives.
Key schedule milestones	
	• Demonstrate robust production - 2 Q 02. • Complete UL testing - 2 Q 02.
Availability; Time to:	
• Samples	• 1 Q 02.
• Small runs	• 2 Q 02.
• Volume	• 3 Q 02.
Anticipated cost per square foot (delivered price to PCB fabricator)	
• Near future	• Volume dependent.
• Intermediate	• Volume dependent.
• Long term	• Volume dependent.
Reliability Testing Results (materials)	
	• Anticipated to be equal to Interra™ HK 4 - 18
Agency or regulatory approvals	
• UL 94V-0	• To be tested.
• UL 746 E	• To be tested.

Attributes	Interra™ HK X - 8
• Physical	• 8 micron thick ceramic filled polyimide dielectric. • ED Copper thickness range: 0.5 ounce - 2.0 ounce. • Thickness uniformity, % +/- 10
• Electrical	• Dielectric Constant 25 - 35 • Capacitance Density, 1MHz pF/in^2 18,100 - 25,400 • Breakdown Voltage, V/mil > 100
Experience	
• Volumes run to date	• Limited.
• Yield data	• Insufficient data.
• Lessons learned	• Coating very thin films with low defect density is challenging.
• Obstacles to implementation	• Need to demonstrate ability to scale up manufacturing. • Fabricator experience with processing very thin laminates. • OEM reluctance to test and implement. • Lack of standards for embedded passives.
Key schedule milestones	
	• Demonstrate reliable manufacturing - 4 Q 02.
Availability; Time to:	
• Samples	• 3 Q 02.
• Small runs	• 4 Q 02.
• Volume	• 2 Q 03
Anticipated cost per square foot (delivered price to PCB fabricator)	
• Near future	
• Intermediate	
• Long term	
Reliability Testing Results (materials)	
Agency or regulatory approvals	
• UL 94V-0	
• UL 746 E	

IV. 2 Frequently Asked Questions for Printed Circuit Board fabricators: Answers from 3M

Joel S. Peiffer received his B.S. in Materials Science from the University of Minnesota in 1982 and has been employed by 3M since 1990. In that time he has worked for 3M's Electronic Products Division in Columbia, MO in the manufacture of high density flexible circuitry and for the last 5 years, in the Optoelectronic Packaging Systems Technology Center developing embedded capacitance materials. Previous to 3M, Joel was employed by Digital Equipment, Century Circuits, Hutchinson Technology and Buckbee-Mears Company. In these positions he was responsible for the manufacture of rigid, rigid-flex and flex circuitry, electroplating and photochemical milling.
jspeiffer@mmm.com, (tel): 651-575-1464

Describe thin core product

Physical:

Dielectric Material: Epoxy loaded with barium titanate
Dielectric Thickness: 8 um (0.3 mils) (standard)
Dielectric Thickness Uniformity: 10%
Copper Thickness: 35 um (1.4 mils) (standard)
Copper Thickness Uniformity: 5%
Material Width: Up to 18.5 inches

Electrical:

Capacitance/Unit Area: 10 nF/in^2 +/- 10% (25C/1 kHz)
Dissipation Factor: 0.005 (25C/1 kHz)
Frequency: >5 GHz
Breakdown Voltage: >50 Volts
DC Leakage Current: <10 $nanoamps/in^2$ (at ≤15V)
Operating Temperature: -40C – 125C ("X7R" behavior over this range)

Experience

Volumes run to date: Pilot Scale

Yield data: Not Optimized (Pre-Commercial)

Lessons learned: Proprietary

Obstacles to implementation:

Design tools, simulation ability, major OEM qualification, regulatory (UL) qualification, established test standards and PCB processes

Key schedule milestones

Availability; Time to:

Samples for Engineering/Verification: Currently available

Small runs: Based on sample feedback and completion of business model

Volume: Based on sample feedback and completion of business model

Anticipated cost per square foot (delivered price to PCB fabricator)

Near future, Intermediate, Longer term: Business model to be determined

Reliability testing results (materials):

Tests Performed on C-Ply Printed Circuit Boards:

ENVIRONMENTAL/RELIABILITY

Thermal Shock/Thermal Cycle
Elevated Temperature and/or Humidity*
Temp, Humidity, Bias (THB)*
ESD

ADHESION

Multiple Solder Reflow
Solder Shock/Solder Stress
TMA 260C
Mechanical (Bend Test)

No significant issues with any of the above tests

*(C-Ply is epoxy based and absorbs a low level of water similar to FR-4 materials)

Agency or regulatory approvals:

Necessary: UL Recognition at laminate level for flammability and maximum operating temperature (MOT)

Complete: Testing for flammability (V-0 results); Testing for Provisional MOT (~130C test results)

Formal UL recognition: Flammability - Q1 2002; Final MOT - Q2 2002

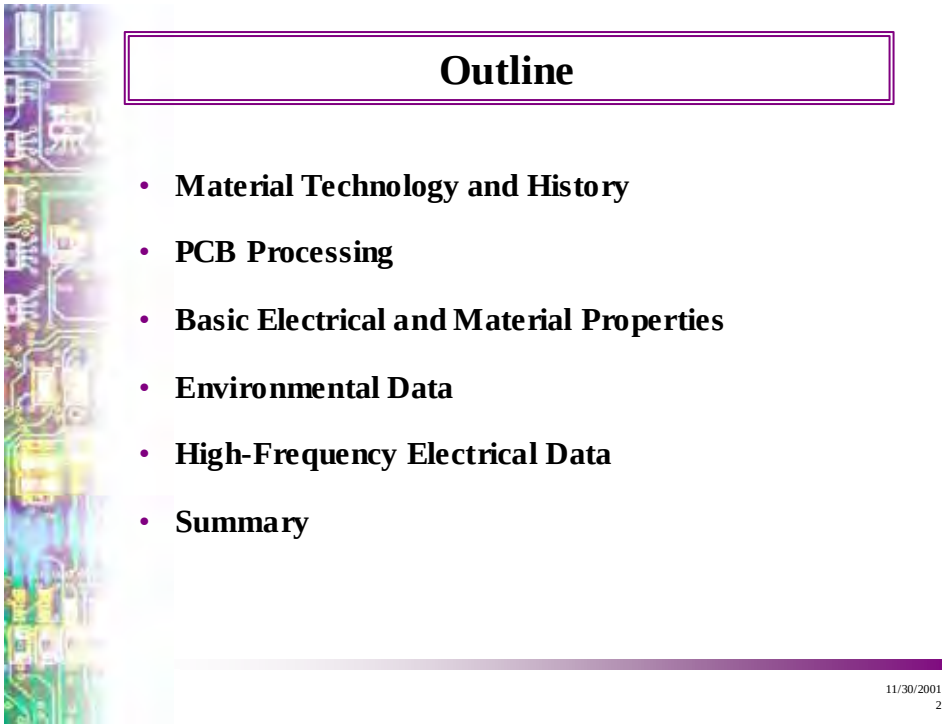
3M Embedded Capacitor Material

This presentation will focus on the advantages of embedded capacitor materials and in particular, the advantages of 3M's embedded capacitor material.

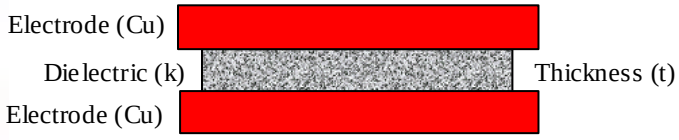
The benefits of embedding a capacitor layer into a printed circuit board or other electronic package are: 1) increased packaging density (or correspondingly a decrease in size and/or number of layers); 2) improved electrical performance (lower power bus noise and EMI) due to lower inductance; and 3) improved reliability due to a reduction in solder joints. When the above benefits are coupled with a reduction in the costs of the capacitors and their placement, the overall goal of a more reliable, better performing, cost-effective capacitor material should be the result.

3M's embedded capacitor material (3M C-Ply) consists of an epoxy/ceramic dielectric sandwiched between two layers of copper. The dielectric is solution coated very thin (for high capacitance) on copper foil (typically 1.4 mil in thickness). The coating is done in a high-speed roll-to-roll process. Two sheets of coated material are then laminated (dielectric-to-dielectric) to produce the final product.

The embedded capacitor material properties include high capacitance (10 – 20 nF/in^2), low loss, an operating frequency of at least 5 gigahertz and an operating temperature of up to ~125C ("X7R" behavior over this range). It has been successfully incorporated into printed circuit boards (rigid and flex) and can be easily incorporated into other electronic packages. It has been found to be compatible with all PCB processing including laser ablation. It has been shown to greatly reduce power bus noise, much better than discrete decoupling capacitors or existing embedded capacitor materials. It has also been shown to reduce EMI.



Thin-Film Capacitor Technology



- Capacitance per unit area (C/A) is proportional to k and inversely proportional to t
- 3M uses a very thin layer (<25 microns) of a precision coated loaded polymer
- Vary C/A by varying thickness (t)

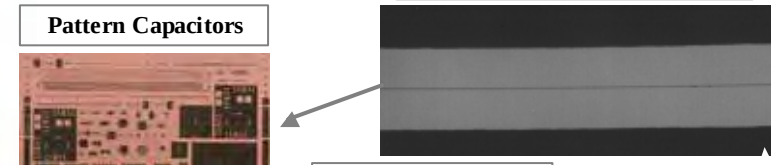
History of Embedded Capacitors at 3M

- **1996 - 1999** **DARPA Program**
- **1998 - 2000** **NCMS Embedded Decoupling Capacitance (EDC)**
- **1999 -** **NIST ATP Embedded Passives**

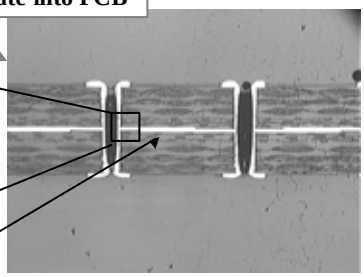
PCB Processing

Supply panels up to 18.5” wide

Pattern Capacitors



Laminate into PCB



C-Ply layer

Board Cross Section

Material Property Goals

Attribute	8 micron
Capacitance/area	10 nF/in^2
Adhesion (1” peel)	>4 lbs.
T260 Life	>5 mins.
Dielectric Constant	16
Freq., Volt., Temp.	meet X7R
Dielectric Strength	~130 V/μm
Breakdown	>50 V
Tolerances	10%
Copper Thickness	35 μm

Focus is currently on an 8 micron dielectric although other thickness’ can be produced

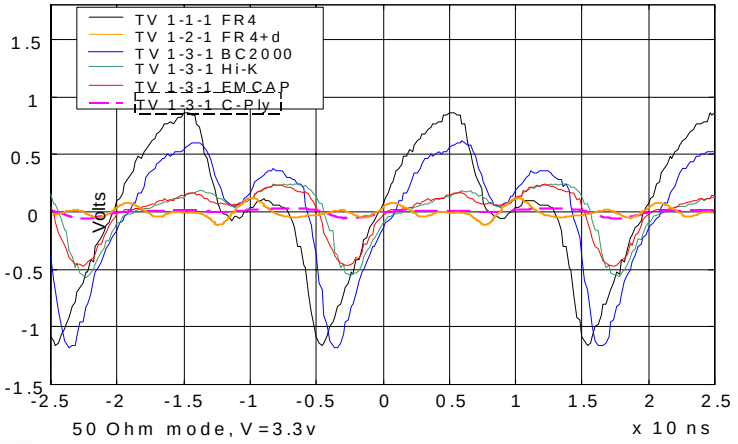
Environmental Testing

Test	Property	Change
High Temp (125°C)	Capacitance	No Change (1000 hrs)
Thermal Cycle	Capacitance	No Change (1000 cycles)
High Humidity (85°C/85% RH)	Capacitance Dissipation Factor	5-15% Increase* 0.4% to 0.9%*
TMA (T260)	Life	>5 minutes**
THB	Life	>1000 hrs (15 V)
ESD	Short Capacitance	None No Change
UL Approval	Various	In Process

***Returned to pre-test level after 125C bake**

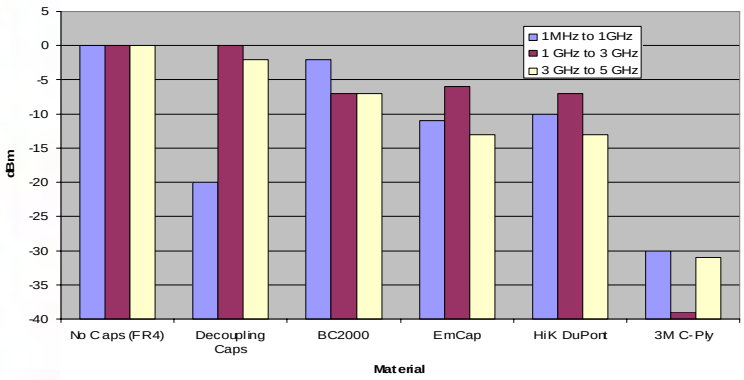
Power Bus Noise (UMR data)

(Time Domain - 50 MHz)



Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

Power Bus Noise on Test Vehicle (UMR)



- **Traditional decoupling capacitors are not effective at frequencies above 1 GHz**
- **C-Ply layer has excellent performance to 5 GHz**

Data from NCMS Embedded Decoupling Capacitance Project Report - 12/00

3M Embedded Capacitor Material

- **Builds on the experience and interaction gained from three industry consortia (DARPA, EDC and AEPT)**
- **Performs well as a distributed power/ground layer, also can produce singulated and isolated capacitors**
- **Passes basic environmental tests**
- **Cost effective for high component density, high speed, and size constrained designs**

V. PCB fabricators

V.1 Frequently Asked Questions for Printed Circuit Board Fabricators: Answers from Sanmina Corporation

James Howard is an Electrical Engineer who has spent 25 years in the field of printed circuit board engineering management, process development, and most recently research and development. In conjunction with Greg Lucas, James patented the technologies of Buried Capacitance, Annular embedded passive components, and capacitively coupled circuits. He currently resides in Carson City Nevada and is a Principal Research Engineer for Sanmina Corporation of Santa Clara California.
jim.howard@sanmiba.com, (tel): 408-557-7010

Current production with <= .002" P/G cores

High volume: Sanmina typically ships several million dollars of internally produced product per month in BC coded sales. Additional thin laminate material is processed for non Buried Capacitance use as well.

Describe "typical" product from above

Typical Sanmina Product :
14 layer to 50 layer
.062 thickness and above
50mm pitch BGA
Lead Counts 1140 up to 1657
high percentage of special surface finish
DataCom industry based product

Any current (very, ultra) thin core projects?

Full scale implementation of .001 core Buried Capacitance material in production.

Customer driven requirement for electrical properties.

Requirements
Fully glass supported .001 layer to be integrated as power & ground plane sandwiches within PCB.

Key schedule milestones
2000 Hour Reliability Testing Completed
Sanmina UL Approval – 2/4/02
Electrical Properties Characterization 1/21/02
Laminate Manufacturer Approval Feb 4, 2002

Experience

Equipment (DES, AOI, ET, etc. ..)

In Place

All Equipment is currently in place to run .001" material in P/G configurations with reasonable yields, at multiple facilities.

Volumes run to date:

14 test lots up to finished board status. Lots were 6 layer to 8 layer test vehicles.

Yield data

Yields equivalent to standard ZBC-2000 processing yields on .001" supported cores.

Lessons learned

1) Hi Pot test at 250V rather than 500.
2) Dimensional Stability is predictable, within the range of standard supported materials.
3) Processing is equivalent to standard ZBC-2000 material processing, with some additional handling constraints.

Obstacles to implementation

Complete UL and electrical categorization testing.
Telcordia Recognition.

Anticipated cost to implement (as a percentage of current P/G layer cost, e.g; 2.5X)

At present, approx. 1.5X material cost of standard ZBC-2000 material. Cost of material could decrease as production quantities increase.

Reliability testing results (PCBs)

Passed 2000 Hour 85%RH/85℃ Test, at 50V DC.

Agency or regulatory approvals

Necessary

UL Recognition in Progress.
Telcordia Recognition.

Complete

Laminate Supplier UL Recognized.

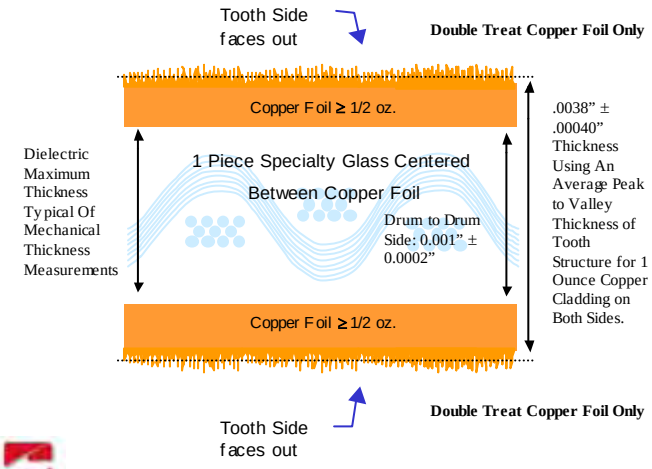
1 Mil Buried Capacitance Material

- **In development for the past 2 years.**
- **Material Parameters:**
  - **Hi Tg. (170ºC) FR-4 Based Resin with specialty glass reinforcement.**
  - **Latest lots holding at 0.001" ± 0.0001" dielectric thickness.**
  - **Peel strengths 7.0 – 7.5 lb/in.**
  - **Flammability Rating: 94-V0**
  - **Projected Capacitance: ≥ 1000 pFd/in^2**
  - **2000 Hr Reliability Testing Completed.**
    - **85%RH/85ºC – 50V DC.**

SANMINA

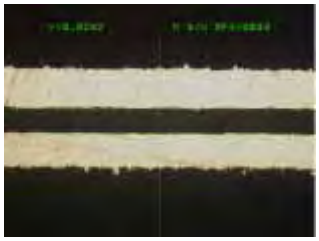
1 Mil Buried Capacitance Material

- Construction Details:

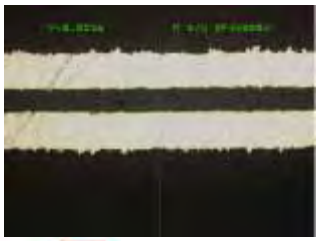


SANMINA

1 Mil Buried Capacitance Material



Measurements in mm.
Thickness is 0.99 mils.



Measurements in mm.
Thickness is 0.93 mils.

SANMINA

HADCO Santa Clara, Inc., Subsidiary

Material Introduction Timeline

Milestone	Target Date
Determine UL Requirements	Complete
Produce UL Test Samples	Complete
Ship to UL	Complete
Receive UL Approval	Feb 4, 2002
Material Testing (In House)	
Determine/Tool Test Vehicle	Complete
Build Test Layers	Complete
Build Test Parts	At Soldermask
Complete Electrical/Initial Reliability Tests	Jan 17, 2002
Issue Conditional Approval	Jan 21, 2002
Introduce to Market	Jan 21, 2002
Volume Testing Complete	May 8, 2002

SANMINA

HADCO Santa Clara, Inc., Subsidiary

Processing Considerations

- Processes on Equipment capable of running 2 mil dielectric material.
  - ♦ May require leadering at Develop/Etch/Strip.
  - ♦ Handling Concerns.
- Yields through Process and Hi Pot are equivalent to 2 mil ZBC-2000® material.
- Cost is approx 1.5 – 2X the cost of 2 mil ZBC-2000® material.
- Scale factors are predictable and within the range of glass supported thin laminates.

SANMINA

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General Expressions of Radial Transmission Line Equations

By Franz Gisin PhD., Sanmina Corporation

Here are the general expressions for a radial transmission line structure (e.g. BC). Solution to both are Hankel functions which get a bit messy sometimes. Once we solve them, however, we can use this to model the "effective capacitance" of BC by modeling BC as a "charged transmission line" with a dynamic load attached. On the flip side, we can also us the same solution to model the losses as a function of separation distance between the planes, different dielectric materials (e.g. loss tangent, etc.) as well as get a handle on SSO and PCB edge resonaces (e.g. how good is that edge plating anyway, etc.).

$$0 = \frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} - \gamma_c^2 V \qquad 0 = \frac{d^2I}{dr^2} - \frac{1}{r}\frac{dI}{dr} - \gamma_c^2 I$$

$$\gamma_c^2 = \left[(R' + j\omega L')(G' + j\omega C') \right]$$

$$R' = \frac{1}{\pi r t \sigma_c} \qquad G' = \frac{2\pi r \sigma_d}{d} \qquad C' = \frac{2\pi r \varepsilon_d}{d} \qquad L' = \frac{\mu d}{2\pi r}$$

Deriving Radial Transmission Line *R'L'G'C'* Values

The per unit element values for series resistance, *R'*, series inductance, *L'*, shunt conductance, *G'*, and shunt capacitance, *C'*, are computed in the following sections. Figure 1 graphically shows a radial transmission line cross section where *a* = disk inner radius, *b* = disk outer radius, *t* = copper thickness, and *d* = dielectric thickness. The cylindrical coordinate system is used, with radial distance, *r*, angle, ϕ, and height, *z*.

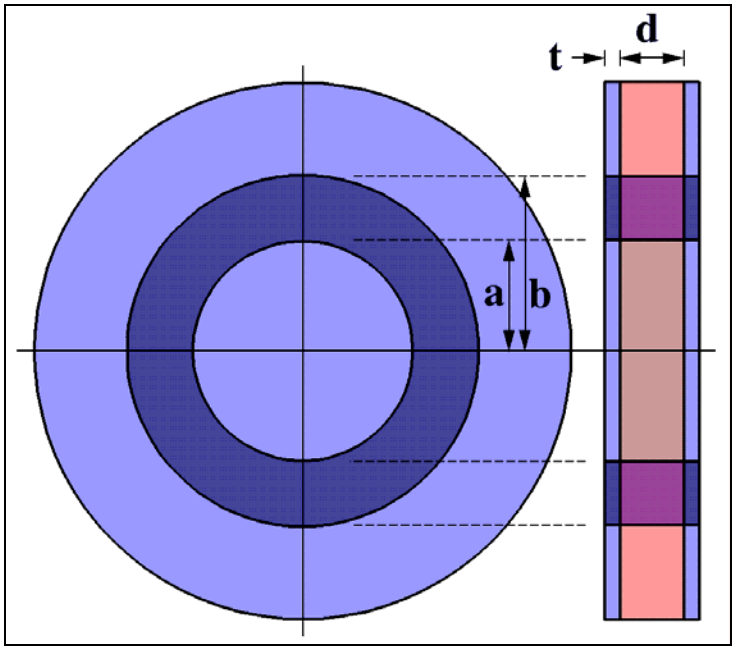


Figure 1: Radial Transmission Line Cross Section

Series Resistance, *R*

The transmission line eqivalent series resistance, *R*, of the metal planes of thickness, *t*, can be found by first applying a voltage, V_0, across the curved surfaces at radius *a* and *b*, and then finding the voltage, *V*, inside the cross section using Laplace's equation. As we shall see later on, the actual value of V_0 is not important, and so we can arbitrarily set the voltage $V_{r=a} = 0$, and $V_{r=b} = V_0$. By assuming the inner radius, $a > 0$, we can solve for *V* by multiplying Laplaces's equation through by *r*, and then integrating twice.

$$\nabla^2 V = \frac{1}{r}\frac{d}{dr}\left(r\frac{dV}{dr}\right) = 0 \quad \Rightarrow \quad \frac{d}{dr}\left(r\frac{dV}{dr}\right) = 0$$

$$\int \frac{d}{dr}\left(r\frac{dV}{dr}\right)dr = r\frac{dV}{dr} + A \quad \Rightarrow \frac{dV}{dr} = \frac{A}{r}$$

$$V = \int \frac{A}{r}dr = A\ln r + B$$

The constants of integration, *A* and *B* can be found as follows.

$$V_{r=a} = A\ln a + B \quad \Rightarrow \quad B = -A\ln a$$

$$V_{r=b} = V_0 = A\ln b + B = A\ln b - A\ln a = A\ln\frac{b}{a} \quad \Rightarrow \quad A = \frac{V_0}{\ln\frac{b}{a}}$$

Once we have found the constants of integration *A* and **B** we can find *V*.

$$V = A\ln r - A\ln a = A\ln\frac{r}{a} = \frac{V_0}{\ln\frac{b}{a}}\ln\frac{r}{a}$$

Next we find the electric field, **E** inside the disk from *V*.

$$\mathbf{E} = -\nabla V = \frac{dV}{dr}\mathbf{a_r} = -\frac{1}{r}\frac{V_0}{\ln\frac{b}{a}}\mathbf{a_r} = \frac{V_0}{r\ln\frac{b}{a}}\mathbf{a_r}$$

Once we found E, we can compute the current through the disk as follows.

$$\mathbf{J} = \sigma_c\mathbf{E} \quad d\mathbf{S} = -rd\phi dz\mathbf{a_r}$$

$$I = \int \mathbf{J}\cdot d\mathbf{S} = \int_{\phi=0}^{\phi=2\pi}\int_{z=0}^{z=t}\frac{\sigma_c V_0}{r\ln\frac{b}{a}}rdzd\phi = \int_{\phi=0}^{\phi=2\pi}\int_{z=0}^{z=t}\frac{\sigma_c V_0}{\ln\frac{b}{a}}dzd\phi$$

$$= \int_{\phi=0}^{\phi=2\pi}\frac{\sigma_c t V_0}{\ln\frac{b}{a}}d\phi = \frac{2\pi\sigma_c t V_0}{\ln\frac{b}{a}}$$

Now that we know V and I, we can find R from Ohms law.

$$R = \frac{V_0}{I} = \frac{1}{2\pi t\sigma_c}\ln\left(\frac{b}{a}\right)$$

Note that at very high frequencies, the thickness, *t*, is equal to the skin depth, δ.

To find the per-unit length series resistance, *R'* (Ω/m) at radial distance, *r*, we let $a = r$, $b = r + \Delta r$.

$$R = \frac{1}{2\pi t\sigma_c}\ln\left(\frac{b}{a}\right) = \frac{1}{2\pi t\sigma_c}\ln\left(\frac{r+\Delta r}{r}\right) = \frac{1}{2\pi t\sigma_c}\ln\left(1+\frac{\Delta r}{r}\right)$$

$$\ln\left(1+\frac{\Delta r}{r}\right)\Big|_{-1<\frac{\Delta r}{r}\le+1} = \left[\frac{\Delta r}{r} - \frac{1}{2}\left(\frac{\Delta r}{r}\right)^2 + \frac{1}{3}\left(\frac{\Delta r}{r}\right)^3 + \ldots\right] \approx \frac{\Delta r}{r}$$

$$R \approx \frac{1}{2\pi t\sigma_c}\frac{\Delta r}{r} \qquad R' = 2\frac{R}{\Delta r} = \frac{1}{\pi r t\sigma_c}\ \Omega/\text{m}$$

Note that the equivalent series resistance, *R'*, is equal to the sum of the resistances in both the power and ground planes, and hence *R' = 2R*.

Shunt Conductance, *G*

The shunt conductance, G, is a bit easier to derive, since the two surfaces, *z = t* and *z = t + d*, are parallel to each other and hence the electric field and current density are uniform in cross section. In this case, the resistance across a disk of dielectric having inner radius *r = a*, and outer radius, *r = b*, can be derived as follows.

$$A = A_{r=b} - A_{r=a} = \left(\pi b^2 - \pi a^2\right)$$

$$G = \frac{1}{R_d} = \frac{\sigma_d}{d}A = \frac{\sigma}{d}\left(\pi b^2 - \pi a^2\right) = \frac{\sigma_d\pi}{d}\left(b^2 - a^2\right)$$

To compute the per-unit length conductance, *G'*, at radial distance, r, we let a = r - $\Delta r/2$, and b = r + $\Delta r/2$.

$$G = \frac{\sigma_d\pi}{d}\left(b^2 - a^2\right)$$

$$= \frac{\sigma_d\pi}{d}\left(\left(r+\frac{\Delta r}{2}\right)^2 - \left(r-\frac{\Delta r}{2}\right)^2\right)$$

$$= \frac{\sigma_d\pi}{d}\left(\left(r^2 + 2r\frac{\Delta r}{2} + \frac{\Delta r^2}{2}\right) - \left(r^2 - 2r\frac{\Delta r}{2} + \frac{\Delta r^2}{2}\right)\right)$$

$$G = \frac{\sigma_d\pi}{d}2r\Delta r = \frac{2\pi r\sigma_d}{d}\Delta r \quad \Rightarrow \quad G' = \frac{G}{\Delta r} = \frac{2\pi r\sigma_d}{d}\ \text{S/m}$$

Shunt Capacitance, *C'*

Like the shunt conductance, the shunt capacitance can be readily found since the power and ground surfaces are parallel to each other. Following the same strategy as was used to find *G'*, we can derive *C'*.

$$A = A_{r=b} - A_{r=a} = \left(\pi b^2 - \pi a^2\right)$$

$$C = \frac{\varepsilon_d}{d} A = \frac{\varepsilon_d}{d}\left(\pi b^2 - \pi a^2\right) = \frac{\varepsilon_d \pi}{d}\left(b^2 - a^2\right) = \frac{\varepsilon_d \pi}{d} 2r\Delta r$$

$$C' = \frac{C}{\Delta r} = \frac{2\pi r \varepsilon_d}{d}$$

Note that the derived value for the capacitance assumes fringing fields at the edges of the planes can be neglected. In most cases, the thickness, *d*, is much smaller than the maximum dimension of the planes, and hence this assumption is valid.

Series Inductance, *L'*

The easiest way to find the inductance is to first compute the magnetic energy, *W*, stored in the dielectric region between the two power and ground disks. As was the case for computing the series resistance, we can arbitrarily define a current, I_0, that passes across the disks. In this case, we can define a sheet current density, **K**, in terms of the current, I_0, and then turn around and find the magnetic field, **H**. Once we know H, we can compute the energy, and from the energy we can compute the inductance.

$$\mathbf{K} = \frac{I_0}{2\pi r}\mathbf{a_r} \qquad \mathbf{H} = \mathbf{K} \times \mathbf{a_n} = \frac{I_0}{2\pi r}\mathbf{a_r} \times \mathbf{a_z} = \frac{I_0}{2\pi r}\mathbf{a_\varphi}$$

$$W = \frac{1}{2}\int \mu H^2 dv = \frac{1}{2}\int_{\phi=0}^{\phi=2\pi}\int_{z=0}^{z=d}\int_{r=a}^{r=b} \mu\left(\frac{I_0}{2\pi r}\right)^2 r dr d\phi dz$$

$$= \frac{\mu I_0^2}{8\pi^2}\int_{\phi=0}^{\phi=2\pi}\int_{z=0}^{z=d}\int_{r=a}^{r=b} \frac{1}{r} dr d\phi dz = \frac{\mu I_0^2}{8\pi^2} 2\pi d \ln\frac{b}{a} = \frac{\mu d I_0^2}{4\pi}\ln\frac{b}{a}$$

From the total energy we can compute the inductance as follows

$$W = \frac{\mu d I_0^2}{4\pi}\ln\frac{b}{a} = \frac{1}{2} L I_0^2 \quad \Rightarrow \quad L = \frac{2W_{\text{total}}}{I_0^2} = \frac{\mu d}{2\pi}\ln\frac{b}{a}$$

Using the same approximation for **ln** (see section where *R'* was derived) we arrive at the per-unit length inductance as follows

$$L = \frac{2W_{\text{total}}}{I_0^2} = \frac{\mu d}{2\pi}\ln\frac{b}{a} = \frac{\mu d}{2\pi}\frac{\Delta r}{r} \quad \Rightarrow \quad L' = \frac{L}{\Delta r} = \frac{\mu d}{2\pi r}$$

Telegrapher's Equations for Radial R'L'G'C' Transmission Line Structures

Using time harmonic phasor notation, the equation for the voltage drop across the series resistance, *R'*, and series inductance, *L'*, and the current through the shunt conductance, *G'*, and capacitance, *C'*, can be computed as follows.

$$-\frac{dV}{dr} = \left[R'(r) + j\omega L'(r)\right] I \qquad -\frac{dI}{dr} = \left[G'(r) + j\omega C'(r)\right] V$$

$$= \left[\frac{2Z_S}{2\pi r} + \frac{j\omega\mu d}{2\pi r}\right] I \qquad = \left[\frac{2\pi r\sigma_d}{d} + \frac{j\omega 2\pi r\varepsilon_d}{d}\right] V$$

$$= \frac{1}{r}\left[\frac{2Z_S}{2\pi} + \frac{j\omega\mu d}{2\pi}\right] I \qquad = r\left[\frac{2\pi\sigma_d}{d} + \frac{j\omega 2\pi\varepsilon_d}{d}\right] V$$

$$-\frac{dV}{dr} = \frac{1}{r}(A) I \qquad -\frac{dI}{dr} = rBV$$

$$\frac{dV}{dr} = \frac{1}{r}(-A) I \quad \Rightarrow \quad I = r\left(-\frac{1}{A}\right)\frac{dV}{dr} \qquad \frac{dI}{dr} = -rBV \quad \Rightarrow \quad V = \frac{1}{r}\left(-\frac{1}{B}\right)\frac{dI}{dr}$$

From these two expressions, we can derive a second order differential equation for the voltages within transmission line structure.

$$\frac{d}{dr}\left[\frac{dV}{dr}\right] = \frac{d}{dr}\left[\frac{1}{r}(-A) I\right]$$

$$\frac{d^2V}{dr^2} = -\frac{1}{r^2}(-A) I + \frac{1}{r}(-A)\frac{dI}{dr}$$

$$= -\frac{1}{r^2}(-A) r\left(-\frac{1}{A}\right)\frac{dV}{dr} + \frac{1}{r}(-A)(-rBV)$$

$$\frac{d^2V}{dr^2} = -\frac{1}{r}\frac{dV}{dr} + ABV$$

$$0 = \frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} - ABV$$

$$= \frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} - \left[r(R' + j\omega L')\right]\left[\frac{1}{r}(G' + j\omega C')\right] V$$

$$= \frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} - \left[(R' + j\omega L')(G' + j\omega C')\right] V$$

$$0 = \frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} - \gamma_c^2 V$$

Substituting $\gamma = j\gamma_c$, we arrive at the voltage equation.

$$0 = \frac{d^2V}{dr^2} + \frac{1}{r}\frac{dV}{dr} + \gamma^2 V \qquad \gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')}$$

In a similar fashion, we can find the current equation.

$$\frac{d}{dr}\left[\frac{dI}{dr}\right] = \frac{d}{dr}\left[-rBV\right]$$

$$\frac{d^2I}{dr^2} = -BV - rB\frac{dV}{dr}$$

$$= -B\frac{1}{r}\left(-\frac{1}{B}\right)\frac{dI}{dr} - rB\frac{1}{r}(A)I$$

$$= \frac{1}{r}\frac{dI}{dr} + ABI$$

$$0 = \frac{d^2I}{dr^2} - \frac{1}{r}\frac{dI}{dr} - ABI$$

$$0 = \frac{d^2I}{dr^2} - \frac{1}{r}\frac{dI}{dr} - \gamma_c^2 I$$

V.2 Frequently Asked Questions for Printed Circuit Board Fabricators: Answers from Merix Corporation

Bob Greenlee
Job Title and Current Responsibilities: Advanced Development Engineer, responsible for process development of the embedded resistor and capacitor materials used in the NIST AEPT Consortium.
Educational Background: 1995 M.S. in Chemical Engineering from Washington State University
Work Experience: 1995 – 2001: Process Engineer, Quality Engineer, and Advanced Development Engineer at Merix Corporation. bobg@merix.com

Processing thin core capacitor materials can be challenging, particularly those with a non-reinforced dielectric that is less than 1 mil thick. Several process steps require special attention to ensure the material is not damaged during manufacturing. Material storage and loading systems, conveyor systems, and lamination systems must be capable of handling thin core material. Equipment modifications or special fixtures may be required to reduce the risk of jam-ups or fractured material. Special attention to cleanliness and the documentation of careful handling practices are also important. This presentation will review some of the lessons we have learned about processing thin core material from our participation in the NIST Advanced Embedded Passives Technology consortium.

Current production with <= .002" P/G cores

- Considerable production, increasing demand.

Describe "typical" product from above:

- Twelve to thirty layer boards, ~0.093" thick.
- Typically with 1 mm pitch ASIC packages.
- 500 - 1500+ leads.

Any current (very, ultra) thin core projects?

- NIST Advanced Embedded Passives Technology (AEPT) consortium test boards.
- Emulator board (also includes buried resistor layer) for the AEPT project.
- Sun Microsystems test boards.
- Prototypes for other OEMs.
- UL qualification boards for C-Ply.

Describe:

- Projects are both customer driven and independent development.
- Requirements are from one to four embedded capacitor cores and four to twenty-two layers.
- Key schedule milestones depend on customer requirements.

Experience:

a. Equipment:

- Pre-Clean: in place, required modification.
- Laminator: in place, required modification.
- Print: in place.
- DES: in place.
- Hi-Pot: in place, required modification.
- PEP: in place, required modification.
- AOI: in place.
- Lamination: in place.
- Electrical Test: in place, required modification.

b. Volumes run to date

- We have processed ~1600 ft^2 of C-Ply to date.

c. Yield data

- Yields of a pilot board are running ~ 75%.
- Yield issues include:

- Handling Damage.
- Hi-Pot Failure.
- Registration related to scaling and layer shift.
- Power to Ground Shorts.

- Yields are steadily improving.

d. Lessons learned

- Equipment with thin core capability is vital.
- Training in thin core handling is key.
- Two approaches to etching thin core:
- Standard etching (etch both sides at the same time).
- Sequential etching (etch only one side, laminate into subpart, then etch second side).

Standard etching:

- Border Modifications:
- No overlapping etched features.
- Full copper out to panel edge.
- No overlapping innerlayer vents.
- Potential Problems:
- Laminate tearing along edge.
- Particle generation.
- Loss of tooling hole integrity.

Sequential etching:

- Process Modifications:
- Image and etch first side of material.
- Laminate into a subpart.
- Image and etch second side of material.
- Potential Problems:
- Registration of second side image to first side.
- Subpart registration to parent part.
- Subparts are more prone to epoxy spots that can create shorts.

Challenges to implementation

- Equipment capable of handling thin core.
- Technician training on thin core handling.
- Defect density of the material.
- Material movement during lamination.

Anticipated cost to implement (as a percentage of current P/G layer cost, e.g; 2.5X):

- This information is proprietary.

Reliability testing results (PCBs)

- NIST AEPT consortium results and supplier test data are encouraging.

Agency or regulatory approvals

- Pursuing UL qualification:
- Working with 3M on laminate qualification.
- Beginning board level qualification.
- Developing IPC standards for embedded passives:
- Material specification.
- Board performance specification.
- Design specification.

Processing Thin Core Capacitor Material

This work was performed under support of the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program, Cooperative Agreement Number 70NANB8H4025

Current Production with ≤ 2 mil P/G Cores

- Considerable production, increasing demand.
- Twelve to thirty layer boards, ~0.093” thick.
- Typically with 1 mm pitch ASIC packages.
- 500 - 1500+ leads.

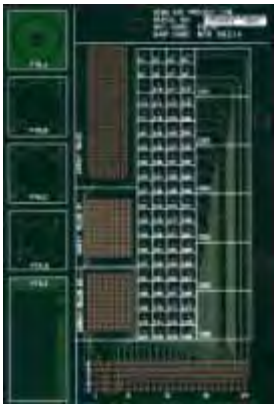
Thin Core Projects
3M C-Ply

- 3M C-Ply used to build boards for:
  - NIST Advanced Embedded Passives Technology (AEPT) consortium test boards.
  - Emulator board (also includes buried resistor layer) for the AEPT project.
  - Sun Microsystems test boards.
  - Prototypes for other OEMs
  - UL qualification boards for 3M

Thin Core Projects
AEPT Test Boards

- TV1-C Testing:
  - **Temperature/humidity**
  - **Thermal cycle**
  - **Thermal shock**
  - **ESD**
  - **Other testing**

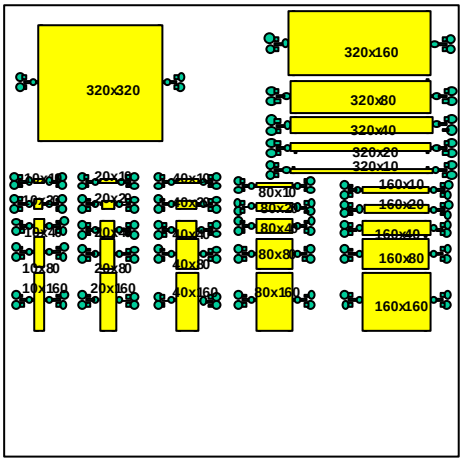
Pictorial view of the TV-1 Capacitor Design.
- 80 X 0.170 sq." Capacitors
- 6 X 0.60 sq." Capacitors
- 5 X NIST Capacitor patterns
- 3 X Daisy chain array capacitors



Thin Core Projects
AEPT Test Boards

- TV2-C high frequency (>5 GHz) test board

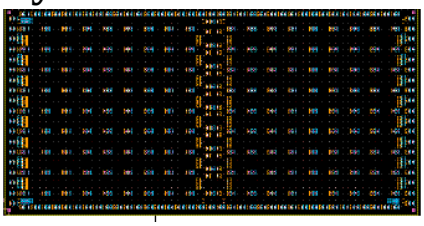
Pictorial view of the TV-2 Capacitor Design.
8 Layers
2 C-Ply cores
Microvias



Thin Core Projects
Nortel Emulator Board

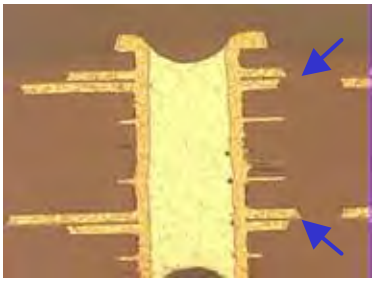
- **14 Layers**
- **4 C-Ply cores**
- **1 Embedded resistor layer**
- **Microvias**
- **Emulates existing high-speed board with buried components.**

Current Thin Core Projects
Sun Microsystems Test Boards

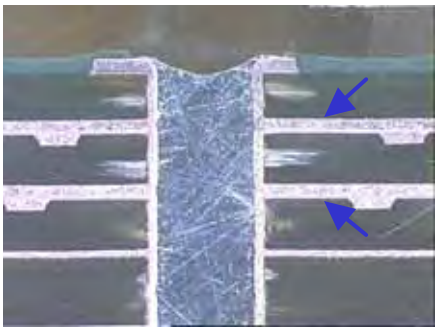


- **20 Layers**
- **4 C-Ply cores**
- **Microvias**
- **Provided impedance and EMI data**
- **Also built with 1 mil FR4.**

C-Ply cores separated by regular core.



Current Thin Core Projects
Prototypes for other OEMs



Adjacent C-Ply cores.

Single C-Ply core in center.

Thin Core Experience: Equipment

- Pre-Clean: in place, required modification.
- Laminator: in place, required modification.
- Print: in place.
- DES: in place.
- Hi-Pot: in place, required modification.
- PEP: in place, required modification.
- AOI: in place.
- Lamination: in place.
- Electrical Test: in place

Thin Core Experience: Volumes & Yields

- We have processed ~1600 ft^2 of C-Ply to date.
- Yields of a pilot board are running ~75%.
- Yield issues include:
  - Handling Damage.
  - Hi-Pot Failure.
  - Registration related to scaling.
  - Power to Ground Shorts.
- Yields are steadily improving.

Thin Core Experience: Lessons Learned

- Equipment with thin core capability is vital.
- Training in thin core handling is key.
- Two approaches to etching thin core:
  - Standard etching (etch both sides at the same time).
  - Sequential etching (etch only one side, laminate into subpart, then etch second side.

Thin Core Experience: Standard Etching

- Border Modifications:
  - No overlapping etched features.
  - Full copper out to panel edge.
  - No overlapping innerlayer vents.

- Potential Problems:
  - Laminate tearing along edge.
  - Particle generation.
  - Loss of tooling hole integrity.

Thin Core Experience: Sequential Etching

- **Process Modifications:**
  - **Image and etch first side of material.**
  - **Laminate into a subpart.**
  - **Image and etch second side of material.**
- **Potential Problems:**
  - **Registration of second side image to first side.**
  - **Subpart registration to parent part.**
  - **Subparts are more prone to epoxy spots that can create shorts.**

Thin Core Experience: Challenges to Implementation

- **Equipment capable of handling thin core.**
- **Technician training on thin core handling.**
- **Defect density of the material.**
- **Material movement during lamination.**

UL Qualification and IPC Standards

- **Pursuing UL qualification:**
  - **Working with 3M on laminate qualification.**
  - **Beginning board level qualification.**
- **Developing IPC standards for embedded passives:**
  - **Material specification.**
  - **Board performance specification.**
  - **Design specification.**

V.3 Frequently Asked Questions for Printed Circuit Board Fabricators: Answers from WUS Printed Circuit Co. Ltd.

Kang Hsu, Chairman of WUS Printed Circuit Co., Ltd. Dr. Hsu joined WUS in 1988. He served as vice President and Chief Marketing officer prior to his current roll with WUS. Before his work at WUS, Dr. Hsu held a variety of engineering, research and management positions at Hughes Aircraft and Battelle Memorial Institutes. He also founded M-Flex, a well known flex circuit manufacturer. He is an author or co-author of 14 technical papers in Chemistry, Computer database application, and PCB fabrications.

Current production with <= .002" P/G cores

No production volume with <= .002" P/G cores, R&D projects only.
We have production experiences with 50um "dielectric" HDI boards. There are 2 HDI processes at WUS:

1. Conventional RCC process: Typical thickness is about 50um +/- 15%.
2. Liquid epoxy process: Typical thickness is about 50um +/- 15% (thin); and minimum thickness can be 25um +/- 15% (very thin).

We have "some" production with liquid epoxy process, and "high volume" production with RCC HDI process.

Describe "typical" product from above (e.g; # layers; BGA ?? mm pitch / ?? leads; thickness …)

1. Conventional RCC: We have several RCC products on high volume production, mostly for communication applications, board thickness is around 0.8mm to 1.2mm. Dielectric thickness is restrained by material vendor's capability. For mass production, the thinest dielectric thickness is 50um. Classified as "thin".
2. Liquid epoxy: Pilot production run; also for communication applications. We can fabricate various thickness requirements as specified by customer, from 25um up to 75um.The process flow compared to RCC is longer, however it can achieve "very thin" requirement and provides better performance on both signal integrity and impedance.

Any current (very, ultra) thin core projects ?

No thin laminate core projects. But we have many projects which liquid type of dielectric materials are utilized to achieve very thin dielectric thickness. These projects are customer driven.

Requirements: In order to achieve lighter, thinner, and smaller for 3C electronic products, PCB design should also change. With reduction in PCB real estate, conventional PTH process is not enough, HDI is a solution . HDI microvias incorporated into thinner dielectric design provide several advantages: lower impedance, reducing parasitic inductance, enhancing signal integrity... These benefit high-speed products.

Key schedule milestones:
WUS Technology Roadmap:

Liquid epoxy: Under pilot run in 2001-2002. Mass production in 2003.
Low Dk and Df materials: Mass production in 2002.
Improve dielectric thickness tolerance from +/-15% down-to +/- 10%.

.

Experience

Obstacles to implementation

We have all equipment in place except Roller Coater.
Roller Coater is scheduled to be in by the end of this year. Once Roller Coater is in place, we're ready for mass production.

Two major issues for now:

Lack of mass production experience.
Dielectric strength of materials is not as good as we anticipated. We're working with material vendors to make improvement.

Anticipated cost to implement (as a percentage of current P/G layer cost, e.g; 2.5X)

Comparing cost of different materials as following:
Highest <=====> Cheapest
Ink material E-> Ink material D-> Ink material C-> Core material A
Core material B: Not available from material vendor yet.

Reliability testing results (PCBs)

Peel Strength Tests, Thermal Shock(288C Floating, and 260C Dipping), Hipot Test, for all materials.

Peel strength

Table below shows the peel strength measurement data:

	A	B	C	D	E
Max:lb/in^2	6.8	4.8	6.9	2.4	3.2
Min:lb/in^2	6	4.16	6.6	1.6	2.8

Thermal stress testing

All material type pass 5 cycles test except Material E. Reliability test condition: 260°C floating 10 seconds, 260°C Dipping 10 seconds.

	A	B	C	D	E
Floating	Pass*	Pass	Pass	Pass	Fail**
Dipping	Pass	Pass	Pass	Pass	Fail

*Score “Pass” means the sample passes 5 cycles of thermal stress test.
**Otherwise will be scored as “Fail”

Break down voltage test

Ink type materials cannot bear voltage higher than 100V.

	A	B	C	D	E
Pass	>500Volt	450Volt	90Volt	90Volt	45Volt
Fail		500Volt	100Volt	100Volt	50Volt

Agency or regulatory approvals

Wus is on going to apply for the approvals

Embedded Passive Test Vehicle Fabrication to Minimize Overall Impedance

By M. Che, Kang Hsu, Brandon Huang, Peter Tan, CP Kau, Dennis Lee, Yijen Lee, Eric Lin, ShanChen Ye, Avanti Wu, Nelson Chen, Anita Chang, WUS Printed Circuit Co. Ltd.

Abstract

Using different dielectric materials, this article benchmarks the impact of the overall impedance for a specially designed test vehicle with embedded passives approach. Our target is to search for a reliable yet cost effective approach to build a PWB with embedded passives achieving the overall impedance target, 500 mOhm at 1 GHz, for this test vehicle design. The test vehicle design concept and its follow-on functional test methods will be summarized. The critical PWB fabrication processes specially related with this study will be described. The pro and con of the various dielectric materials and its impact to the overall impedance will be compared. Most of all, a set of reliability test results will be analyzed and presented.

Materials

Material A

A traditional epoxy base 2 mils thickness thin core, high Tg-170°C and lower CTE from ambient to 288°C. This product goes through standard FR-4 processing; no post bake after pressing, drilling parameters and hole wall preparation are standard. Permittivity is about 4.6@1MHz; 4.28@500MHz; and 4.29@1GHz.

Material B

The thin core is an epoxy (non-bromide) filled with $BaTiO_3$ particles. Core spec is 8um thick dielectric with 1OZ copper. Dielectric constant is 14-18@1MHz.

Material C

Material C was developed as a thermal curable type intermediate dielectric material for roller coating and vertical screen printing coating machine, featuring its copper adhesion stability, inner layer adhesion and laser process-ability. The solid content is ranged from 74% to 76% with DK 3.9@1MHz.

Material D

This material is similar to Material C, requiring different processing method. This dielectric is a thermal curable material applicable for coating and copper foil method. In other words, this material is suitable for lamination. The solid content is ranged from 67% to 69% with DK 3.4@1GHz.

Material E

Material E is another build up material. It is ink type and photo-decomposition. DK is about 25.9@1KHz.

Equipment

The unique equipment used for fabrication includes:

Coating machines

Roller Coater, a vertical 2 sides printing machine. It features easy replacements of rollers, high clean class, good ink viscosity control, and uniform flow speed. Allowable minimum board thickness is down to 4 mils.

Laminate machines

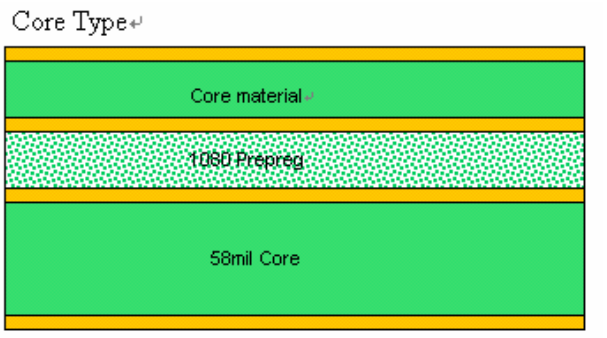
Hot Press Machine, max 200 kgf/cm^2 pressure. Platen thickness accuracy at 0.02mm, plane accuracy at 0.02mm. Platen size is 750mmX750mm. This machine has good heat transfer and low temperature difference.

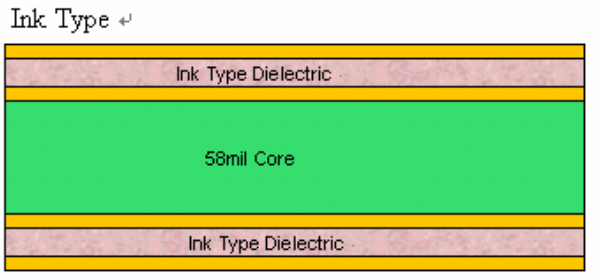
Test Board Features:

For different testing purpose we design 2 different test vehicles; one is for thin dielectric researching and the other is for impedance measurement

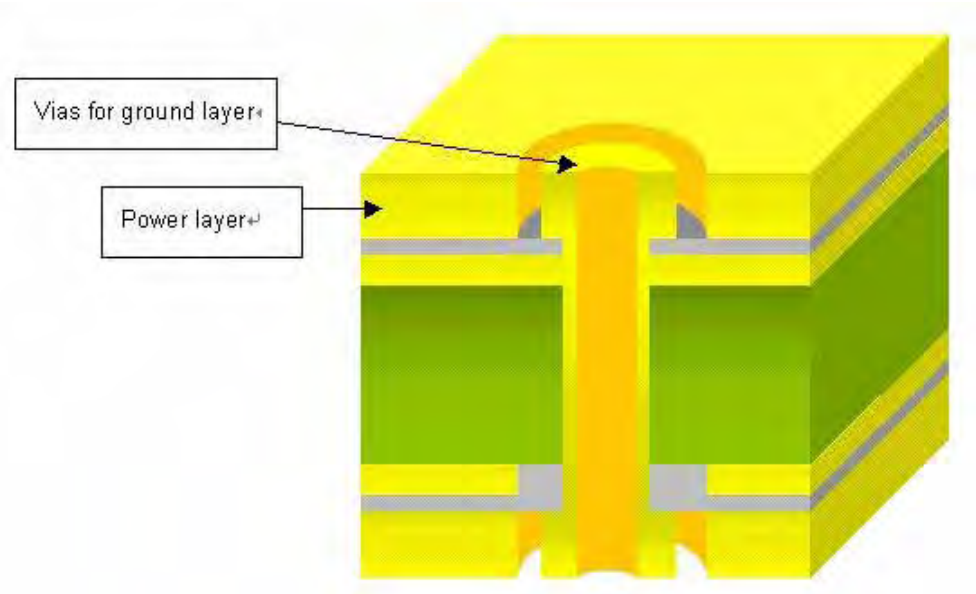
Test vehicle for thin dielectric researching:

The test board has an outline dimensions of 5”x10”. The construction contains four copper layers with different board thickness when using different materials.
There are two different stack-up structures for aforementioned five type materials. Two of them are core type and the rest of the three are ink type. Core type is made of two cores riveting together, and ink type is made of single core with ink coating dielectric on both sides. Below are the structures of both core type and ink type stackup:



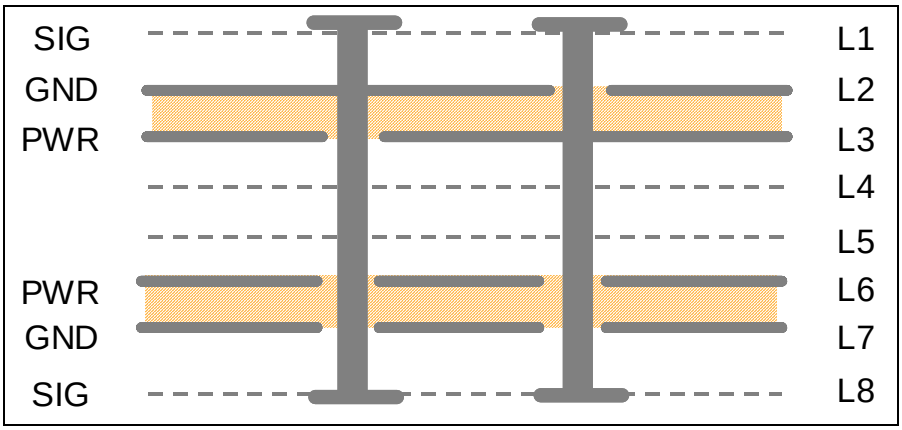


To support open/short test, we designed specific vias to lead out inner ground layer. As shown in the 3D drawing, yellow layers represent copper layers; grey layers represent ink type dielectric, and the green layer represents FR4 core.



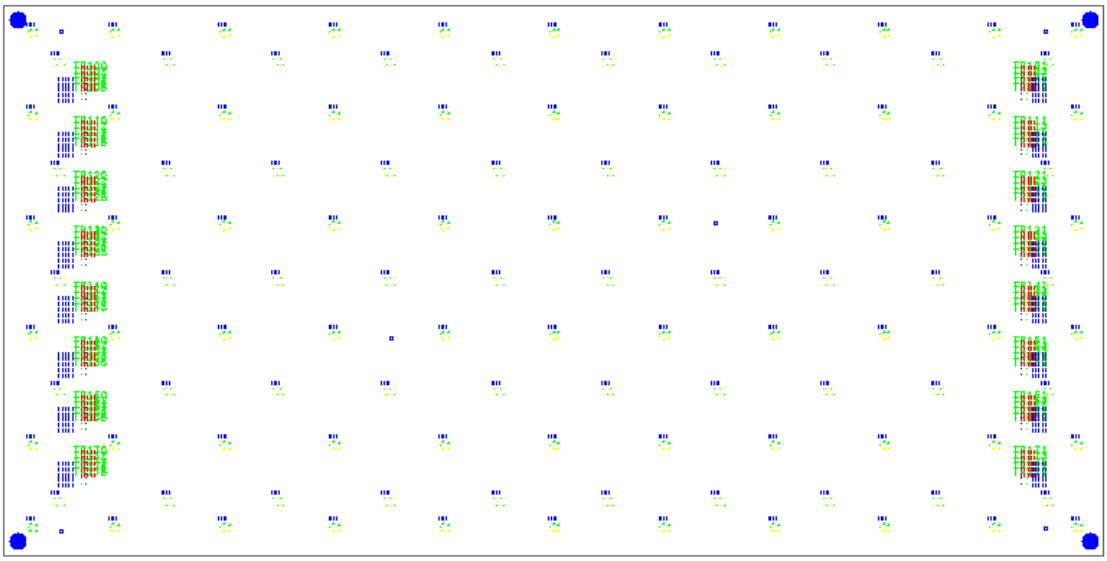
Test vehicle for impedance measurement:

The test vehicle for the impedance measurement has an outline dimensions of 5”x10”. The construction is eight copper layers as shown below. There are two thin cores, 3 mils below the surfaces.



Courtesy of SUN-East

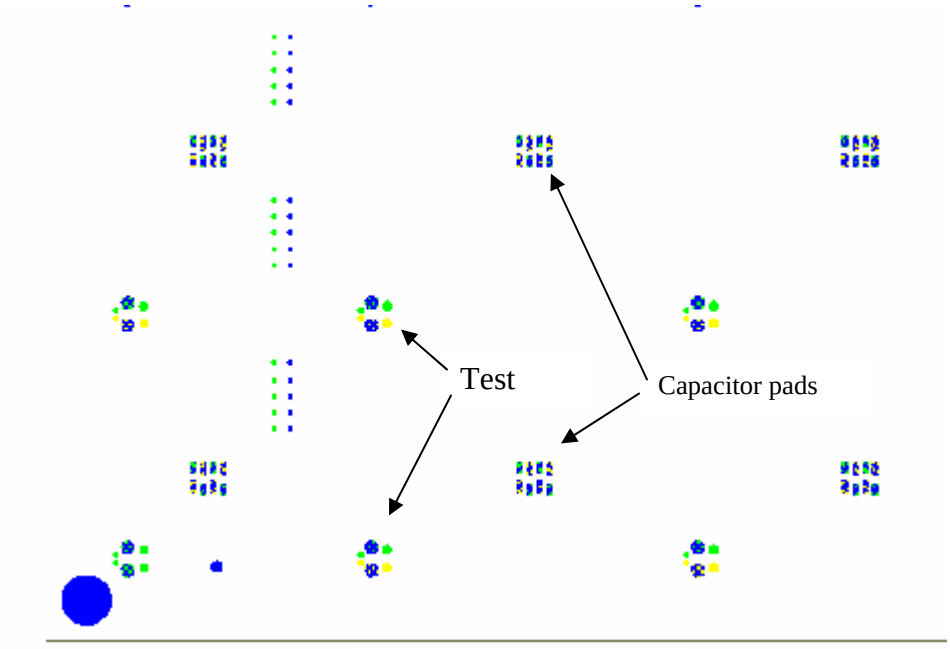
Each signal layer has five straight traces, connected to vias and test points. The signal traces were not used in the measurement of the power-distribution network.



Courtesy of SUN-East

Top overall view of the board with the capacitor pads and test vias.

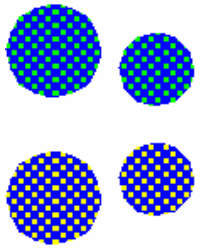
There are two one-inch square grids overlaid on the footprint of the board. The two grids are offset by half an inches. On one grid there are connection points for bypass capacitors, the other grid serves for testing.



Courtesy of SUN-East

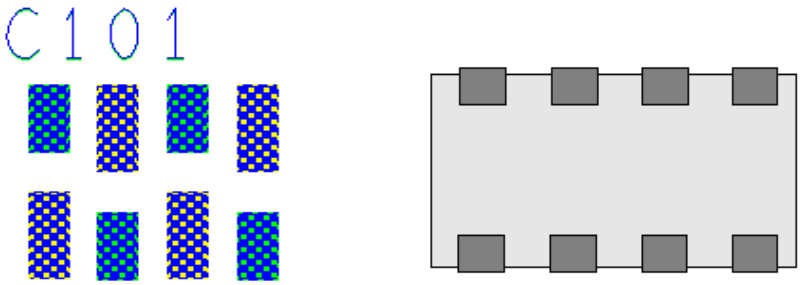
Zoomed top view of the board showing the two one-inch grids. In this document, only the test via grid was used.

To connect the measurement probes , as shown below, a set of plated through holes are located on one of the grids. The upper vias are connected to ground plane, the bottom vias connect to power plane. The bigger vias are 70 mils center to center, taking directly the pins of SSMB PCB posts. The smaller vias are 50 mils apart, and are sized to take 0.082" semirigid probes



Courtesy of SUN-East

The pads for eight-terminal capacitors are shown below. In the bare-board measurements, the capacitor pads were not connected or used in any way.



Courtesy of SUN-East

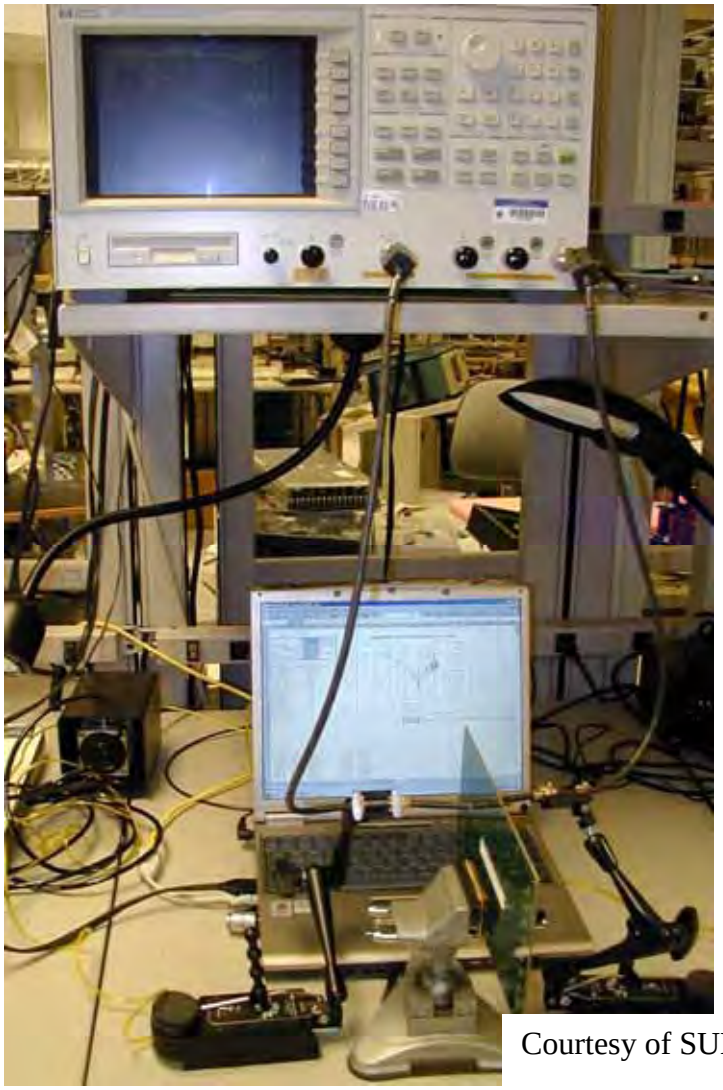
'Test vehicle for impedance measurement' is sourced from 'SUN-East'

The measurement setup

Instrumentation

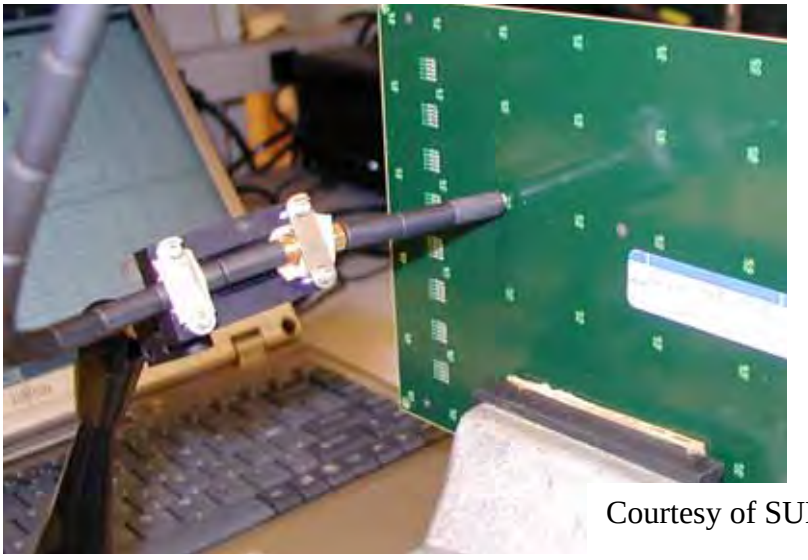
The self and transfer impedances were measured with the two-port measurement method with a Hewlett Packard HP4396A Vector Network Analyzer. Since only transfer parameters had to be measured, the transmission/reflection test kit was not used. This omission of the transmission/reflection kit actually increased the available dynamic range. The maximum frequency range was 0.1MHz to 1.8GHz, the output power at the RF OUT connector was set to –3dBm. Bandwidth was usually set to 100Hz, in cases when the impedance dropped to low values and the thermal noise began to show up on the measured trace, the bandwidth was further reduced to 10Hz. Input B was used to receive the signal.

The test points were connected to the VNA inputs through two pieces of 24-inch long Tensolite 0.082" E-Z coax cables with 50-mil open pigtail and 50-mil long ground wire as posts connecting to the plated through holes. To suppress cable-shield resonances, each cable was covered with 33 pieces of FerrShield 28B0250-1 absorbing ferrite sleeves.



Courtesy of SUN-East

Probes



Courtesy of SUN-East

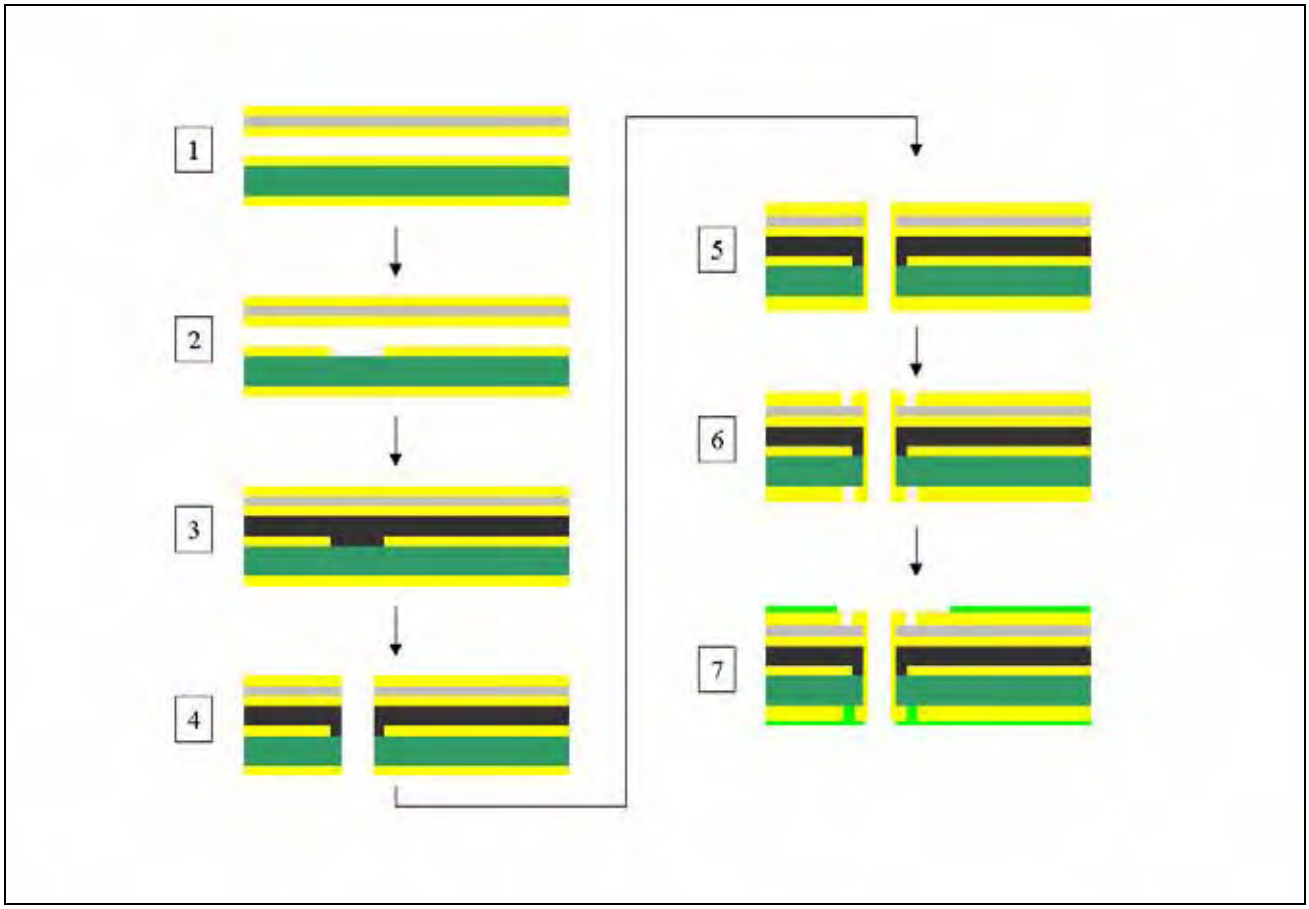
Ferrite covered coax cable with semirigid probe in EZ-Probe station, with ferrite sleeves.

Process

For different materials, there are three process approaches. They are:

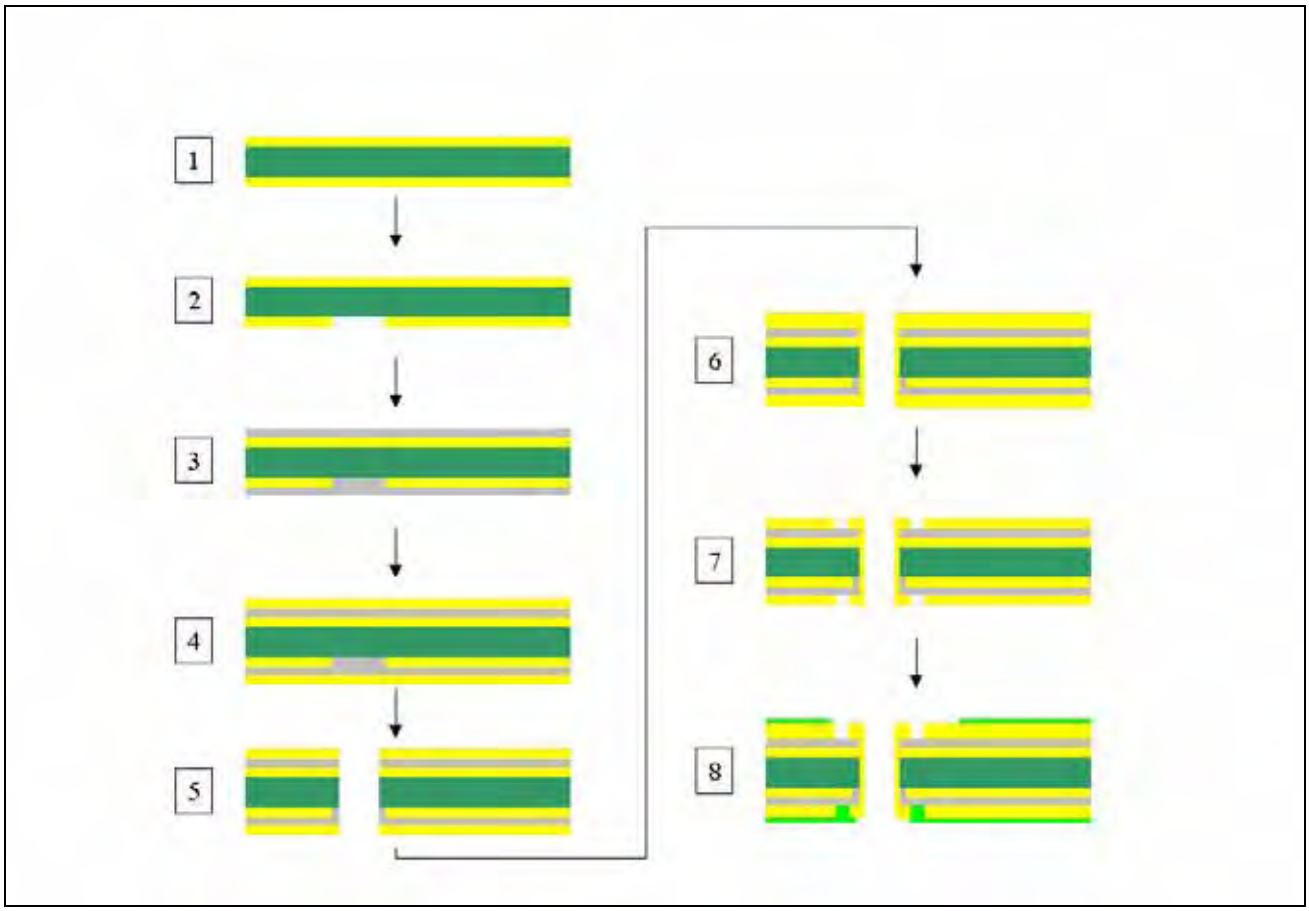
Core type process for Material type A or B

1. Upper core: Material A or B ; Lower core: 58 mil FR4.
2. Inner layer circuit formation.
3. Laminate two cores with 1080 prepreg inside.
4. NC drilling.
5. Copper plating.
6. Outer layer circuit formation.
7. Solder mask processing.



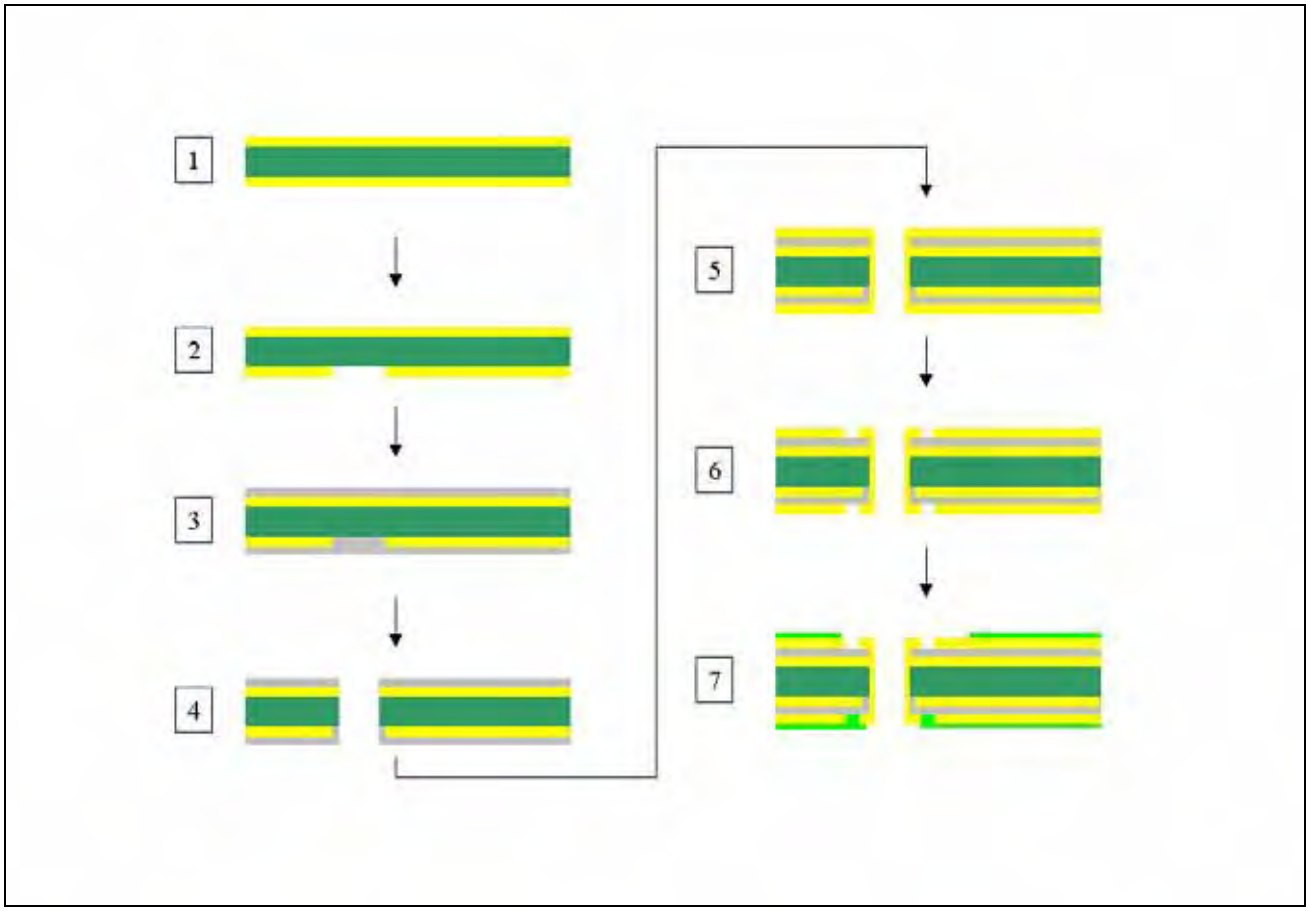
Ink type I process for Material D and E

1. 58 mil FR4 core
2. Circuit formation for inner layers .
3. Dielectric coating by roller coater.
4. Laminating with copper foils.
5. NC drilling
6. Copper plating
7. Outer layer circuit formation
8. Solder mask processing.



Ink type II process for Material C

1. 58 mil FR4 core
2. Circuit formation for inner layer.
3. Dielectric coating using roller coater, and followed by baking
4. NC drilling.
5. Copper plating.
6. Outer layer circuit formation.
7. Solder mask processing.

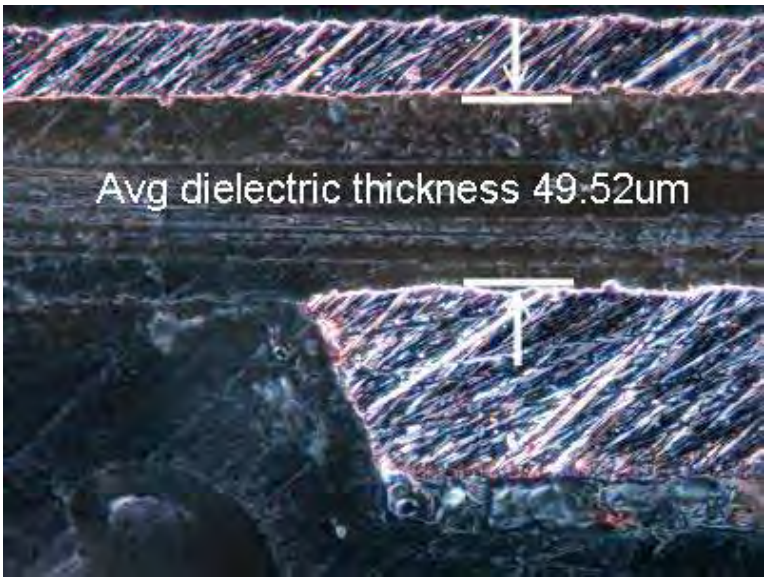


Summary of test vehicle for thin dielectric researching

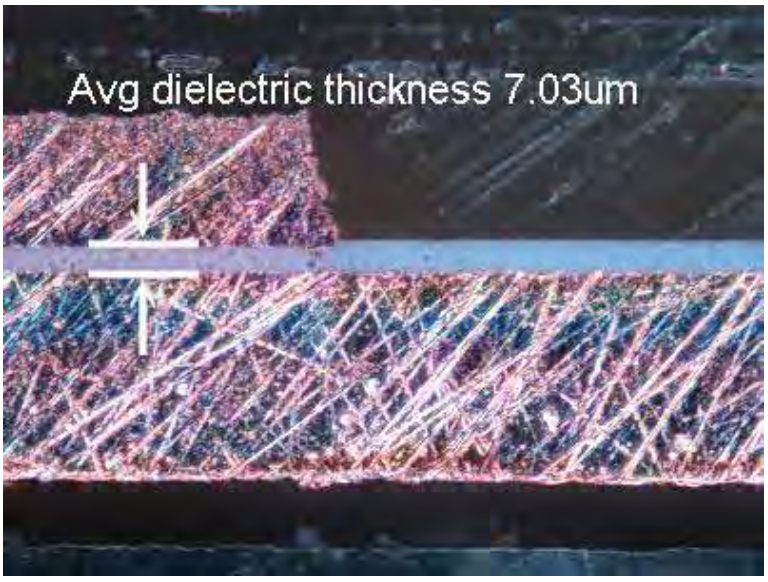
Thickness

Table below shows the thinnest dielectric that we have tried for different material types:

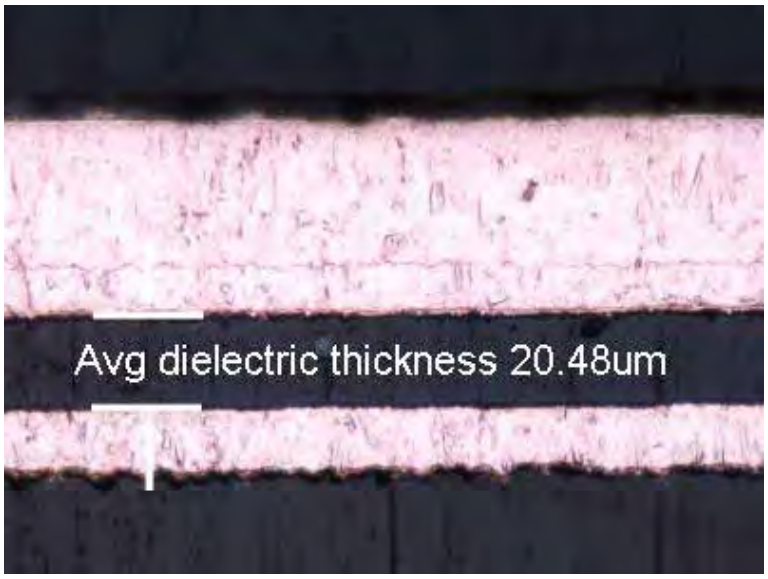
	A	B	C	D	E
Thickness(um)	49.52	7.03	34.65	20.48	10.35
Cpk	2.45	0.62	2.13	1.03	0.8



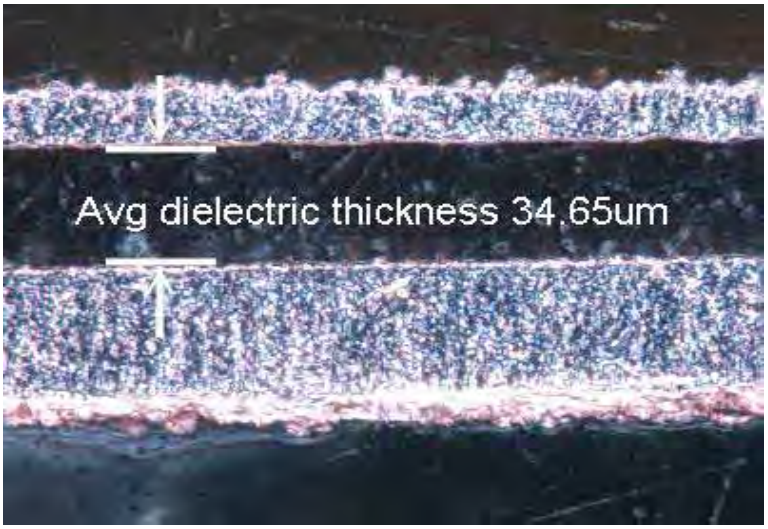
Material A with 500X zoom



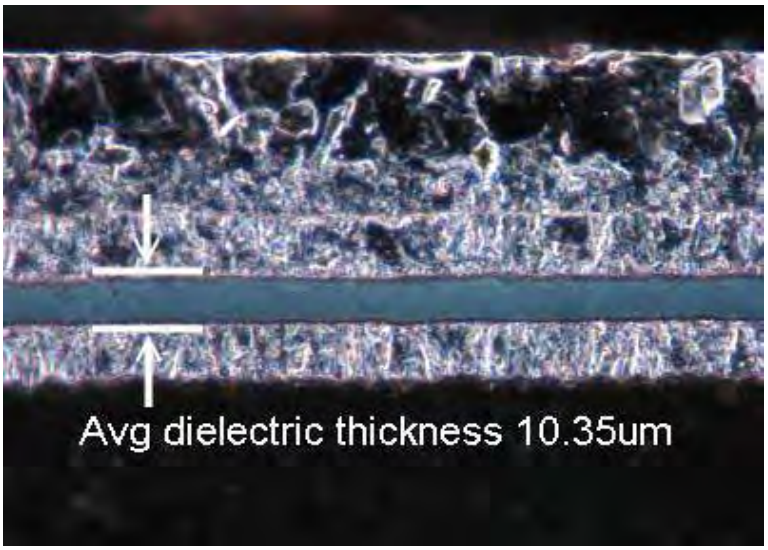
Material B with 500X zoom



Material C with 500X zoom

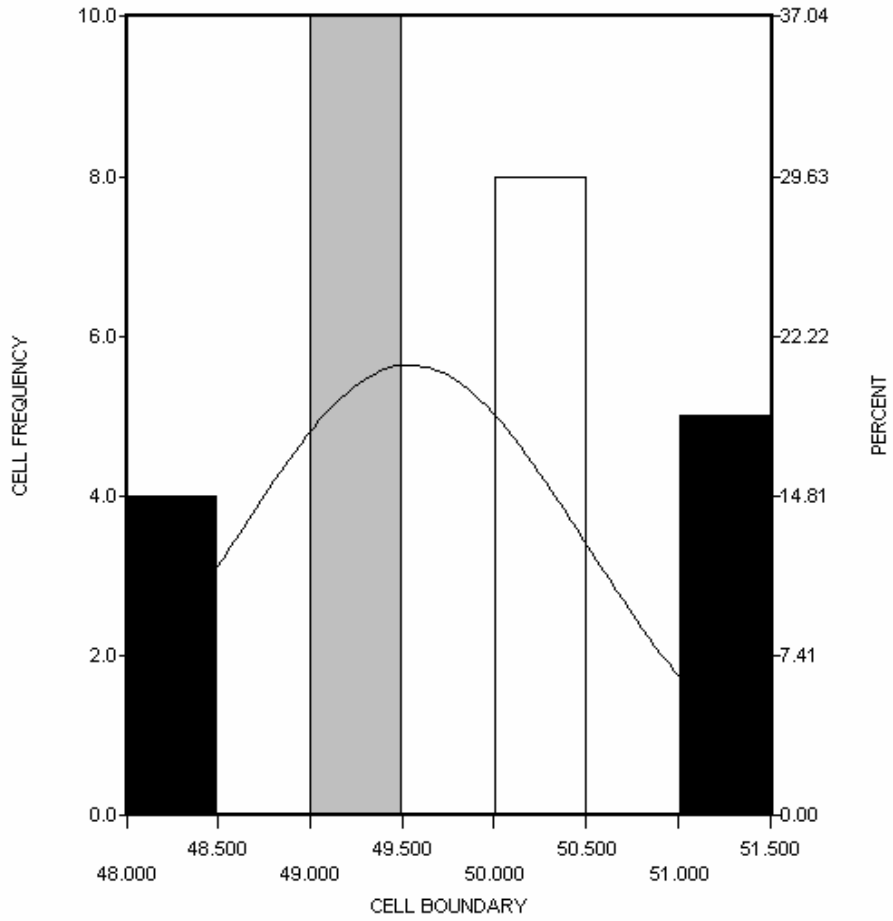


Material D with 500X zoom



Material E with 500X zoom

Material A

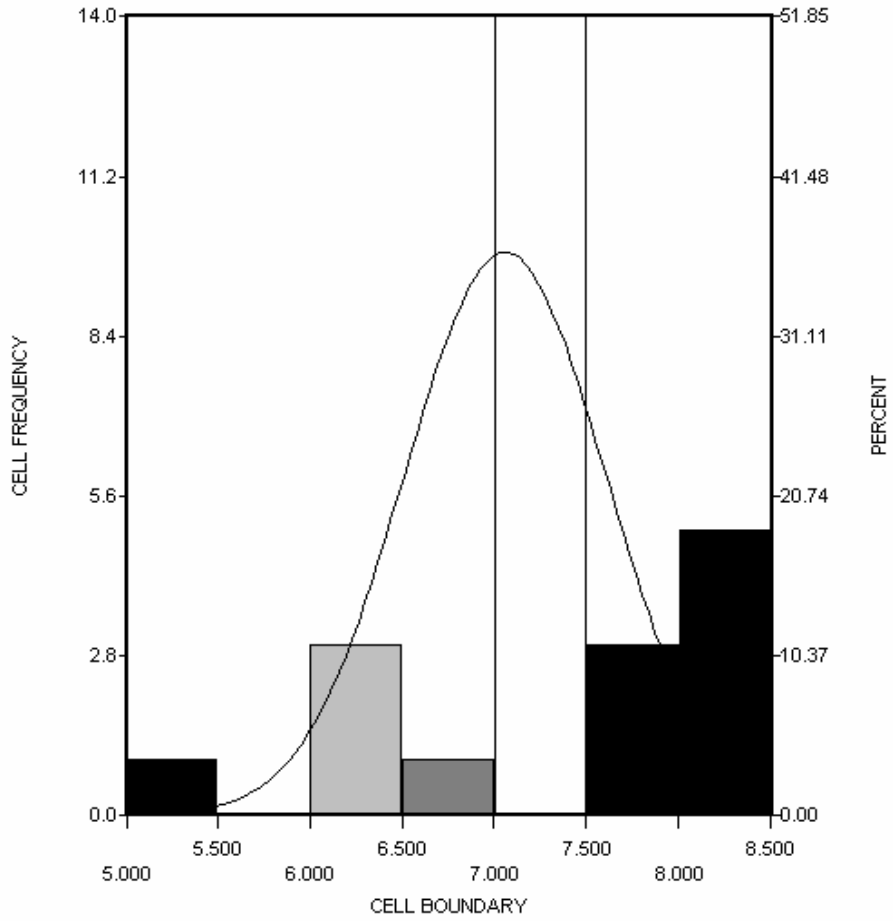


Fitted curve is a Normal. K-S test: 0.200. Lack of fit is not significant.

SUMMARY DATA	PERFORMANCE STATISTICS	CAPABILITY ANALYSIS (.00 sig	
ANALYSIS OF GROUPS 1-27	NOMINAL : 50.000		NORMAL
GROUPS = 27 (27 OBSERVATION	LOW SPEC : 42.500	Cp	2.62
LARGEST VALUE : 51.000	HIGH SPEC : 57.500	Cr	38%
SMALLEST VALUE : 48.000	AVERAGE(m) : 49.519	Cpm	2.34
OVERALL RANGE : 3.000	m - 3s : 46.655	Zl(Cpl)	7.35(2.45)
POPULATION SIGMA : 0.957	m + 3s : 52.382	Zu(Cpu)	8.36(2.79)
SAMPLE SIGMA : 0.975	m - 4.00s : 45.701	Cpk	2.45
PROCESS SIGMA (s) : 0.954	m + 4.00s : 53.336	PROCESS	capable
SKEWNESS : 0.070	0 VALUES BELOW 42.500	% LOW	0.0000%
KURTOSIS : -1.098	0 VALUES ABOVE 57.500	% HIGH	0.0000%
	0 VALUES OUT OF SPEC	% OUT	0.0000%

WARNING: Capability analysis is not valid for out of control processes.

Material B

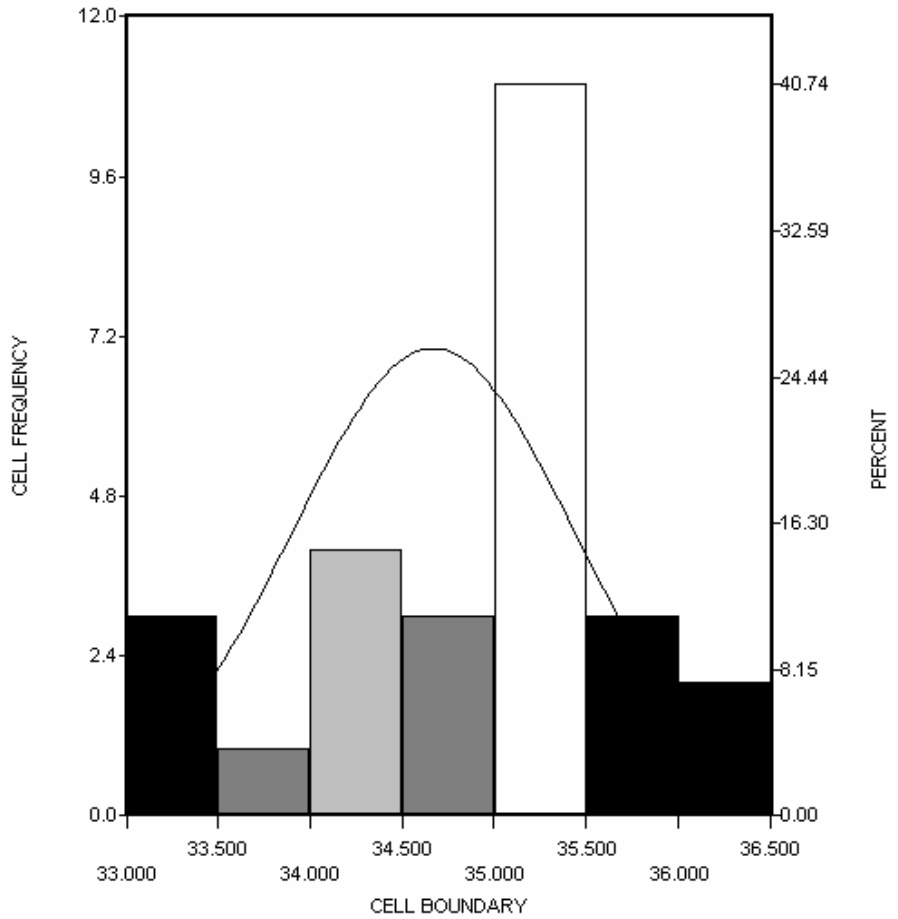


Fitted curve is a Normal. K-S test: 0.028. Lack of fit is significant.

SUMMARY DATA	PERFORMANCE STATISTICS	CAPABILITY ANALYSIS (.00 sig	
ANALYSIS OF GROUPS 1-27	NOMINAL : 7.000		NORMAL
GROUPS = 27 (27 OBSERVATION	LOW SPEC : 5.950	Cp	0.64
LARGEST VALUE : 8.000	HIGH SPEC : 8.050	Cr	156%
SMALLEST VALUE : 5.000	AVERAGE(m) : 7.037	Cpm	0.64
OVERALL RANGE : 3.000	m - 3s : 5.401	Zl(Cpl)	1.99(0.66)
POPULATION SIGMA : 0.693	m + 3s : 8.673	Zu(Cpu)	1.86(0.62)
SAMPLE SIGMA : 0.706	m - 4.00s : 4.856	Cpk	0.62
PROCESS SIGMA (s) : 0.545	m + 4.00s : 9.218	PROCESS	incapable
SKEWNESS : -0.757	1 VALUES BELOW 5.950	% LOW	2.3117%
KURTOSIS : 0.756	0 VALUES ABOVE 8.050	% HIGH	3.1626%
	1 VALUES OUT OF SPEC	% OUT	5.4743%

WARNING: Capability analysis is not valid for out of control processes.

Material C

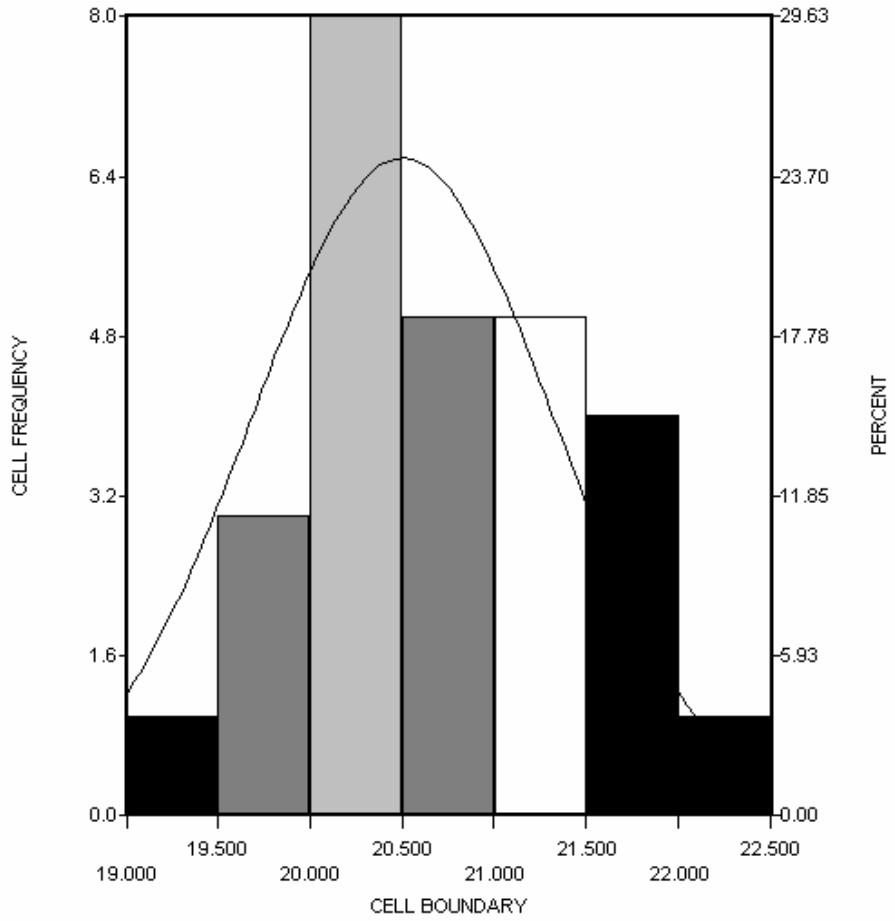


Fitted curve is a Normal. K-S test: 0.062. Lack of fit is not significant.

SUMMARY DATA	PERFORMANCE STATISTICS	CAPABILITY ANALYSIS (.00 sig	
ANALYSIS OF GROUPS 1-27	NOMINAL : 35.000		NORMAL
GROUPS = 27 (27 OBSERVATION	LOW SPEC : 29.750	Cp	2.28
LARGEST VALUE : 36.000	HIGH SPEC : 40.250	Cr	44%
SMALLEST VALUE : 33.000	AVERAGE(m) : 34.648	Cpm	2.07
OVERALL RANGE : 3.000	m - 3s : 32.347	Zl(Cpl)	6.39(2.13)
POPULATION SIGMA : 0.826	m + 3s : 36.949	Zu(Cpu)	7.30(2.43)
SAMPLE SIGMA : 0.841	m - 4.00s : 31.580	Cpk	2.13
PROCESS SIGMA (s) : 0.767	m + 4.00s : 37.716	PROCESS	capable
SKEWNESS : -0.545	0 VALUES BELOW 29.750	% LOW	0.0000%
KURTOSIS : -0.561	0 VALUES ABOVE 40.250	% HIGH	0.0000%
	0 VALUES OUT OF SPEC	% OUT	0.0000%

WARNING: Capability analysis is not valid for out of control processes.

Material D



Fitted curve is a Normal. K-S test: 0.621. Lack of fit is not significant.

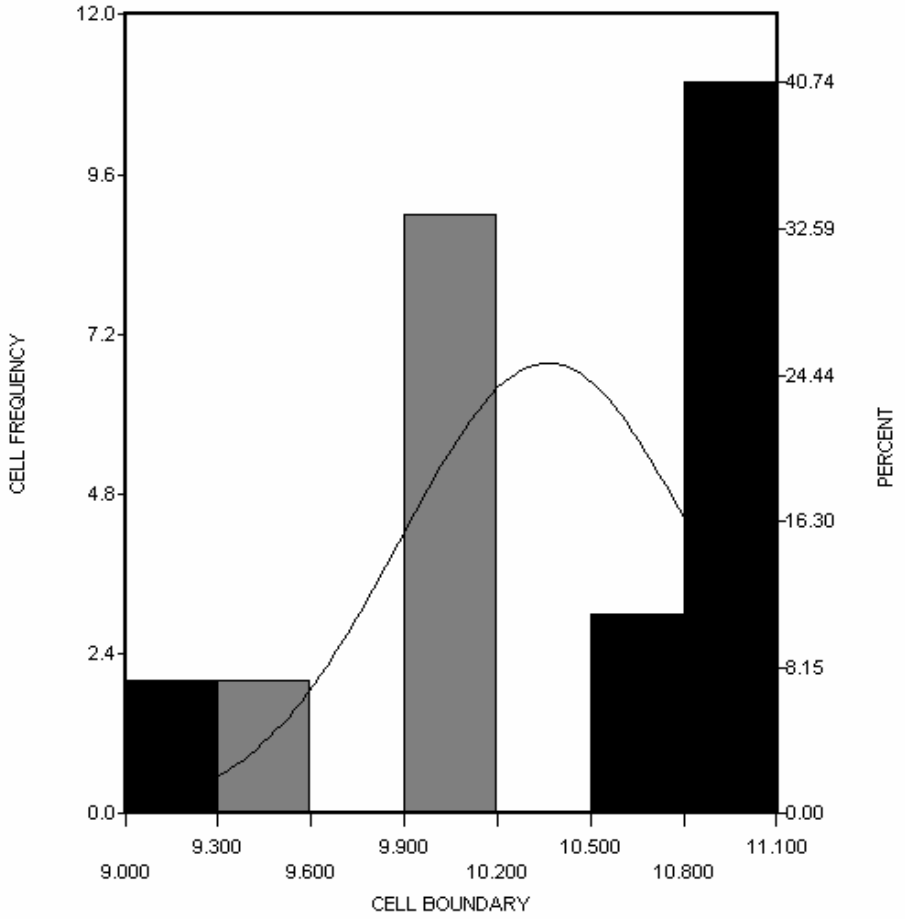
SUMMARY DATA	PERFORMANCE STATISTICS	CAPABILITY ANALYSIS (.00 sig	
ANALYSIS OF GROUPS 1-27	NOMINAL : 20.000		NORMAL
GROUPS = 27 (27 OBSERVATION	LOW SPEC : 17.000	Cp	1.22
LARGEST VALUE : 22.000	HIGH SPEC : 23.000	Cr	82%
SMALLEST VALUE : 19.000	AVERAGE(m) : 20.481	Cpm	1.05
OVERALL RANGE : 3.000	m - 3s : 18.027	Zl(Cpl)	4.26(1.42)
POPULATION SIGMA : 0.739	m + 3s : 22.936	Zu(Cpu)	3.08(1.03)
SAMPLE SIGMA : 0.753	m - 4.00s : 17.209	Cpk	1.03
PROCESS SIGMA (s) : 0.818	m + 4.00s : 23.754	PROCESS	marginal
SKEWNESS : 0.125	0 VALUES BELOW 17.000	% LOW	0.0010%
KURTOSIS : -0.924	0 VALUES ABOVE 23.000	% HIGH	0.1040%
	0 VALUES OUT OF SPEC	% OUT	0.1050%

WARNING: Capability analysis is not valid for out of control processes.

01/11/21 17:15

CHART7: Process Capability Chart: DATA10.QDB - DATA3

Material E



Fitted curve is a Normal. K-S test: 0.017. Lack of fit is significant.

SUMMARY DATA	PERFORMANCE STATISTICS	CAPABILITY ANALYSIS (.00 sig	
ANALYSIS OF GROUPS 1-27	NOMINAL : 10.000		NORMAL
GROUPS = 27 (27 OBSERVATION	LOW SPEC : 8.500	Cp	1.05
LARGEST VALUE : 11.000	HIGH SPEC : 11.500	Cr	95%
SMALLEST VALUE : 9.000	AVERAGE(m) : 10.352	Cpm	0.84
OVERALL RANGE : 2.000	m - 3s : 8.920	Zl(Cpl)	3.88(1.29)
POPULATION SIGMA : 0.636	m + 3s : 11.783	Zu(Cpu)	2.41(0.80)
SAMPLE SIGMA : 0.648	m - 4.00s : 8.443	Cpk	0.80
PROCESS SIGMA (s) : 0.477	m + 4.00s : 12.261	PROCESS	incapable
SKEWNESS : -0.486	0 VALUES BELOW 8.500	% LOW	0.0052%
KURTOSIS : -0.935	0 VALUES ABOVE 11.500	% HIGH	0.8063%
	0 VALUES OUT OF SPEC	% OUT	0.8115%

WARNING: Capability analysis is not valid for out of control processes.

01/11/21 17:13

CFP.QDC: Process Capability Chart: DATA1 - DATA1

Peel strength

Table below shows the peel strength measurement data:

	A	B	C	D	E
Max:lb/in^2	6.8	4.8	6.9	2.4	3.2
Min:lb/in^2	6	4.16	6.6	1.6	2.8

Thermal stress testing

All material type pass 5 cycles test except Material E. Reliabilty test condition: 260°C floating 10 seconds, 260°C Dipping 10 seconds.

	A	B	C	D	E
Floating	Pass*	Pass	Pass	Pass	Fail**
Dipping	Pass	Pass	Pass	Pass	Fail

*Score “Pass” means the sample passes 5 cycles of thermal stress test.
**Otherwise will be scored as “Fail”

Break down voltage test

Ink type materials cannot bear voltage high than 100V.

	A	B	C	D	E
Pass	>500Volt	450Volt	90Volt	90Volt	45Volt
Fail		500Volt	100Volt	100Volt	50Volt

Yield rate

A	B	C	D	E
100%	93.33%	66.67%	~33.33%	Need to Improve

Summary of test vehicle for impedance measurement

Thickness

Table below shows the dielectric thickness that we have tried for different material types:

	A	C	E
Thickness(um)	61.93	45.78	22.05
Cpk	2.67	2.58	1.16

Thermal stress testing

All material type pass 5 cycles test. Reliabilty test condition: 260°C floating 10 seconds, 260°C Dipping 10 seconds.

	A	C	E
Floating	Pass*	Pass	Pass
Dipping	Pass	Pass	Pass

*Score “Pass” means the sample passes 5 cycles of thermal stress test.
**Otherwise will be scored as “Fail”

Break down voltage test

Ink type materials cannot bear voltage high than 100V.

	A	C	E
Pass	>600Volt	70Volt	
Fail		80Volt	

Yield rate

A	C	E
100%	72.22%	Need to Improve

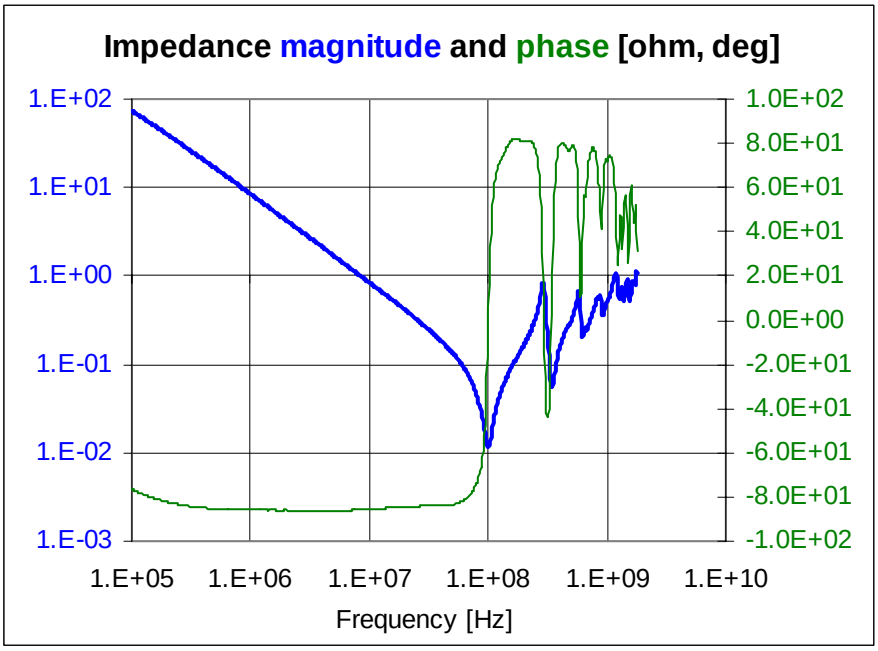
Impedance Measurement Results

Below is the summary of the bare-board wide-band impedance measurement results on Material A, C, and E boards.

There are two one-inch grids on the boards, one grid determines the locations of possible capacitors to mount to, the other grid identifies the test points. There are six rows and eleven columns of test points, giving a total of 66 test connection possibilities.

Summary of Material A results

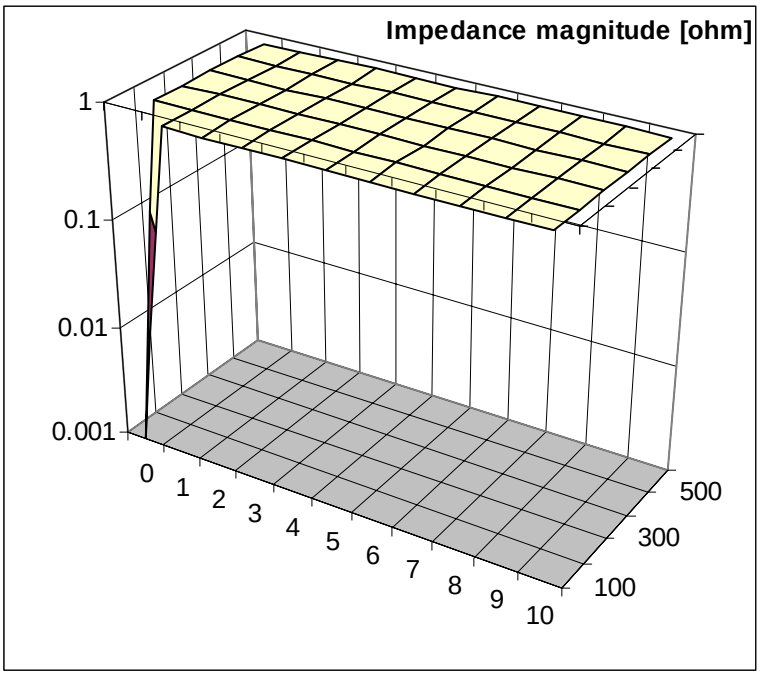
A representative self-impedance magnitude plot is shown below. The 2.4-mil laminate provides <1ohm impedance up to 1GHz. Note the resonance peaks and dips are pronounced in the impedance profile.



Courtesy of SUN-East

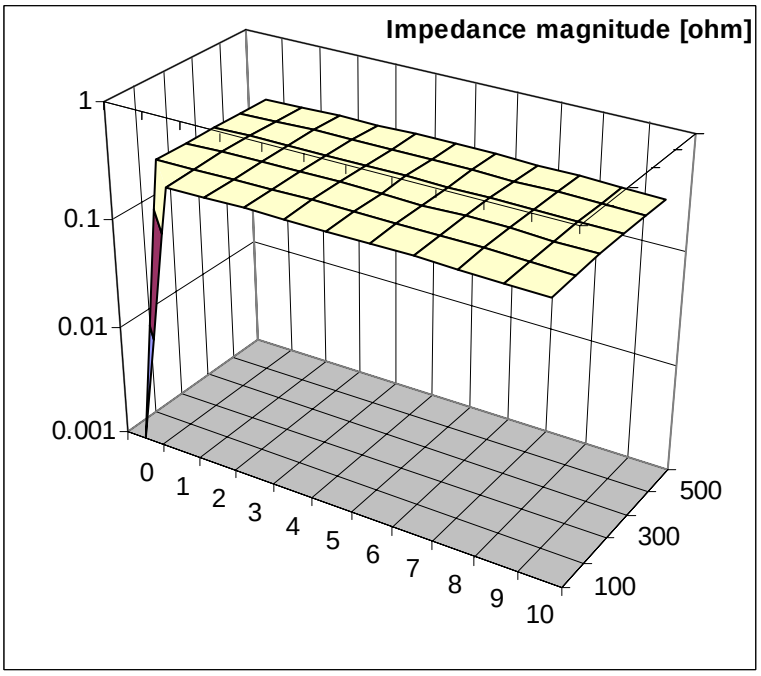
Self impedance magnitude (blue, thick line with left-side vertical axis) and phase (green, thin line with right-side axis). Test point: J400.

Note that on all subsequent impedance surfaces the J100 (lower-left corner) test point is intentionally shorted.



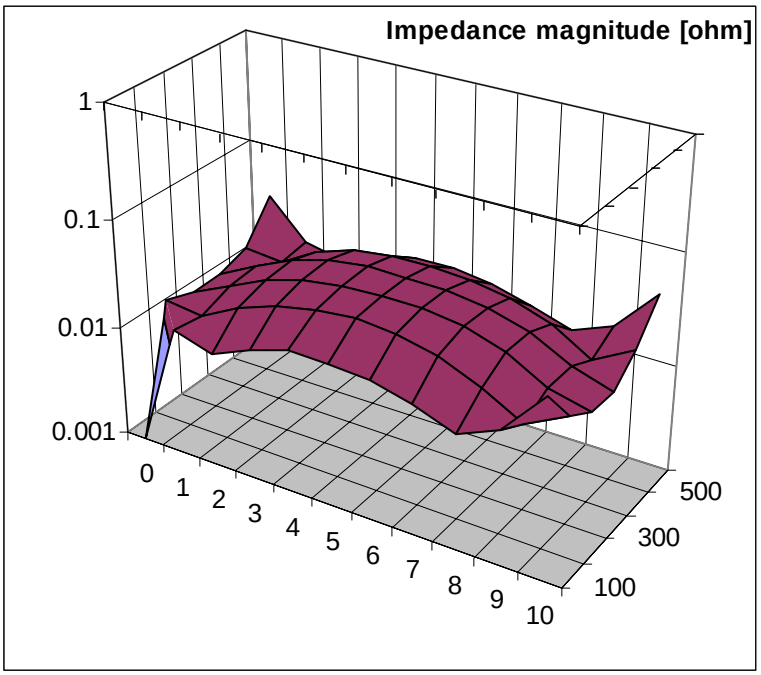
Courtesy of SUN-East

Self-impedance magnitude at 10MHz, along the surface of the board.



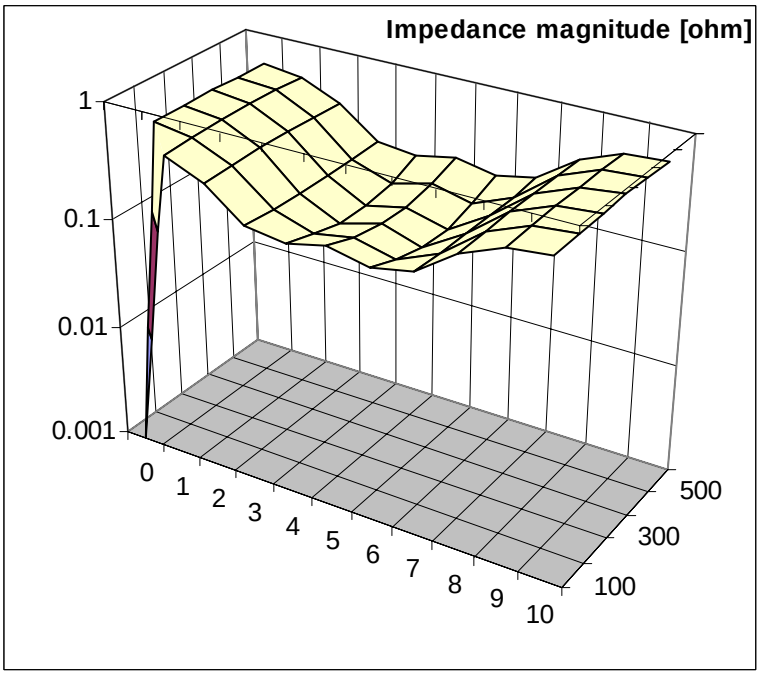
Courtesy of SUN-East

Self-impedance magnitude at 30MHz, along the surface of the board.



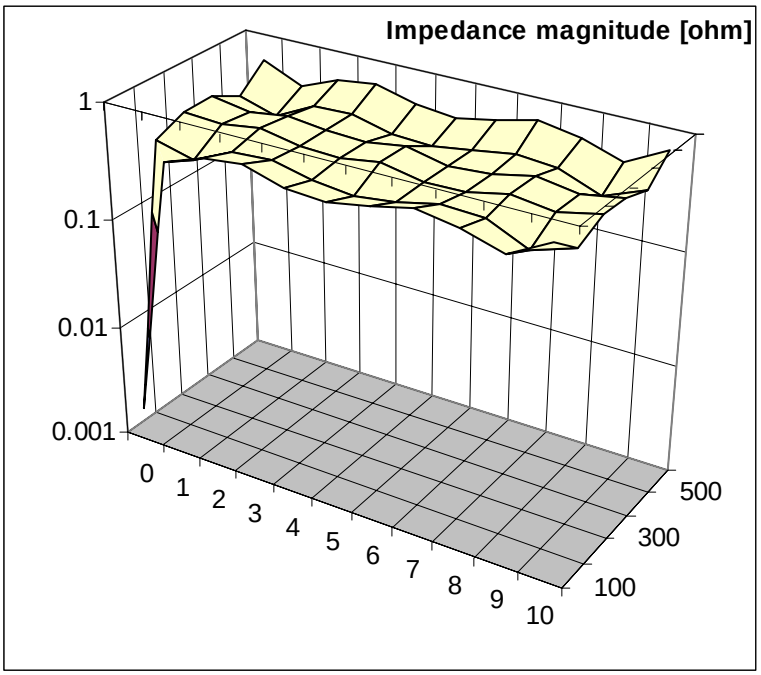
Courtesy of SUN-East

Self-impedance magnitude at 100MHz, along the surface of the board.



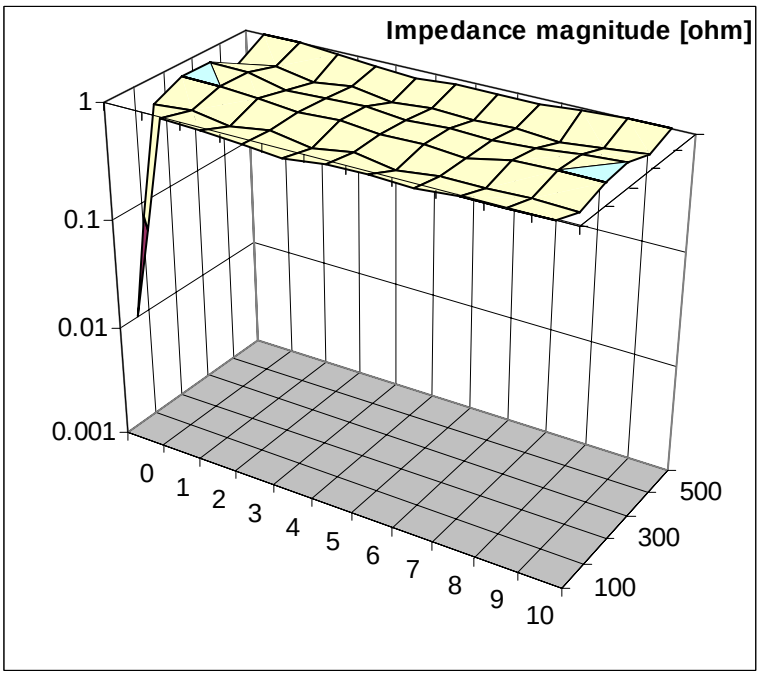
Courtesy of SUN-East

Self-impedance magnitude at 300MHz, along the surface of the board.



Courtesy of SUN-East

Self-impedance magnitude at 1000MHz, along the surface of the board.

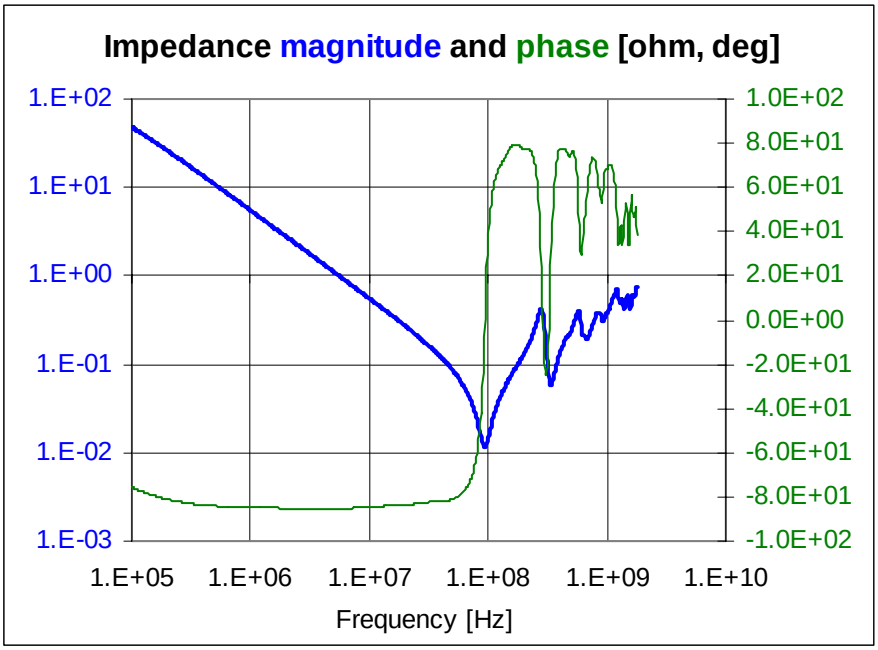


Courtesy of SUN-East

Self-impedance magnitude at 1800MHz, along the surface of the board.

Summary of Material C results

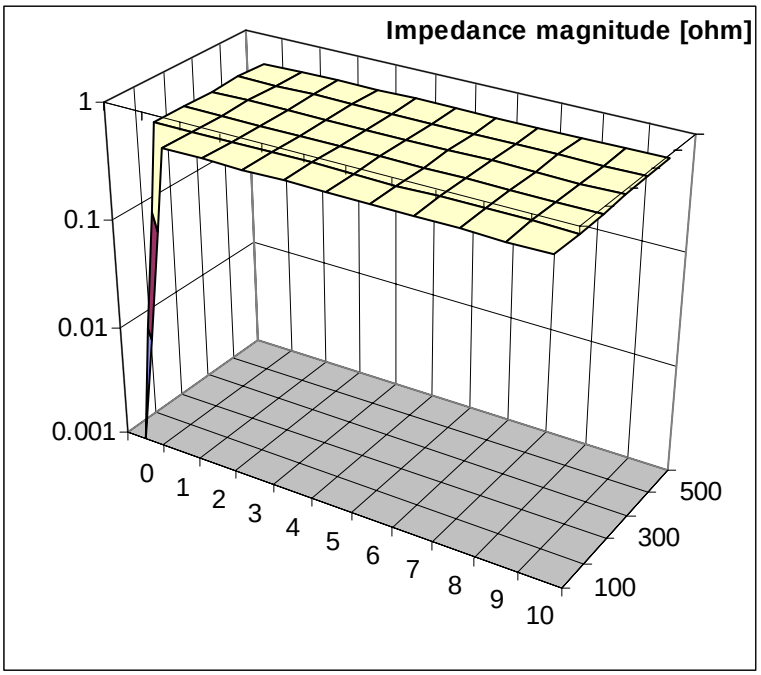
A representative self-impedance magnitude plot is shown below. The 1.7-mil laminate provides <0.6ohm impedance up to 1GHz. Note the resonance peaks and dips are pronounced in the impedance profile.



Courtesy of SUN-East

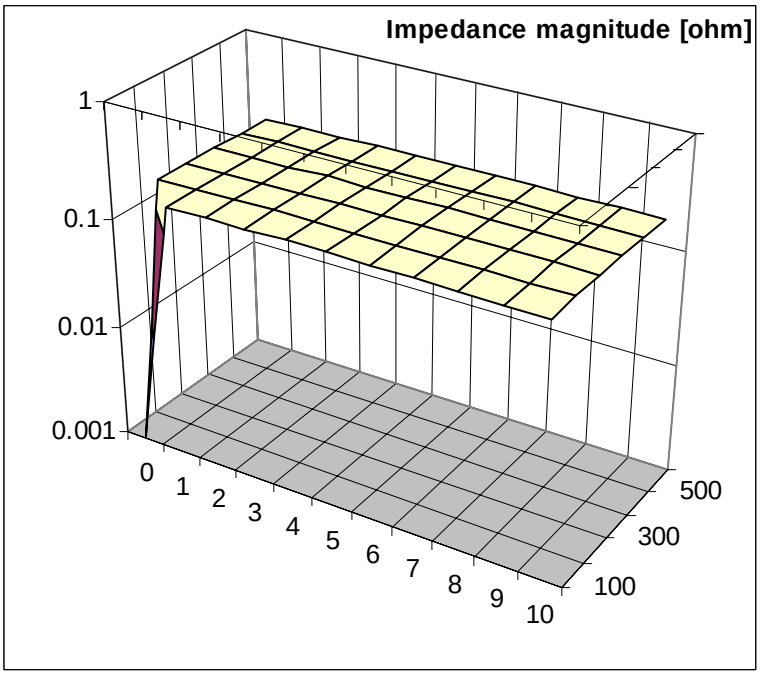
Self impedance magnitude (blue, thick line with left-side vertical axis) and phase (green, thin line with right-side axis). Test point: J400

Note that on all subsequent impedance surfaces the J100 (lower-left corner) test point is intentionally shorted.



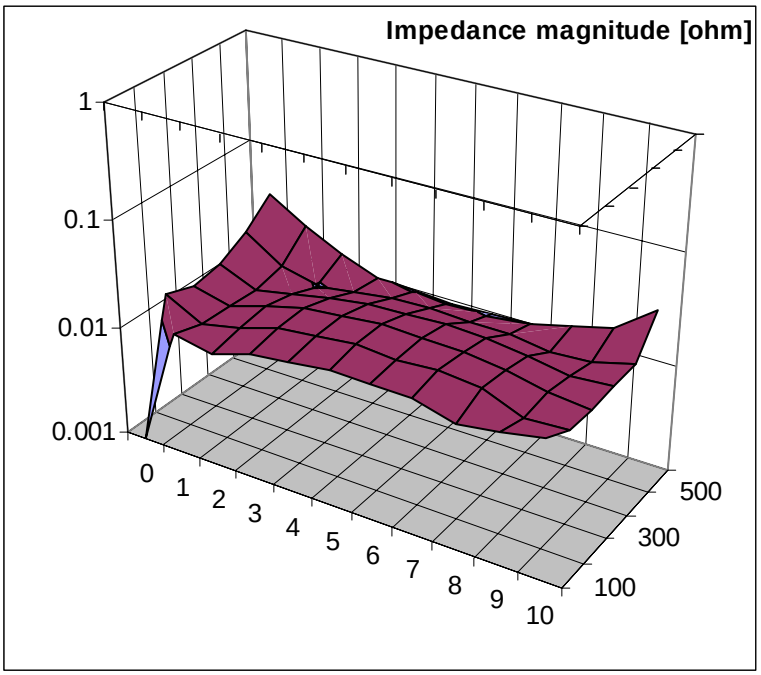
Courtesy of SUN-East

Self-impedance magnitude at 10MHz, along the surface of the board.



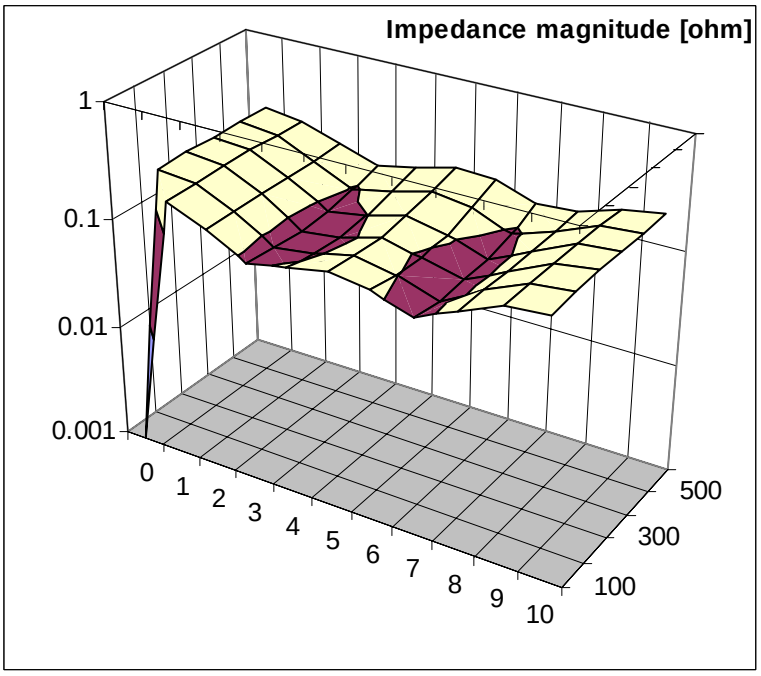
Courtesy of SUN-East

Self-impedance magnitude at 30MHz, along the surface of the board.



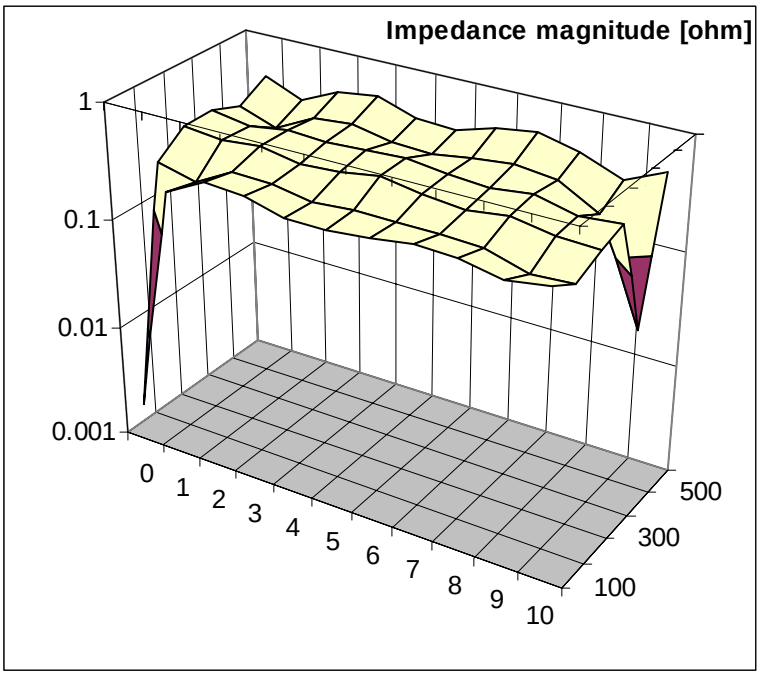
Courtesy of SUN-East

Self-impedance magnitude at 100MHz, along the surface of the board.



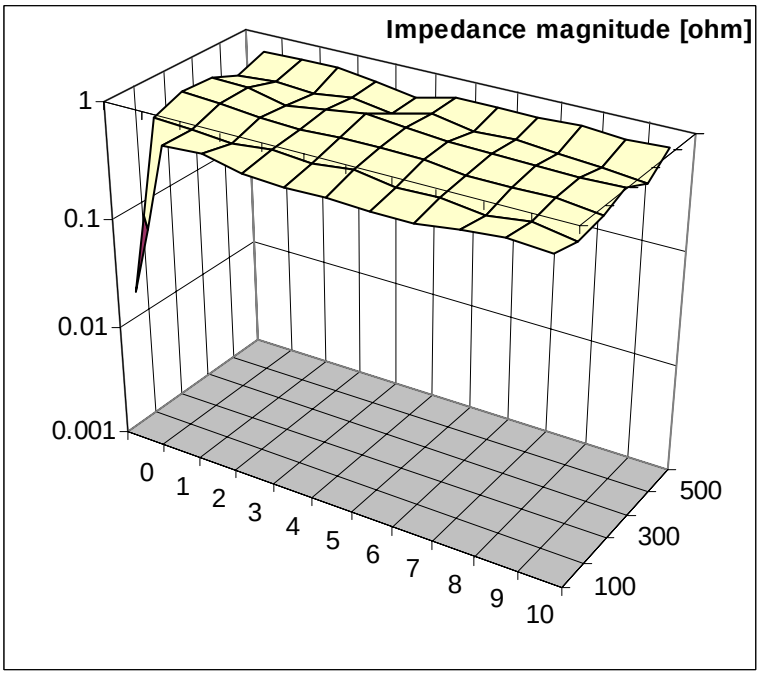
Courtesy of SUN-East

Self-impedance magnitude at 300MHz, along the surface of the board.



Courtesy of SUN-East

Self-impedance magnitude at 1000MHz, along the surface of the board.

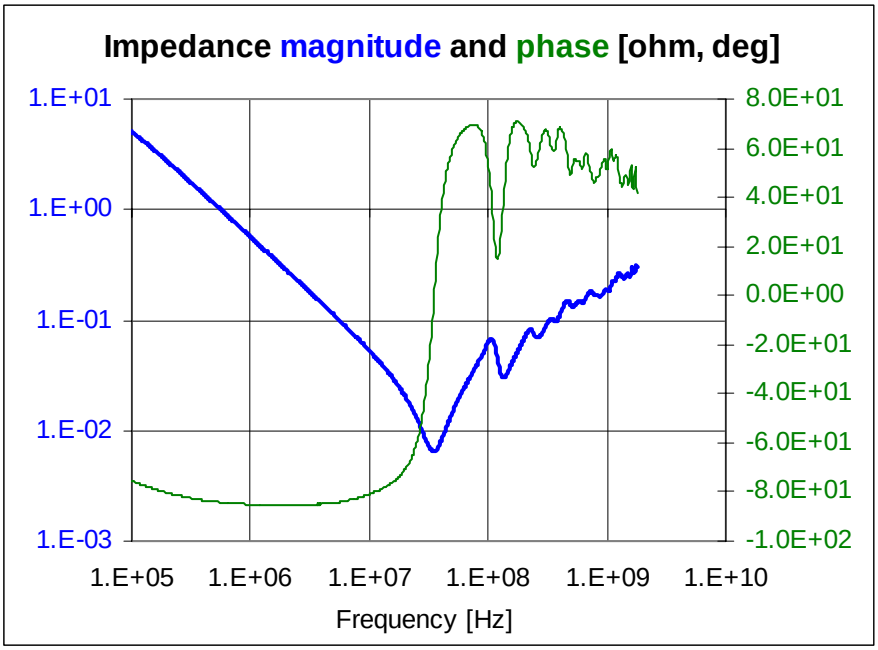


Courtesy of SUN-East

Self-impedance magnitude at 1800MHz, along the surface of the board.

Summary of Material E results

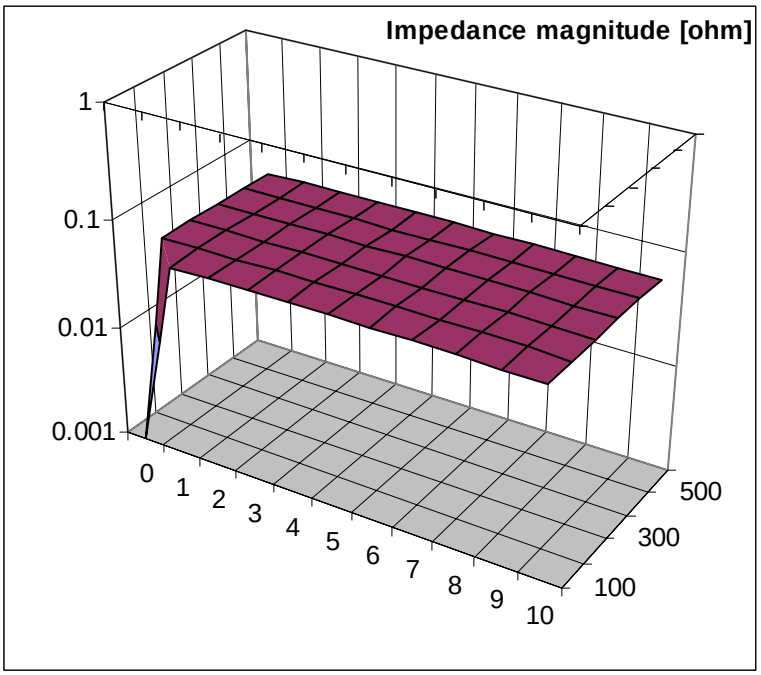
A representative self-impedance magnitude plot is shown below. The 0.7-mil ceramic-filled laminate provides <0.25ohm impedance up to 1GHz. Note the resonance peaks and dips are dampened in the impedance profile.



Courtesy of SUN-East

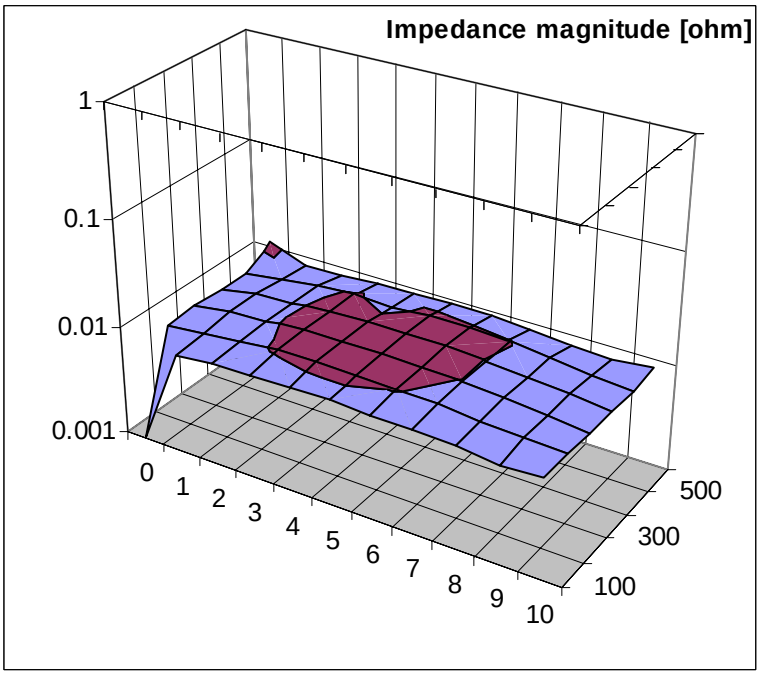
Self impedance magnitude (blue, thick line with left-side vertical axis) and phase (green, thin line with right-side axis). Test point: J400

Note that on all subsequent impedance surfaces the J100 (lower-left corner) test point is intentionally shorted.



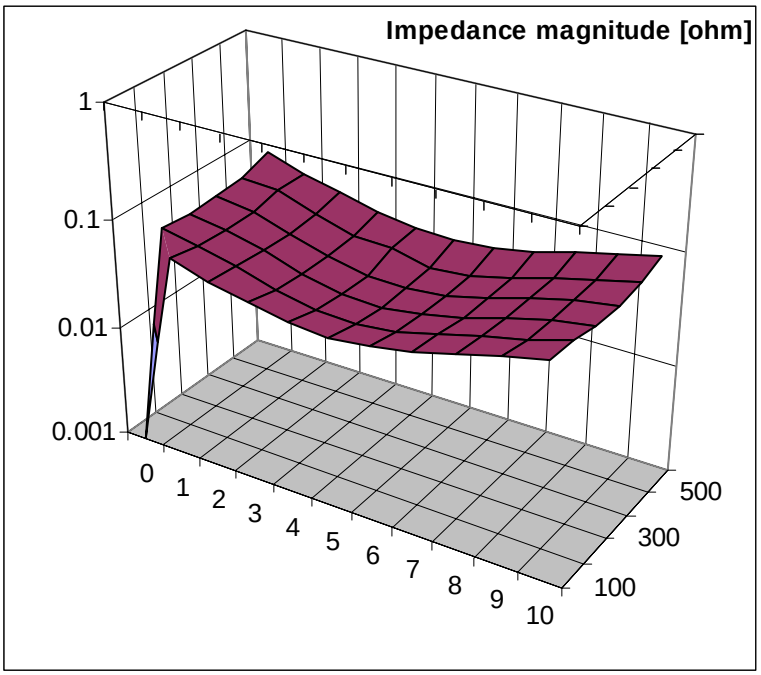
Courtesy of SUN-East

Self-impedance magnitude at 10MHz, along the surface of the board.



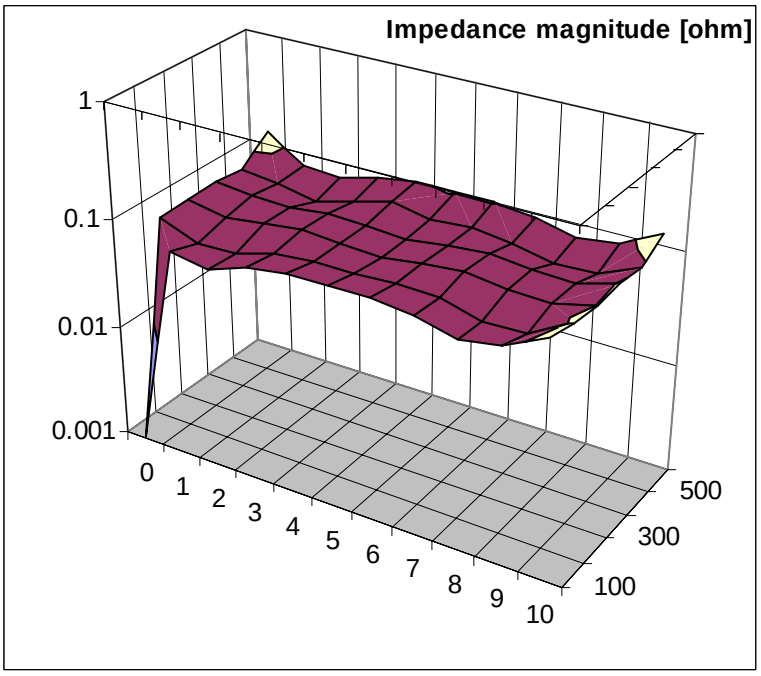
Courtesy of SUN-East

Self-impedance magnitude at 30MHz, along the surface of the board.



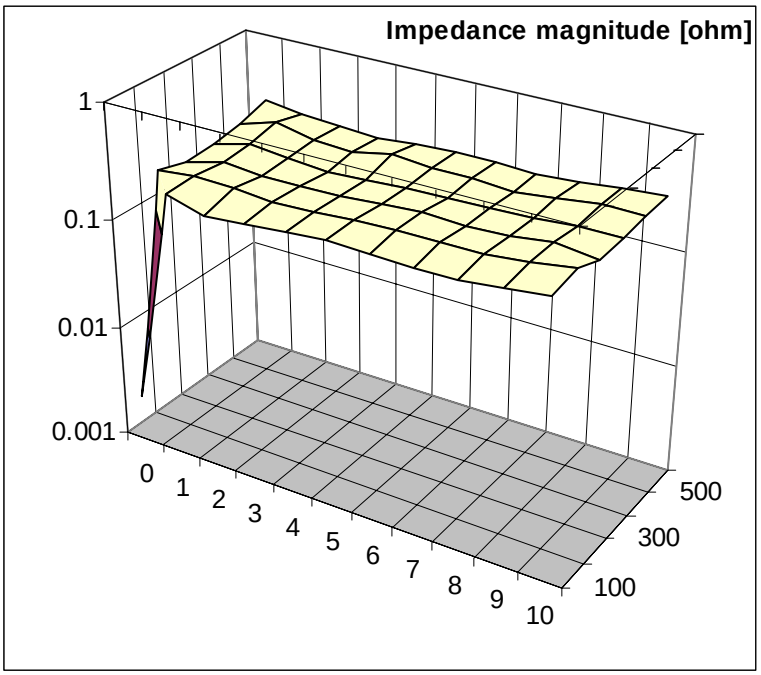
Courtesy of SUN-East

Self-impedance magnitude at 100MHz, along the surface of the board.



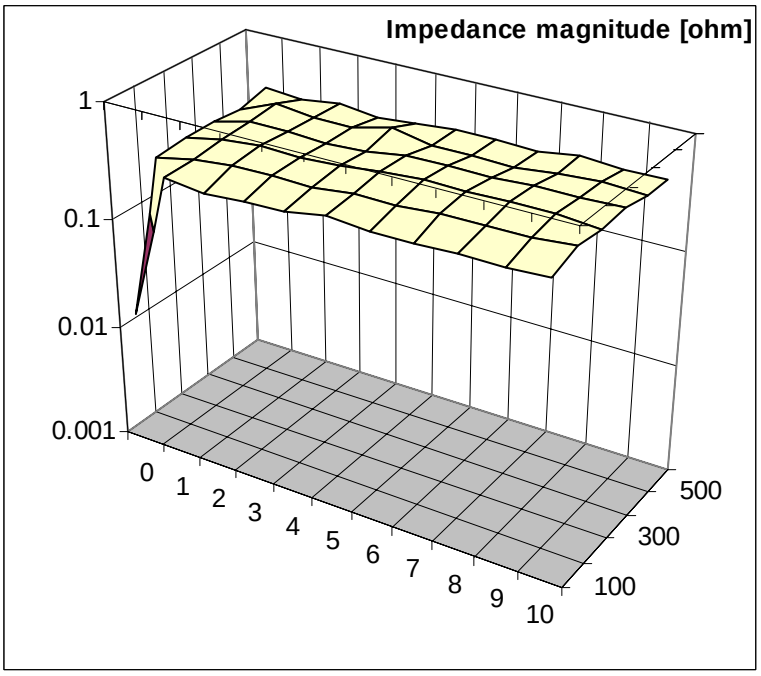
Courtesy of SUN-East

Self-impedance magnitude at 300MHz, along the surface of the board.



Courtesy of SUN-East

Self-impedance magnitude at 1000MHz, along the surface of the board.



Courtesy of SUN-East

Self-impedance magnitude at 1800MHz, along the surface of the board.

Conclusion

1. Material E provides the best performance on impedance among all three ink type materials.
2. Material C and D are both a more cost effective way for build up process.
3. With roller coater, we can achieve very thin dielectric.

Further Action

1. Keep on improving the yield rate on both Material D and E.
2. Material D needs to have a impedance testing.
3. Material D and E need further researching to be done.
4. Optimize break down voltage test of Material C, D and E.