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Conference panel

Board and Package Level PDN Simulations

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Abstract

This panel will feature software users presenting company "wish lists," features of simulators that are considered necessary or useful, but either are not available today, or not in a fully functional manner. The purpose is to orient software companies to focus on features, which are the most important to many of the end users. To support the wish lists, the panel members will submit simple challenges for the software vendors, for which the answer is either obvious (can be found by simple speculation) or repeatable measured data exist, and these challenges, representing the sought-after features, can be handed over to the software vendors after the panel discussion.

Sergio Camerlo, Director, Engineering, Internet Systems Business Unit, Cisco Systems. Mr. Camerlo's current organization is strongly focused on high-speed interconnects and packaging technology and its application to products.Sergio's work on signal, timing, power integrity, and high-speed board /backplane layout engineering has recently been complemented with the addition of substrate and packaging design for ASIC and Advanced Modules (MCP and SiP). Several new products benefit from the successful application of advanced disciplines and methodologies developed through Sergio's organization and leadership. The most recent and visible result is the Next Generation Catalyst 6500 family, whose physical layer and overall packaging (ASIC, card, board and backplane) results from specific and fundamental work of his organization. Mr. Camerlo is also chairing the Cisco Switching Patent Committee and is involved with the industry and academia to foster the development of new high-speed interconnects and packaging materials and methodologies.

James Drewniak, Professor, Electrical Engineering, University of Missouri, Rolla, is one of the principle faculty in the Electromagnetic Compatibility Laboratory. His research and teaching interests include electromagnetic compatibility in high-speed digital and mixed signal designs, electronic packaging, and electromagnetic compatibility in power electronic based.

Jun Fan, Senior Hardware Engineer, NCR Corporation, is focused on signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, PCB noise reduction, and differential signaling. Dr. Fan received the Conference Best Paper Award from the Applied Computational Electromagnetics Society in 2000. He serves as secretary of TC-9 Computational Electromagnetics Committee of the IEEE EMC Society.

Ravi Kaw, Chip Package Co-Design and Signal Integrity, ASIC Products Division, Agilent Technologies, has published over 25 papers in the areas of device physics, IC processing, and packaging, and currently holds three patents. Dr. Kaw received several Best Paper Awards. In 1994 he received SRC's Outstanding Industrial Mentor Award. He chaired EPEP in 1999 and 2000. He is a Fellow of IEEE.

JP Miller, Distinguished Technologist, Industry Standard Servers, Hewlett-Packard, is working on advancing the development technology used in ISS. Mr. Miller has been with Compaq and now HP for 17 years designing desktops and servers from the first Systempro server. He represented Compaq on the InfiniBand specification development.

Alex Waizman, Principal Engineer, iMPG Design Center, Intel, is responsible for the package design, motherboard integration and package and mother board power delivery in developing the Centrino ^{TM} microprocessor. He has previously worked on a variety of analog-related topics including: Ethernet physical access, delay line and phase locked loops, high-speed testing and high speed IO design.

Istvan Novak, Senior Signal Integrity Staff Engineer, Sun Microsystems, is engaged in the design and characterization of power-distribution networks and packages for workgroup servers. He creates simulation models, and develops measurement techniques for power distribution. Mr. Novak has more than twenty years of experience with high-speed digital, RF, and analog circuit and system design. He is Fellow of IEEE for his contributions to the signal-integrity and RF measurement and simulation methodologies.

Part I. Modeling/Simulation of Power Distribution Networks (suggestions for incremental advances)

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I. Introduction

Modeling tools for power distribution networks are a relatively recent offering [1]. These tools did not exist a decade ago and their debut is constantly challenged by a rapid increase in clock frequencies coupled with tremendous increases in power demands at ever reducing voltages [2]. In the past, IC systems used inter-chip signals that had much lower frequency than the on-chip signals. This trend is changing and even reversing itself. The advent of mixing digital and RF signals has complicated the issue further. Digital systems are also supposed to allow the use of several voltages that have different noise/impedance characteristics. Fortunately there has been a great surge in the development of tools that can address some of these issues [3,4], but more needs to be done. The old tools depended on a methodology of quasi-static modeling of various physical components of packages/boards. These sub-circuits are then connected together for simulation. Unfortunately this methodology is limited to low bandwidths. Today's designs demand switching less than one volt in about 50psec, which translates to bandwidths of 7 GHz and a very small noise margin. Any tool that is being developed in 2004 must address issues for several years down the line. This means handling systems that clock at 5GHz in 2005 to 12 GHz in 2010, according to 2001 ITRS roadmap. This also means that the tool should create broad-band models rather than single frequency models. These broad-band models must be spice-compatible, so one can connect active circuits to them seamlessly. This demands use of EM-CAD that is computationally complex, yet leverages advances in fast solver technology, fast processor speed, and parallel distributed computing. All these tools could use *Model Order Reduction* (MOR) to enhance their computational efficiency.

II. Suggested approach

For the short term, existing tools could be enhanced to support incremental upgrades that are summarized below.

1. Standalone modeling tool for P/G structure of PC Boards should have the granularity of the package balls (pins). The modeling tools for packages are generally more advanced than the ones for PC Board Power Delivery Networks. One can define each power and ground pin of the package as a node but the corresponding pads on the board are not defined individually. Thus one is forced to short all power balls/pins together. This is an obvious over-simplification.

2. Package P/G modeling tool that yields peec models of reasonable/usable size, using MOR techniques. Most commercial tools provide peec models of the P/G network but these are often large and cumbersome to use. A lot of research has been done in the area of MOR that needs to trickle to the commercial tool level.

3. Package/PCB modeling tools that model vias of various complexities accurately. This is true of power and ground vias as well. Simply treating vias a cylinders is no longer acceptable because their broadband behavior depends on the various couplings at each layer.

4. Package/PCB modeling tools that yield broad-band models of reasonable/usable size. This is a universal MUST for all tools.

5. Package modeling tools that include models for a portion of the PC Board stack-up that extends a cm or two beyond the package. This is a compromise for systems that are simply too large to handle. Chopping off a section of the PC Board is a convenient "divide & conquer" technique. Nodes should be defined at the reasonable intervals at the edge of this board for P/G, so one can add noise sources to mimic an actual full-board operation.

6. "On-chip P/G grid" modeling tool that is reasonable in size and complexity. This may call for statistical methods for assessing electrical performance. It is no longer acceptable to define an entire ASIC as a current sink. The on-chip power grid has its own granularity and current sinking characteristics. Several attempts have been made to model this, but none have been translated into commercial tools.

7. Combined package modeling and on-chip P/G mesh modeling tool.

8. On-chip loading schemes with hierarchical representation of circuit blocks to reduce complexity. This would be a method to reduce the complexity that one encounters with such full-system problems. This could be handled mathematically or as equivalent circuits representation.

9. Tools to model 3D E&M effects (delay and radiation) for reasonably complex structures with greater computational efficiency.

10. Easy-to-learn/use hook-up to simulation tool(s).

11. Tools that 'teach' rather than just model. These should have visual aids for current flow.
There is a great need to help users visualize what they model. This is especially true of return currents. Smart engineers use intuition to accomplish this and that often means dependence on highly qualified individuals to do modeling.

12. Willingness to accept the latest R&D work done at Universities in a win-win manner.

13. Tools should have the capability to clip-off OR add-on lines and planes and passives to give the user a better handle at "what-if".

14. Tools should include sensitivity analysis as a rule, considering that most packaging/PCB structures have geometrical tolerances of 5 to 10%.

15. Ability to model planes that have holes, cuts, and are occasionally meshed.

16. Ability to treat the actual cross-section of a trace rather than approximate it with a rectangle.

The list can go on and on, but most suggestions are simple extensions of the state of the art. These changes are needed now and should be implemented without delay.

References:

1. Speed-2000 & Power-SI from Sigrity Inc.
2. 2001-ITRS Roadmap
3. SI-Wave from Ansoft.
4. PakSI-Wave from Optimal Corp.

Part II. HP Discussion of a Wish List for Power Integrity Tools

JP Miller, Hewlett-Packard

I. Introduction

Hewlett-Packard is a company of diverse businesses encompassing printers, servers, consumer products, and PCs among others. I have elected here to concentrate on server applications because designers of servers seem to be at the forefront of signal integrity and power integrity investigation. Even selecting from among servers as I have for this discussion there are several kinds of servers, which demand differing design methodologies. In addition due to mergers and geographic separation diverse cultures have led development teams to take differing approaches to power integrity design. So I have attempted to look for themes that recur rather than list every desire.

Users of power integrity tools in servers range from specialists who sometimes have advanced degrees in engineering and do research to explore the boundaries of our understanding of signal and power integrity. They often write and develop custom tools to serve their needs and have the sophistication to fully understand the capabilities and limitations of such tools. At the other end of the range are engineers who primarily develop the schematics and supervise the layout of printed wiring boards. They are little interested in the technical subtleties and would utilize power integrity tools to provide answers that will get them quickly from a block diagram to a reliably functioning PWB.

There are two basic types of organization in need of tools. One includes specialists as part of a signal integrity service organization that provides most of the signal integrity input to a design team. The second type is the stand alone design team organized around a specific product development. This second organization consists primarily of the schematic and PWB layout engineers. Such a team may or may not have an engineer on the team who is somewhat specialized in signal integrity. Since the two types of organization are in different business units the communication between them has so far been ad hoc.

In general the specialized signal integrity organizations have done more formal evaluations of tools. The other organizations tend to use a tool when it is clearly needed immediately and it is clear it will provide immediate results. Tools that I know have been investigated by one group or another include Sigrity Speed 2000, Ansoft HFSS and Cadence Spectraquest. One group has used Speed 2000 for a couple of years and portions of Spectraquest have been used as well. Several planned in-depth evaluations of each of these tools have floundered for various reasons. Several other tools including Flo/EMC have been looked at. None have found widespread use. The most heavily used tools have been internally developed. Many designers depend on spreadsheets, hand calculations, expert recommendations, gut guesses and over design.

One final industry factor looms large. It is the trend toward multiple power domains for each semiconductor device in a system with those domains often not shared with neighbor devices. This has greatly increased the complexity, cost and delay in power system design by forcing additional layers and split layers into our designs. Power system design has become much harder.

II. The Panel Charter

Areas not covered by tools

Existing tools are very weak in three areas. The first is in modeling of noise sources. When asked what should be put into their tool to represent the noise sources some vendors reply "that's up to you." Well that is just not good enough. Many more experienced engineers can come up with a guess as to the di/dt of a package knowing the number of switching outputs. But he has less information about the inductance or capacitance of the package or on-die which will limit that di/dt. Nor does he have good information about what the core transient currents will be. Nor does he have a good idea how long a current step may be maintained from the semiconductor by design. Nor does he know how often such steps of current will take place so he can explore lower frequency power resonances. The experienced signal integrity engineer knows to get this information but then needs a good way to incorporate the information for package simulation and to later make a more simplified model for system simulation.

One engineer suggests: Tools should adequately model the semiconductor chip and package so the internal behavior of the package can be explored for resonances in the C-L-C loops involving on-chip bypass and package inductance. Both transient and AC analysis can be useful. AC sweeps can be utilized to uncover package resonances and to generate impedances to synthesize a simplified model of the package. This can usually be done with fewer than 20 elements. Provide tools which can generate, from the complex detailed model of a semiconductor chip on a multi-layer package substrate, a simplified model more suitable for supporting PWB simulation with many devices installed.

 The board design engineer on a tight schedule does not have the ability and time to construct such models and needs assistance. This could be in the form of prompts for the right information and how it can be estimated if it is not vendor supplied. Entry into a tool of the current vs. time profile of the semiconductor or the packaged device with the ability to convert it to a periodic form and then sweep the period over a large frequency range would allow exploration of the system design for resonances.

The second area of major shortcoming is in helping to decide what is good enough. Again the tool vendors indicate this is up to you. True, it is. Ultimately you must decide how much noise you want to tolerate in your system. But one methodology, for example, is to set a uniform low impedance target across the whole frequency spectrum. This is clearly not necessary when viewed at the board or system level. The semiconductor device package attenuates the noise from the device before it gets to the board. The harmonic content of any switching taking place in the device is down tens of dB at high frequencies. And even if the noise is present on the board it gets attenuated going into a victim package where it might have done harm. All this suggests a goal of much higher power plane impedance may be acceptable at higher frequencies. The users of this tool would benefit from drawing a more realistic impedance vs. frequency goal. The board power distribution system will not need to be so good as otherwise predicted. But again the engineer needs help. What he really wants to achieve is a low enough noise level that no harm ensues. The tools need to accept vendor supplied frequency dependent noise budgets as input.

In design it is very important to do rapid what-if prototyping. Quick reconstruction to modify one or a very few parameters one at a time is subsequently needed. One of our specialists has produced his own tool that converts sketches from a standard drawing tool into meshed 3-D SPICE models. It allows very fast investigations that can be turned around and simulated in a couple of hours. The vendor supplied tools require a lot more time and a higher level of expertise on the part of either the signal integrity engineer or the board design engineer on a PWB CAD tool. Such tools are often used by highly skilled operators working for sub-contractors. Such a scenario is an ill fit for the highly interactive what-if

process. If the CAD operator follows his usual process he will get too far along to incorporate conclusions from the what-if process. Tools should incorporate rapid construction of geometric models for these exercises. Vendors usually claim to have this ability but the people I have interviewed do not agree with this claim.

Another area of need for the system designer is in understanding the role of the power supply. Some tools incorporate a simple power supply model of a Voltage source, inductance and capacitance. But again it is up to you to define the model. The power supply is a feedback control system with a transfer function. Many power converters now can respond in the microsecond range to massive current changes. They need large amounts of low inductance low ESR capacitance to respond to the fastest of changes. Slower changes are handled by the feedback control system. The tools allow one to attach a model to a simulation (although it is not clear all can provide for remote sense lines.)

Again this is an area where the power integrity tools are not the only help needed. I have been told many power supply designs are never modeled and simulated because good models for the control devices are not available until years later. But what I think would be helpful is a behavioral model of capacitance, inductance and the closed loop response of the power supply. The tools need only provide the attach point including remote sense, the ability to run a SPICE like model and the ability to simulate all the way to DC for Voltage drop. Tool vendors could also help standardize the behavioral model and its connection.

There are lesser shortcomings in the design process. One tool provides a part by part means of estimating the layout dependent inductance associated with a bypass capacitor which can then be applied to a collection of capacitors. This tedious aspect of entering data in the pre-layout design could be overcome in the post layout simulation where the pads, nets and connection to the plane of bypass capacitors could be captured automatically and the associated placement inductance calculated automatically.

Almost all designs have multiple power/ground plane pairs to support multiple Voltages but now many designs also have multiple power/ground pairs of the same Voltage to support very high currents. Sometimes two or three layers of 2 oz copper are needed for current. Modeling capability to determine the interaction of these multiple layers is needed.

In addition many systems designs employ multiple boards.   Some systems may be racks of uniform boards plugged into a backplane. Many at HP are irregular boards plugged into irregular places in a mother board often drawing power through a connector as well as supporting high speed signals. There are two problems associated with multiple boards that tools could address. The first is just the logistical one of smoothly integrating a complete power analysis in a multi-board system. The tools can not do this consistently now.   The more difficult problem is to simulate the effect of connector impedance and the high currents on the ground potential across such connectors.

The theme running through this discussion is that power integrity analysis tools should be an integrated part of a comprehensive design methodology. There is a need to cover both pre-layout design with easy to use what-if analysis and post layout design verification with automated capture and simulation of layout dependent aspects such as capacitor footprints. There is the need to explore the fine geometric details of a multi-GHz package and to simplify the models for quicker analysis of boards and power supplies down to DC. There is need for complexity and accuracy to satisfy the SI expert and the speed and agility while still giving meaningful results for the PWB design engineer. And finally there is a

need for simplified standardized modeling of semiconductor devices and power supplies as part of a system power simulation tool.

III. Features needed in tools

The following is a list of some of the features needed in tools:

1. Tools should be modular in construction so the design can be easily debugged.
2. Clearly defined portions of tools can be used by beginning designers to get feet wet and incorporated into previously established methodologies.
3. We need quick entry capability because we can not rely on CAD tools to do the what-if analysis. By the time a respectable CAD design is done it is often too late to make power design changes.
4. The structure of a comprehensive design methodology should be built into the tool.
5. Substantial self-guided tutorials should be utilized to beef up on-line help.
6. Tools need to extend DC to calculate Voltage drop and current handling.
7. Voltage drop and ground effects should cross board and device package boundaries.
8. Tools need to handle multi-GHz frequency ranges to cover package resonances as dimensions approach ½ wavelength.
9. Provide a mechanism to include the tolerance of semiconductors to system noise as goals into the power integrity tool.

IV. Services needed of tool vendors

Tool vendors can help make their tools more attractive by providing some of the following services.

1. Work with other tool vendors to standardize interfaces especially between package and board and board and Voltage regulator. Any vendor's model should be an easily included file in any tool vendor's power integrity simulation.
2. Make it easy for users to incorporate models of current vs. time of semiconductor chip into the system simulation in the case where the vendor does not supply the package model.
3. Work with semiconductor vendors and power converter vendors to establish models to standard interfaces and encourage them to provide models to users.
4. Encourage semiconductor vendors to establish standard representations of noise tolerance.

V. Services needed from others

At the risk of redundancy I would like to list what people other than the tool vendors can provide to help.

1. Semiconductor vendors need to deliver detailed standardized current vs time data and package characteristics in a simplified format to be included in simulation.
2. They also need to provide susceptibility of their devices to system noise as a function of frequency.
3. We need to get across to semiconductor vendors just how much cost they are adding with multiple power domains and they need to respond in their designs.
4. Power supply behavioral models should be provided by the power supply vendors that reflect simplified versions of the closed loop response, the output impedance and the load line of the power supply

VI. What we need to add to the mix

We need to help ourselves.

We should insist that our semiconductor suppliers provide current vs. time profiles for the power sections of their devices as they now provide IBIS or SPICE models and multi-pin coupled package models as they do now with their IBIS and SPICE models so we can explore the power distribution in the package and develop meaningful models to use to design power distribution at the board level. In lieu of the last we should ask that our semiconductor suppliers provide simplified current vs. time models with package models suitable for use at the board level. We should encourage them to participate in standards setting so these models fit easily into the tools provided in the marketplace.

Likewise we should induce power supply vendors to provide behavioral models that adequately represent simplified versions of the closed loop response, the output impedance and the load line of the power supply. They should provide inputs to their models for remote sense lines.

We need to take active steps to drive more of the work associated with power deliver to early stages of the design process. It is extremely hard to change stackup, plane cuts and splits and to insert additional bypass without disturbing routing which may already be in place. We should be more analytic about it to reduce costs by using power integrity tools

VII. Final words

As a result we view the solutions to the power integrity design process as having many dimensions one of which is the power integrity tools. I have tried to present material pertinent to the theme of the panel but have brought in more to set the context. The increased power levels, faster logic and the proliferation of power domains have conspired to make the systems design task more onerous. Any relief from this onslaught would be welcome.

Part III. NCR's View on Board-Level Power Distribution Network Modeling

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I. The PDN is an integral system including both chip-level and board-level components

The power distribution network (PDN) is a challenging while critical design aspect in high-speed printed circuit boards. It is a complex system comprised of components with mixed geometrical scales, such as on-chip power grid/on-chip decoupling, chip package, board-level power/ground planes, and board-level decoupling. This presents a challenge, especially for a full wave modeling. Although it is possible to analyze chip-level and board-level components separately, modeling the power distribution network as an integral system is more important and more beneficial for circuit designs. The focus of this panel discussion is board-level PDN design. But, to achieve a good board-level design, knowledge of the IC chips is also necessary. For example, the concept of PDN target impedance provides a basis for a board-level PDN design. To determine the target impedance, current requirements for ICs (drawn from the board) need to be analyzed. A common practice assumes the currents are constant over frequency, which can result in significant over-design. If actual current requirements in frequency domain can be modeled in the chip-level with package and board effects included, a more precise goal for board-level PDN design can be obtained.

II. A tool for generating design rules

Printed circuit boards are getting more and more complicated and difficult to lay out with the increasing data rates and decreasing component sizes. In addition, product cycle is becoming shorter and shorter. All these make it impractical to completely model all details and pieces of the board during layout. Design rules still play an important role. Correctly designed rules can help layout technicians do a quick and relatively good job in certain situations. Therefore, such a modeling tool is desirable for generating rules that can precisely model the details of some PDN geometries, not necessarily being super fast and capable of modeling all the geometries. But the modeling should be accurate and robust. Even in the board level, the PDN geometries may have mixed scales, for example, a small via versus a large solid plane.

III. A tool for post-layot evaluation

A modeling tool is needed after board layout complete, to evaluate the performance of the designed PDN as a whole. The tool should be fast, and capable of modeling most, if not all, of the PDN geometries simultaneously with acceptable accuracy. If design objectives are not achieved, the tool should be able to identify the areas for improvements. Again, this tool should be fast since a few iterations may be needed to achieve all the design goals.

IV. Transition is also a source of power noise

Simultaneous Switch Noise (SSN) is well known as a major source of power bus noise. The spectrum of the generated noise voltage due to SSN has both odd and even harmonics of the fundamental clock frequency. There's another mechanism that can cause power bus noise but often neglected in PDN modeling. In multi-layer printed circuit boards, there are intentional signals, such as clock, bus signals, or other fast switching signals, often transitioning from one signal layer to the other through vias. If these vias trespass the power/ground plane pair (power bus), the signals can be coupled to the power bus, and thus resulting in power bus noise. A unique characteristic of this noise is that it only has odd harmonics if the duty cycle of the transitioning signal is close to 50%. Reference capacitors and ground vias help mitigate this noise, but a tool is needed to identify these hot spots on a post route basis then determine how many reference capacitors and ground vias are needed. In addition to power bus noise and resultant EMI, signal integrity can be an issue as well resulting in a reliability problem.

V. Location, location, location

When an IC device switches state, it draws current from the PDN. We know that although some charge is stored in the power/ground plane pair (at low frequencies it is a parallel-plate capacitor), most is available from decoupling capacitors. Every decoupling capacitor has a parasitic inductance. From a time-domain point of view, inductance always impedes the change of current. Therefore, it takes time for the charge that is stored in the decoupling capacitor to be available. The larger the inductance value is, the slower the delivery of charge. Intuitively, decoupling capacitors should be placed close to IC devices, since the capacitor that is close to the IC forms a smaller loop, thus a smaller inductance in the loop. In the real world, things are more complicated than that. The inductance of the loop not only is a function of the distance between the capacitor and the device, but also depends on the layer stackup, capacitor pad designs, and capacitor package size. In some cases, such as a thin power/ground plane pair, the effects of the distance to the inductance value may be negligible compared to those of the others parameters. Therefore, in these cases, capacitor locations are not critical. By knowing this, they can be placed where room may be available and critical space can be saved for signal routing. In other cases, such as a thick power/ground plane pair, locations are important, and capacitors shall be placed as closely to the ICs as possible. A good modeling tool shall be able to analyze the effects of the capacitor locations with all factors considered, and quantify the benefits of local decoupling (placing a decoupling capacitor closely to an IC device) to provide adequate information for a board designer to make correct choices between decoupling benefits and routing flexibility.

VI. Time-limited analysis

When an IC device switches state, it draws current only within a short period of time. As we discussed earlier, not all decoupling capacitors on the board will participate as current sources within the limited rise/fall times. Only those that are placed close to the switching device can make charge available within the rise/fall time are effective for this particular switching device. Furthermore, although charge is stored in the entire power/ground plane pair, not all the charge is available during the logic transition as well, since it takes time for charge to travel from where it is stored to where it is needed. To analyze whether there's enough charge available for a device's switching, a time-limited analysis is preferred in the time domain. By focusing on only a limited period of time (on the order of the rise/fall time), the elements that participate the transition can be easily identified, and it is clear whether there's enough transient current available by monitoring the displacement currents both on the power/ground planes and through the decoupling capacitors.

VII. Choice of individual capacitor values

In regarding the individual capacitance values for surface mount technology (SMT) decoupling capacitors used in the PDN design, there are two common "conflicting" approaches: one promotes using the maximum available capacitance values within the selected package sizes to achieve a low power bus impedance at the high frequencies and a high overall capacitance at the low frequencies; the other promotes using an assortment of capacitance values to obtain a wide and flat impedance response over frequency. The modeling tool should be able to analyze the two approaches under the same conditions (and others, if appropriate), and provide advice as to which approach is more effective for the particular situation. The tool should allow the designer to make a decision as to which approach he wants to use, or to decide on its own what values and placement to consider. The tool shall consider all factors such as capacitor package parasitics (ESL and ESR values), board stackup, board dimensions, vias and pads, etc.

Losses in PDN designs:

Losses are everywhere in a power distribution network: there are parasitic resistive loss associated with the decoupling capacitor (ESR); dielectric loss associated with the dielectric layers between the power and ground planes; skin-effect loss of the copper planes (power/ground); and, lumped element resistive loss elements that may be placed in series with the decoupling capacitor. Various measurements and modeling have demonstrated that losses are beneficial for PDN designs, since they usually damp resonant peaks otherwise shown in the impedance profile of a PDN. It is well known that the lower the impedance of a PDN, the better its performance in reducing power bus noise and in mitigating radiated emissions. There could be both lumped and distributed resonant peaks in the impedance vs. frequency curve of a PDN. The lumped peaks are due to the series resonances of capacitances with inductances, while the distributed ones are due to the geometrical parameters of the power and ground planes. Any peaks are undesirable for a PDN since they indicate a potentially larger noise voltage generated by the same amount of noise current at each peak frequency. By adding losses to the PDN designs, the unwanted peaks can be reduced. For example, the "embedded capacitance" has been found to be electrically superb for power bus noise mitigation. An embedded capacitance layer actually is a very thin power/ground plane pair, usually with a thickness of a few mils to a few microns. By decreasing the layer thickness between the power and ground planes, skin-effect losses are increased on the surfaces of both copper planes. The increased skin-effect losses cause the resonances completely disappear and the overall impedance magnitudes are very low. The modeling tool needs to include all loss elements into considerations, and shall be able to handle ultra-thin power/ground plane pairs with thickness as thin as a few microns.

Dense pin field in power bus:

Most modeling tools that have been developed in the past for power integrity of high-speed printed circuit boards have focused on solid reference planes (power/ground planes), and treated the injection point of the noise as a single point in an otherwise solid power/ground plane pair. However, the noise sources are often high pin-count packages with footprints spanning several square centimeters. Because of the density of the solder balls, e.g., for BGA parts, the power/ground layers beneath the package footprint are not solid, but rather a mesh pattern that conforms to the spacing of the solder balls on the BGA part. Further, the power network on the package substrate is a similar type of mesh geometry. The impact that the mesh geometry has on the impedance seen looking into the power network at the silicon, and the limitations in transient current draw associated with it is presently unknown. Modeling shall be able to determine the impedance and transfer functions associated with the PCB mesh geometry, as well as the package substrate. In particular, the impact of the conductor mesh on the power/ground planes on the PCB shall be determined. The transfer function associated with the package itself also needs to be determined.

Part IV. PDN Simulation Tool Requirements – SUN's View

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I. Introduction

The design of *Power Distribution Network* (PDN) is becoming increasingly difficult with the ever higher number of different supply voltages, higher operating frequencies and faster signal edges. The design challenges embrace the entire system, starting on the silicon, and ending at the power entry point of chassis. Good design practices, resulting in good power delivery without unnecessary over design, require adequate simulation tools to predict the behavior of PDN. While each part and section of the PDN may be equally important, here we focus on the simulation tools for package and board power-distribution networks: silicon power distribution and detailed simulation tools for power-conversion circuits (DC-DC and AC-DC converters) are beyond the scope of this summary.

The power-distribution network should provide the active devices with clean power, where the transient voltage fluctuations are within specified limits. The excitation of the PDN is coming from the signal currents and active devices' core currents. In a complex, software-driven system, the transient excitation current is hard to predict. To circumvent this problem, the PDN can be designed in the frequency domain, to meet a specified self and transfer impedance profile. This requires the proper accounting of all major frequency-dependent effects along the PDN.

Besides providing clean power to the active devices, a large portion of the PDN usually serves also as return path for various digital (and possibly also analog) signals. Single-ended signaling is directly vulnerable to the fluctuation of the reference path, while differential signaling offers some degree of isolation. Voltage drops and fluctuations along the return path may get transformed into common-mode and differential-mode noise components, directly superimposed on signals. Correct accounting for *Simultaneous Switching Noise* (SSN) contributions requires a proper modeling of the return path of signals, which may be different at different frequencies.

Because the PDN physically encompasses a big part of the system, noise appearing on the PDN may create not only signal-integrity issues, but also *Electromagnetic Compatibility* (EMC) problems. Capturing the near-field and/or the far-field radiation from a PDN with complex geometry is a very challenging task. As a first step in preventing EMC issues, the key requirement is the proper capturing of potential structural resonances.

II. List of required features in power distribution simulation tools for packages and PCBs:

II.1. Handle irregular plane outlines and large internal cutouts

The challenge in this feature is to properly capture the structural resonance frequencies due to irregular outlines and internal cutout shapes of PDN planes. Some tools use transmission-line grids to simulate PDN [1]. If the tool uses a crude approximation of the plane shapes, the discrepancy between measured and simulated modal resonance frequencies can be significant. One example was described in detail in [2]. On the left, Figure 1 shows the outline of one of two plane shapes sharing the same layer, having a non-rectangular outline and a large cutout. A uniform rectangular-outline grid approximation is superimposed. On the right, the measured self impedance versus frequency is shown, with the simulation result from the rectangular-outline uniform grid. The rectangular uniform grid approximation has an impedance minimum at a frequency, where the measured impedance has a peak.
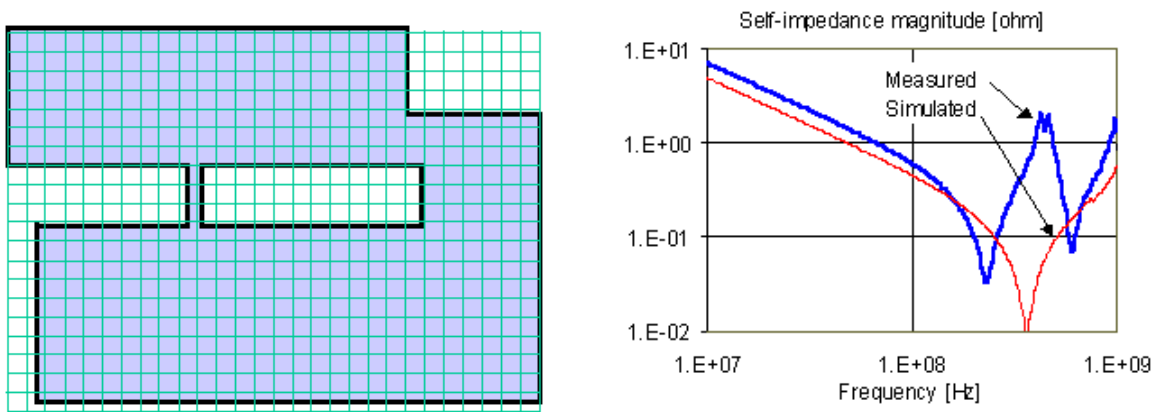
Figure 1: Topology and measured/simulated impedance of a non-rectangular plane shape.

II.2. Handle multiple paralleled plane pairs of possible different shapes/sizes, including vertical via connections

State-of-the-art packages often have multiple plane pairs supporting the power distribution and serving as reference planes. Printed-circuit boards of medium and large computers also tend to have multiple plane pairs for the same reason. Multiple plane pairs may be needed simply to provide sufficiently low DC resistance. In this case, the distribution of voltage drop along the paralleled planes connected through vias may be of primary interest. At high frequencies, the structural resonances of different-shaped paralleled plane pairs will interact, and this interaction has to be correctly simulated. The challenge is to properly capture the PDN's behavior from DC up to the highest frequency of interest, including DC drop and complex modal resonances.

II.3. Handle various degrees of plane perforations due to antipads, thermal connections, and other small holes in the self and transfer impedance calculations of PDN

The PDN planes are very seldom full planes: there are several reasons why the planes may be sprinkled with smaller and bigger voids. Vias and through holes not connecting to the particular plane require clearance holes (also called antipads) on the planes. For manufacturing reasons, some vertical via and through holes, which do connect to the particular planes, may have a set of small voids at the connection

point, called thermal relief, connecting the via barrel through a number of spokes to the plane. Finally, the board may have smaller and bigger holes on the planes, or through the entire board, for mechanical reasons. Dictated by the construction technology, some packages and some printed circuit boards may require meshed planes or planes with various sizes of vent holes.

As illustrated for various geometries in [3], depending on the relative location of metal voids with respect to the potential standing wave pattern on the planes, a relatively small missing area of the plane may result in significant shift of modal resonances and distortion of impedance profiles. A typical scenario is under large packages, also in connector areas, where the vertical connections can significantly perforate the planes. Sometimes the small perforation holes tend to blend together to form cuts and slots on the planes. Plane perforation also increases the plane's resistance and inductance.

There are multiple challenges here. Simpler is the transfer impedance calculation, where the connection points are outside the perforated area. In this case the challenge is to properly capture the shift of structural resonances. Figure 2 is an illustration of possible shifts in the transfer-impedance profile due to various sizes of narrow rectangular slots on a board.
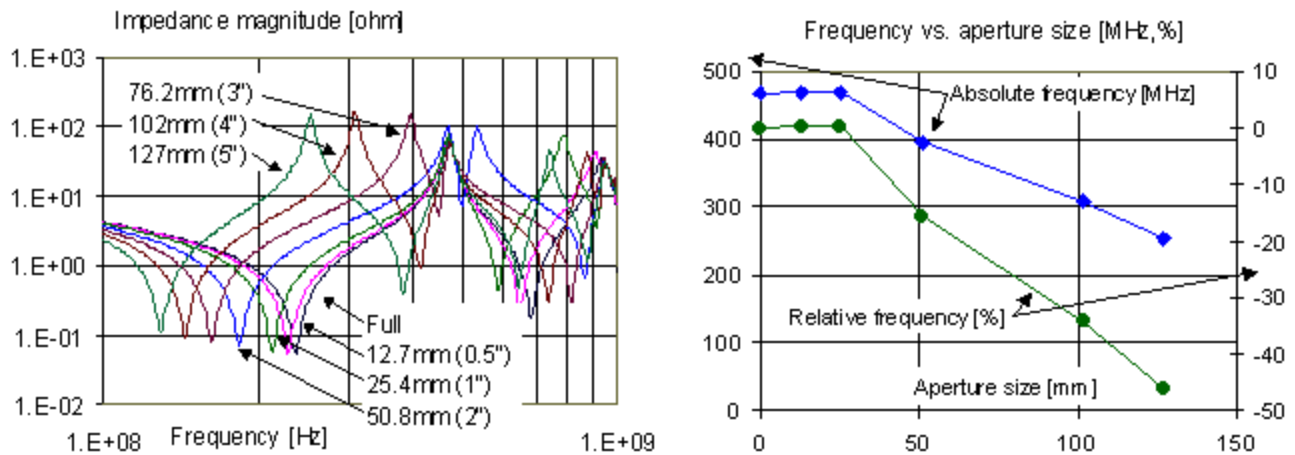

Figure 2: Measured transfer impedance along the shorter side of a 152mm x 102mm (6"x4") test board, with various length of a rectangular 0.8mm (0.03") wide slot from the side. On the right, the frequency shift of the first modal resonance peak is shown under the same conditions.

A bigger challenge is to capture the self impedance of the perforated area with reasonable accuracy. The self impedance can be defined at connection points on the surface of package or the PCB, but in this case the self impedance contains the series impedance of the connecting vias. The PDN impedance presented by the PCB planes and connected bypass capacitors may create a much smaller impedance, which might be overwhelmed by the series via impedance. This is illustrated in Figure 3 (on the left), where a thin laminate's self impedance is measured in different configurations (Figure 35 of [4]). The board had an 8um thin PDN laminate closer to the top surface. The three curves of the graph refer to measured self impedance taken on the top pads of vias (label: Near side), on the bottom pads of vias (label: Far side) and by measuring with one probe on the top and the other probe on the bottom pads (label: Opposite sides). This third trace represents the actual self impedance of PDN with no series via impedance.

Self-impedance magnitude of bare board with 8-um laminate [ohm]

Far side

Near side

Opposite sides

Frequency [Hz]

Self-impedance magnitude, measured [ohm]
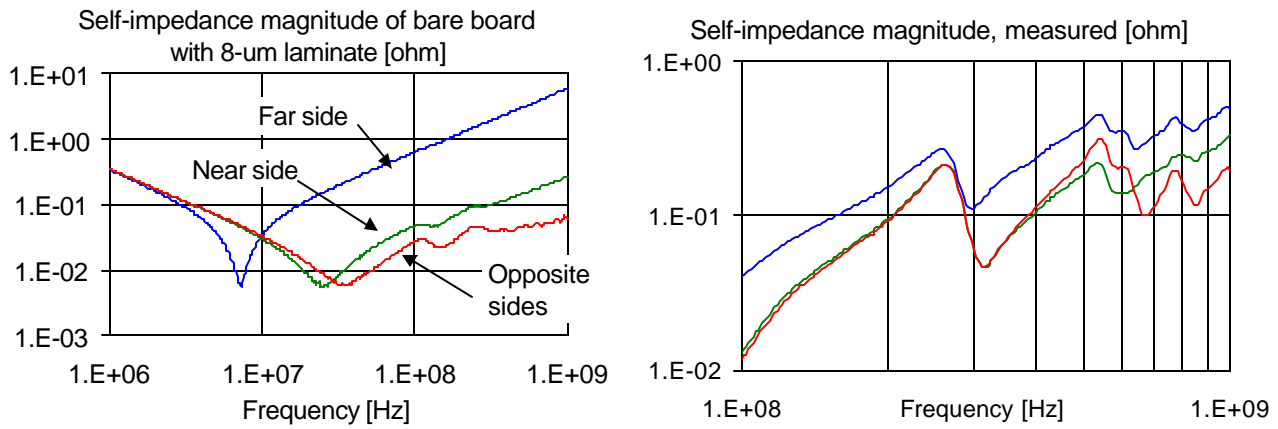
Frequency [Hz]

Figure 4: Measured self-impedance plots of PDNs. On the left, self impedance of a bare board, measured with and without vertical via connections. On the right, self impedance of a bare board, with three different local perforation patterns.

The right-hand graph in Figure 4 shows the measured self impedance of a bare test board, similar to described in [5], where the three traces on the graph represent various degrees of local perforations. The lowest-running trace had only the one pair of test-connection vias, with no nearby perforation. The middle trace had two additional antipads 2.54mm (100 mil) away. The topmost trace had three additional antipads nearby.

II.4. Handle the coupling and resonance-pulling effect among adjacent plane-pair cavities through splits and openings

Density requirements often force designers to split metal layers into separate power-plane shapes. These power-plane cavities may or may not share a common ground plane, but in either case, the dielectric gap of the split creates a small coupling between the cavities. Similarly, in a vertical stackup of a multiplayer board, otherwise electrically independent power nets may be coupled through the vertical dielectric separation and/or splits in the planes. The challenge here is to capture and properly account for the coupling among the various nearby cavities. Figure 5 illustrates this coupling (from [3]).

Impedance measured, simulated [ohm]

Simulated

Measured

Frequency [Hz]

Impedance magnitude [ohm]

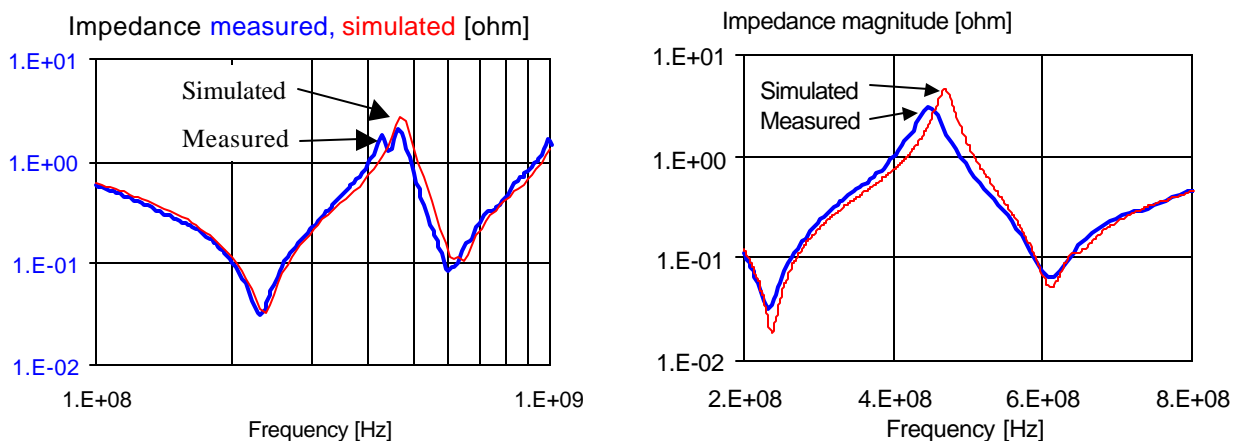Simulated
Measured

Frequency [Hz]

Figure 5: Illustration of coupling between adjacent plane-pair cavities. Measured and simulated self impedance with adjacent cavity present (on the left) and with adjacent cavity physically removed (on the right). Note the double peak of measured impedance with the adjacent cavity present

II.5. Seamless integration of large package and board files, extracting PDN contribution to signal-return path bump-to-bump, extracting frequency-dependent return path geometry

The challenge is to integrate separate large board and package files with minimum user interaction, and to properly account for the return path through the PDN along the entire length of connections.

II.6. Include frequency-dependent bypass capacitor and plane models

Upon closer inspection, basically all components used in PDN exhibit some degree of frequency dependence in their capacitance and/or inductance. The challenge here is to properly model the frequency dependent effects (see e.g., [6]) and to incorporate the suitable model in the simulation tools. Obtaining the accurate data for the PDN components may rely on measurements. Figure 6 shows a few illustrations of frequency dependent capacitance and inductance values of bypass capacitors and power/ground planes ([4], [7], [8]).
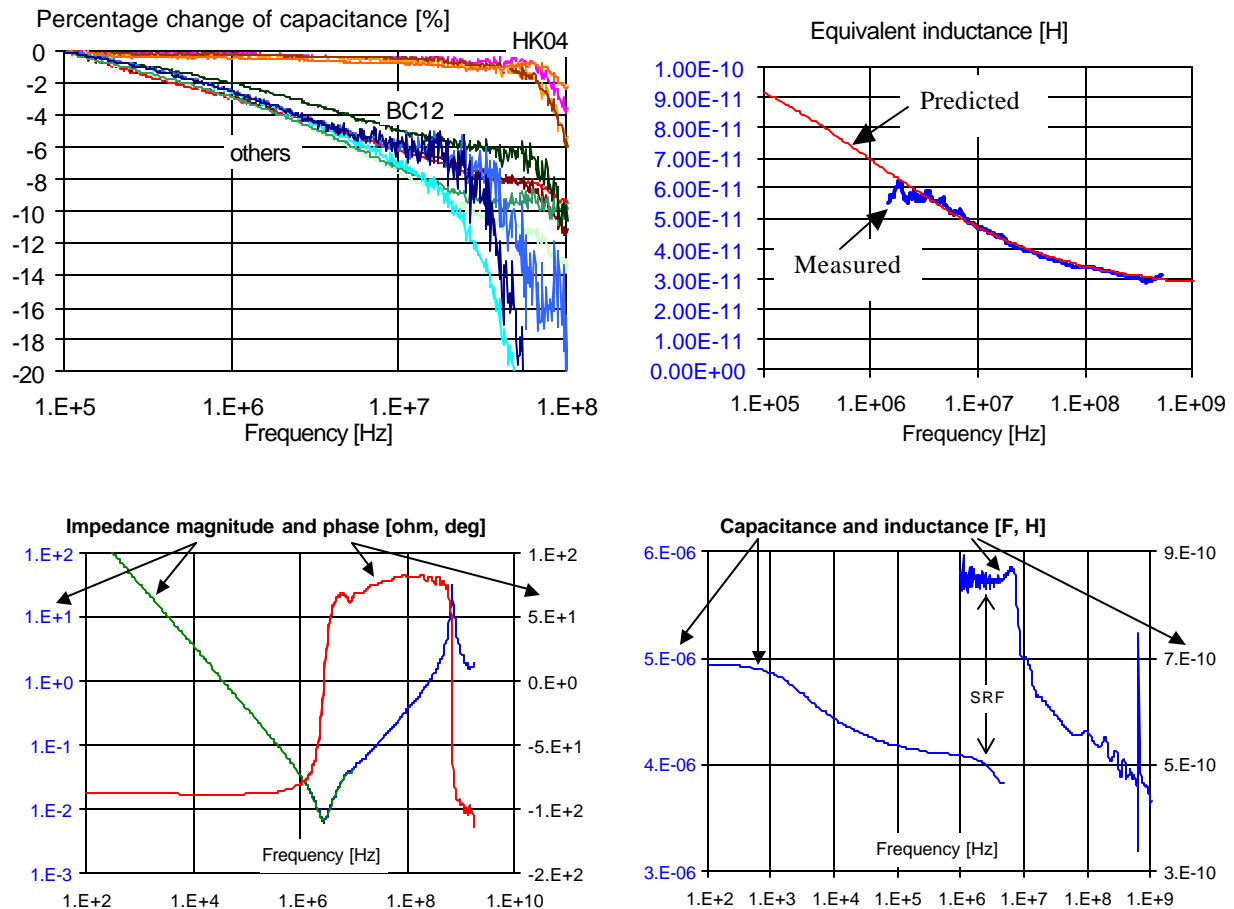
Figure 6: Illustration of frequency dependency of PDN components. On top left: comparison of percentage change of static capacitance of thirteen different thin power/ground laminates (from [8]). On top right: measured and estimated frequency dependent inductance of a 1-mil polyimide laminate with two-ounce copper on either side (from [8]). Lower left: measured impedance magnitude and phase plot of a 4.7uF 0508 ceramic bypass capacitor. Lower right: the extracted capacitance and inductance versus frequency curves for the same part (from [7]).

Acknowledgements

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Part V. Power Distribution Network Modeling and Design for High-Speed Digital Systems

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1. Considerations for PDN Design – Time-Domain (SI) and Frequency Domain (EMI)

An adequately designed power distribution network serves different functions, depending upon the direction from which the design is approached. In one case, the function is to supply sufficient current at a rate that allows for proper functioning of the IC devices, while maintaining adequate noise margins for *signal integrity*. In this case, the non-ideal effects are dominated by time-limited artifacts including the impact on rise time, overshoot/undershoot, and ringing. These design issues are *time-domain* considerations. From another perspective, the switching IC devices are sources that result in noise over a wide frequency range, which is distributed throughout the digital system as a consequence of the power distribution network. The noise can be coupled off the PCB by various paths resulting in *EMI*. The design objective is to mitigate this noise by reducing the noise voltage over frequency on the PDN, which might be achieved through a low-impedance network as seen from the IC device power pins. In this case, the design issues are *frequency-domain* considerations. Both sets of design objectives must be met, and an ideal design tool would have good functionality in the time- and frequency-domain.

The significant design issues for the PDN are relatively straight-forward to enumerate. In this perspective, only multi-layer PCB designs that use entire layers, or large area fills for power and ground are considered. Specifically, the design choices include:
*   layer spacing and stackup,
*   surface-mount capacitor locations,
*   surface-mount capacitor value(s),
*   power/ground layer materials – high ε_r materials, loss
*   noise isolation/segmentation of power areas
*   signal routing and noise coupling to/from the power areas
*   total capacitance value required – power areas, components

By and large, these design choices are currently determined using a combination of simulation and study on problems of limited complexity, and previous design experience in a "best engineering design practice" approach, i.e., establishing design guidelines. The shortcoming of this state of affairs is that as the data rates and design density increase, and logic levels decrease, a quantitative evaluation of a design

is needed to meet increasingly stringent specifications. In the absence of mature, and robust tools for PDN design, the consequence is over-design. It is worth noting at this juncture that the above list can be divided into two groups. The first six items are PCB/package related. The seventh, however, is IC device related, i.e., requires an adequate IC model at the power pins to assess the required total capacitance needed in the design.

2. PDN Tools for Design

Ideally, suitable design tools would be available for design discovery and development of guidelines, as well as pre- and post-layout analysis. The objectives, functionality, modeling accuracy, speed, and user might be different in each case; however, a necessity for engineering is a sophisticated graphical user interface that facilitates model development in the easiest manner possible. In the case of design guidelines, the concern is to include in as complete a fashion as possible all aspects and geometry associated with a well-defined geometry. Specific examples of problems might include noise coupling resulting from a via transition through the power layers, or extracting the impedance of the package/PCB interface. These geometries are truly 3D, and for fast devices can require full-wave (formulated from Maxwell's equations) numerical modeling using FEM, MOM, or FDTD. The solutions will be very good for a well-defined geometry of minimal to moderate complexity. Care is required to model all the essential features and physics at hand, including non-ideal geometry effects such as conductor cross-section, or interconnect non-uniformity at sufficiently high data rates. A single simulation can be quite time-consuming, and many simulations may be needed to understand the relevant physics and develop a design guideline, or extract a desired circuit model. These tools typically require users with expertise in EM, numerical modeling, and the intricacies and nuances of the particular tool being used. In addition, the set-up, and model development time is significant. There are a number of very good, and mature tools commercially available for the various numerical electromagnetic modeling methods – MOM, FDTD, and FEM.

An objective of a pre-layout tool is to provide guidance, preferably quantitative, for first pass design and for choices that may be difficult or cumbersome to change, once the board is fully laid out. Examples include layer stack-up, plane splits and segmentation, IC placement, SMT capacitor location and value, and routing of signals that might transition through the planes and couple noise to/from them. In addition, a pre-layout tool should help provide insight, and be a learning resource for PDN design. The level of complexity of the modeling would be moderate, and include the power areas, multiple planes, arbitrary plane geometries, plane splits, cutouts, mesh fabric resulting from device pin and BGA fields, and models for the power draw from ICs. This type of pre-layout tool would quantitatively make A/B comparisons for PDN design, even though the un-certainty resulting from the reduced complexity would not provide absolute information for the SI impact on any given net or specific EMI levels. The output would be time-domain waveforms at a device terminals or open-circuit voltages on the planes, as well as frequency domain noise on the PDN. The users of such a tool might be designers and SI engineers that have a knowledge of circuits and the physics at hand, but not necessarily experts in computational electromagnetics. The model development time would be minimal, and the run time would be very fast, on the order of minutes, or a few tens of minutes. Ideally, it would be compatible with industry standard SPICE tools so that additional model complexity beyond the PDN could be included. At least one tool is commercially available that fits some of these aspects. However, a serious "fly in the ointment", with regard to PDN design in general, is the lack of IC device models at the power pins, which impacts all tool development. With this last exception, a good pre-layout tool is very achievable.

Finally, there are post layout tools. A post-layout tool would read in the board design files, perform a quantitative analysis with known uncertainty, sufficient for predicting the SI impact on critical signal nets at a device, and noise on the planes, both in the time- and frequency domains. The tool would be usable by designers and SI engineers. The model development time would be negligible, since the board files are read in from the design tool. Finally, the run time should be relatively fast, and the tool should provide feedback and guidance on problem areas, or optimization. Presently, there are no such tools, and the challenges in developing it are significant.

3. Models, Modeling, and Measurements

Suitable pre- and post-layout tools for PDN design require good models for circuit simulation, including interconnect models, models for non-ideal planes and materials, and IC device models. The types of interconnect models include chip-to-package, package-to-PCB, SMT components to the PCB, and via transitions through the planes. Non-ideal plane effects include arbitrary shapes, cutouts, splits, and other segmentations, as well as the mesh left by a device pin or BGA field. Also included should be material effects. Several different models for the planes, including the non-ideal effects and material properties have been developed that can be fast, and some suitable for a SPICE environment – both transient and swept- frequency response. Models for circuit simulation of the interconnects at all levels can be extracted from full-wave modeling, though the process may be tedious and time-consuming. The single greatest piece missing for the PDN simulation being considered here is adequate, or even rudimentary IC device models at the power pins. In the absence of device models, only A/B comparisons between two iterations of a design are possible, and no absolute assessment of the PDN design impact on signal integrity, or EMI is possible. Determining the total value of capacitance is then a "best guess" that often leads to over-design. Further, there is no quantifiable stopping point for the PDN design.

Modeling has to do with putting it all together – complexity, as well as determining accuracy, and uncertainty. For example, a via transitioning through the power/ground planes will require an interconnect model that includes a model for the signal path, as well as the coupling to the planes. The complete simulation must be put together from the component models to reflect the physics of the problem. The accuracy required of individual component models will be limited by the uncertainties in the design, including manufacturing tolerances and lumped element component values, e.g., the capacitors. Circuit model extraction for component models using full-wave numerical tools is also an "art form" itself, and will contribute to uncertainties in the overall PDN modeling.

A critical aspect of model development, and modeling, whether for interconnects, PCB planes, or devices, is making good measurements along the way to guide the model development, and modeling process. Critical types of measurements include swept-frequency measurements (frequency domain), e.g., a vector network analyzer, time-domain measurements, e.g., signals and eye patterns, and transient current measurements at device signal and power pins, in particular for large pin-count devices. With effort (often a great deal) and the right fixturing, measurements for verifying component models for interconnects and discontinuities can be made for model validation. However, a suitable method for measuring transient currents at the power pins of large pin-count ICs (for example with BGA packages) is currently unavailable, which is a significant impediment to model development for the IC in a PDN design tool.

5. The Ideal Tool and Challenges

Meeting the challenges associated with increasing data rates and design densities, as well as decreasing logic levels demands a sophisticated PDN post-layout tool. Such a tool would read board design files, and be able to include multiple boards within the simulation. Ideally, such a tool would be SPICE-based, or SPICE compatible. In addition to performing design analysis, the ideal tool would also provide design guidance for improvements, or even optimization.

The challenges for developing such a tool are primarily the overall complexity of the resulting PDN simulation, i.e., the sheer number nets, components, and power areas that might need to be considered, even for a limited portion of a design, as well as a proven and well-developed model library. The proven aspect of the library relates to adequately representing the physics and connecting the constituent component models back to measurements. The well-developed portion of the library relates to spanning the parametric space of common geometry variations of the library constituent models, as well as the IC device models. These challenges are not small, and this ideal may not be achievable any time soon. However, developing a good pre-layout tool specifically for PDN design is very achievable.