DesignCon East 2005

TecForum TF-MP2

Inductance of Bypass Capacitors

How to Define, How to Measure, How to Simulate

Presenters:

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Session organizer and chair:

Istvan Novak	SUN Microsystems, Inc.

Abstract

Have you ever wondered why the same size bypass capacitor is listed with different inductance from different vendors? Do you want to know how some of the major OEMs want the inductance to be determined? Are you interested in knowing how major capacitor vendors measure the inductance? This TecForum will give an overview of how consultants and OEMs (Xilinx, SUN) model capacitors, what are the important contributors to a capacitor's inductance in a real design, as well as how capacitor vendors (AVX, Kemet) do the testing. Participants who want a dialog with the presenters, can attend the panel discussion "Bypass capacitors: how to determine their inductance?"

This is a continuation of the TecForum and panel discussions at DesignCon 2005, Santa Clara, on the same topic, held by Sanyo, Taiyo-Yuden, Cisco, Intel and SUN.

Part I. A Measurement Technique for High Frequency Low Inductance Decoupling Capacitors

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Abstract

A method to characterize the behavior of high performance, low inductance decoupling capacitors using specially designed test boards has been developed. Fundamental to the approach is measurement of open and shorted characteristics of the test board so that board and capacitor contributions can be separated using modeling software. Simple C-L-R series equivalent circuits are not adequate for predicting component response of low inductance multi-terminal devices like IDC's. For these, a branched equivalent circuit model is minimally required for accurate circuit simulation. Details of the construction of the high frequency test board and the measurement technique are discussed along with examples of measured devices and correlations.

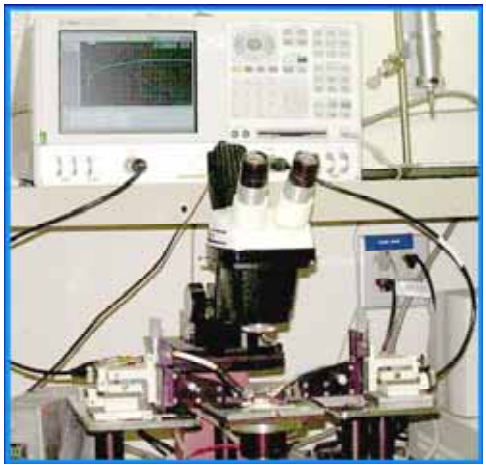
Introduction

System circuit designers are concerned with the electrical performance of the integrated load, substrate circuitry, mounted decoupling capacitor(s) and other "up-stream" components of the power supply network. In order to predict circuit performance, designers must have either s-parameter data or equivalent circuit parameters that accurately characterize decoupling capacitor behavior alone, over a broad frequency range, without influences of the specific test substrate or measurement techniques used to obtain the data.

Equivalent circuits of multilayer ceramic capacitors have traditionally been derived from a single series CLR network in order to describe the part's electrical response. This approach is accurate for a range from low- to intermediate-frequencies, i.e., for those frequencies that occur at or below the main series L-C resonance, and slightly above that resonance. This relatively simple analysis provides three critical parameters that are used to describe the component's behavior at high frequency; namely, Equivalent Series Capacitance (ESC), Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR).

Performance requirements for decoupling have migrated to increasingly higher frequencies, and as one result, decoupling capacitor designs have become more complex, evolving to include multi-terminal "interdigitated capacitors" (IDC's) that have very low ESL and ESR, and thus improved high frequency response. Network analyzer measurements of high frequency decoupling capacitors, like IDC's, reveal response characteristics that are not observed in less sophisticated designs like 2-terminal MLC's. One consequence of this is the realization that the simple single CLR series equivalent circuits cannot accurately describe the impedance behavior of the multi-terminal device for the entire range of interest frequencies, which now span from just below 1 MHz to ~10 GHz. Thus, improved models are needed that produce consistent equivalent circuit parameters for predicting capacitor performance over a wide frequency range. This paper summarizes work at AVX Corporation to design test boards, conduct network analyses, extract capacitor performance from the measurement "system" and fit data to equivalent circuit that give an accurate representation of component performance over a wide frequency range.

Equipment Description



Equipment for Capacitor Measurements

Agilent E8358A Vector Network Analyzer 0.3 MHz - 9 GHz
Signatone Probe Station
(2) - Cascade Microtech Mdl 101-117 Manipulators
GGB Pico-probe Mdl GS40A 500P
GGB Pico-probe Mdl SG40A 500P
Cascade Microtech Mdl 106-683 Calibration Substrate
Eagleware Genesis V8.1 Design Software

Figure 1. Data acquisition equipment includes a network analyzer, pico-probes and a high frequency test substrate.

Measurements of decoupling capacitors are done with commercially available network analysis equipment (Fig. 1). The device under test is mounted to a circuit board that includes test points for high frequency probes. Use of probes is preferred over high frequency connectors that complicate test board design and can give undesirable mechanical stress to the board and components. The network analyzer, cables and probes are compensated with short, open, load and through (SOLT) calibrations, using a purchased Impedance Standard Substrate. Network analyzer data files for the capacitors, and compensations of shorted and open test substrates are saved for manipulation in circuit simulation software, described below.

Test Board Design

Proper high frequency characterization of decoupling capacitors requires that they be mounted to a circuit board. The circuit board must be designed to approximate the substrate that will be used in conjunction with the capacitor in end-use, i.e., the substrate must have appropriate solder pad dimensions, trace widths, metallization weights, via placement and dielectric properties such that the parasitic high frequency behavior of the test substrate does not overwhelm the capacitor performance.

The test board is designed so that all positive terminals of the decoupling capacitor are connected to a common plane and all negative terminals are connected to another plane (Fig. 2). Solder pads for mounting the component are placed on the top surface of the board, where pad dimensions are taken from vendor datasheets. Connections from the top side are made with filled vias using at least one via placed in the center of the each solder pad. It is desirable to make the test board capacitance as low as possible, that is, the length and width dimensions are made small, so that board resonances are as high as possible and above the frequency range of interest for the decoupling capacitor. Test boards used for this work are 1 cm square and are made with Getek, a low K (3.8) and low loss dielectric suitable for measurements in the GHz range.

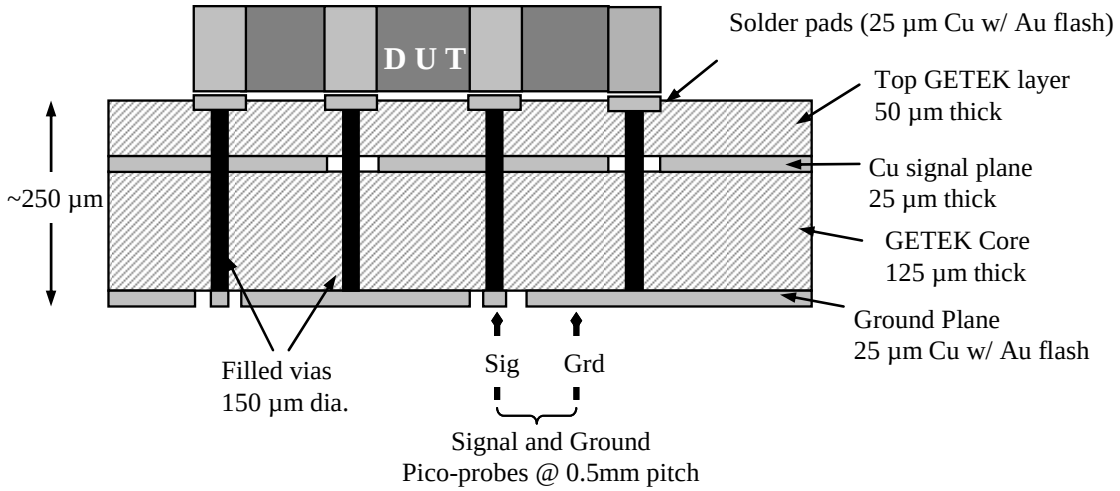


Figure 2. A cross-section schematic (not to scale) of the high frequency test board shows the layout and suggested dimensions.

Figure 3 shows photographs of the top and bottom sides of the test board along with a short-circuited board and a one with a mounted part. The IDC test board at AVX has a pad layout that accommodates both 8- and 10-terminal part styles by using a common row of solder pads as shown. A superimposed

profile on the photographs shows the relative location of an 8-terminal component. The short circuit is made using a piece of 0.25 mm thick brass foil, large enough to cover all of the solder pads, soldered in place. Both the brass foil and decoupling capacitor are mounted with a reflow solder method, using either SnPb eutectic or SnAgCu "Pb-free" solder pastes.

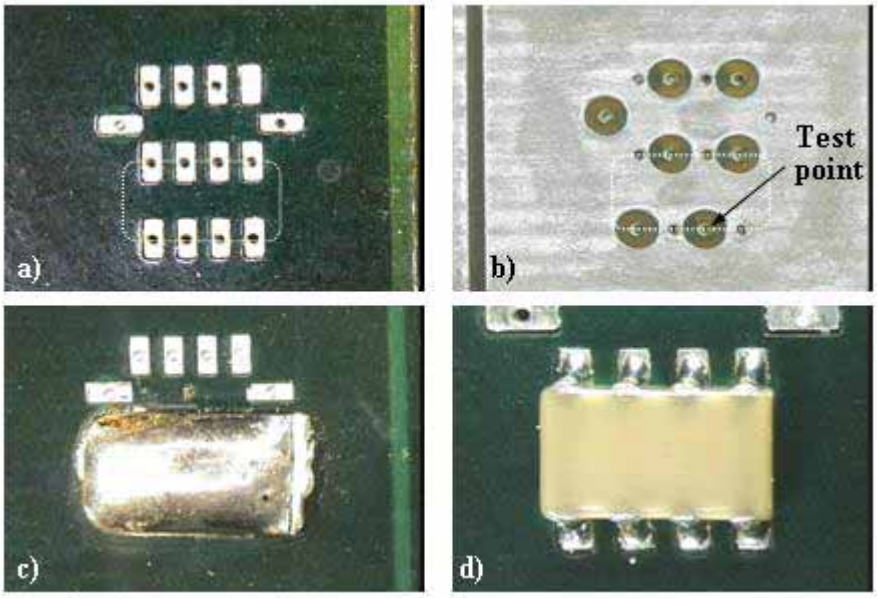


Figure 3. The IDC test board showing a) top (component) side, b) bottom (probe) side, c) test board with the soldered brass foil short-circuit, and d) mounted 0508 8T IDC.

Measurement Procedure

There are three sets of measurements needed for the characterization: 1) the open circuit board, 2) the short-circuited board, and 3) the board with the component attached. As described below, these data sets are used in conjunction with simulation software to determine equivalent circuit parameters and extract the decoupling capacitor-alone behavior from the measurements.

Measurement of Open Test Board

The test board should be characterized without any device mounted on it to determine the open-circuit board capacitance. In practical terms, the test board capacitance forms a parallel resonance with the component inductance. This resonance may be neglected as it typically occurs above 5 GHz for the test board as described above, in which case the measurement of the open circuit test board is not necessary. After proper SOLT compensation, the sets of pico-probes are placed on a signal via pad located on the bottom surface of the test board, as shown in Figure 2. Note that the center probe of both sets are placed on the same via pad, without touching each other, and the ground probes contact the adjacent ground plane on the board bottom. The scattering-parameters are collected in the S_{21} mode, or transmission loss in dB, at least, or the full complement of forward and reverse parameters may be recorded for more detailed analyses.

Measurement of Shorted Test Board

A short circuit is formed on a test board by soldering a piece of brass foil over the solder pads for the component. It is desirable to have continuous, yet thin, solder coverage on all pads under the foil. As

above, the board is probed from the bottom, using the same signal via used for the open measurement, and s-parameter data are recorded. Ideally, since the applied short is very thick relative to the board metallization, the brass foil has only a small contribution to the overall inductance and resistance measured for the test board. Typically, 3-5 shorted boards are prepared and measured, seeking repeatability of the fitted Rs (shorted resistance) and Ls (shorted inductance) of plus/minus 0.2 mohms and 3 pH, respectively.

Measurement of Capacitor on Test Board

The decoupling capacitor is reflow-soldered to the test board, ensuring that all terminations make contact and the joints have a robust solder fillet. Scatter parameters are obtained by probing the board from the bottom, again using the same signal via location used for open and short measurements. Measurements for the ceramic capacitor are delayed at least one day after soldering to allow the capacitance to stabilize after heating.

Modeling Component Performance

Modeling Software

Circuits consisting of lumped elements with 50-ohm ports as inputs and outputs are used to fit and describe the capacitor response, and *Eagleware*™ version 8.1 software (www.eagleware.com) is used for circuit simulation and modeling. Equivalent circuit models using a) a simple series CLR and b) a branched CLR network can be used to represent the frequency responses. Once the model is completed the raw measurement data is imported and compared against the model. An optimization routine is set up in *Eagleware* to allow the software to manipulate the circuit elements to achieve an acceptable fit between the model and the measured data.

Open Board Model

The open board model for our test board consists of a capacitor in shunt from a 50-ohm transmission line to ground. The modeled value of this capacitor is 12 pF. This value is small enough to be neglected relative to the decoupling capacitor, and, as mentioned above, will form a high frequency resonance in parallel with ceramic capacitor inductance that is a characteristic of the geometry of the test board.

Shorted Board Model

The shorted board is modeled as a series RL in shunt with a 50-ohm transmission line to ground. At low frequencies the inductive reactance of the test board is assumed to be zero and all of the measured impedance is from the resistance of the test board. The resistor value (Rs) in the model is adjusted to match the measured data at the low frequencies. As the measurement frequency increases the impedance of the test board due the inductance also increases. At high frequencies most of the impedance is due to the inductance of the test board and not the resistance.

To model the inductance the resistor value is held constant and the inductor value (Ls) is changed until the best fit between the measured data and the model is achieved. Basically, these parameters will exist in series with a DUT that will be loaded at a later time on the test board. The R_s and L_s have great impact on the measurements of the multi-terminal capacitor. For this reason, these need to be present as separate modeled elements in series with the device. Figure 4 shows the S_{21} sweep for the short-circuited IDC test board, resulting in substrate parasitics have been determined to be 1 mohm and 60 pH.

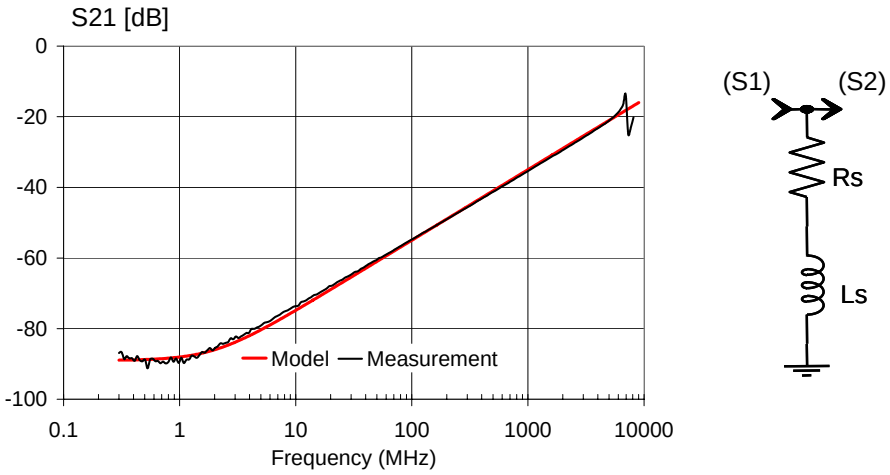


Figure 4. Measured S_{21} data and a fitted model for the shorted IDC test board give equivalent Rs of 1 mohm and L_s of 60 pH. The high frequency resonance is not modeled.

Board + Component Models: Simple CLR Fit

Traditionally, a simple series CRL network can be used to describe the high frequency s-parameter or impedance data for simple multilayer ceramic capacitors. However, for a capacitor with a more complex terminal structure like an IDC, this simple CLR circuit describes the data only within a limited frequency range.

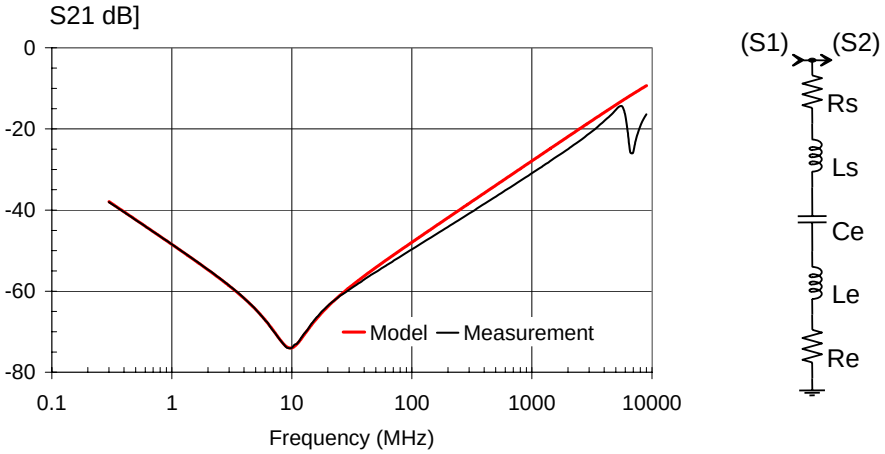


Figure 5. A comparison of measured S_{21} for a typical 0508 8-terminal 225 IDC and modeled values from a simple series CLR equivalent circuit shows good fit at low and mid frequencies, but the model over-estimates inductance at high frequency.

For example, for a 0508 8T 225 IDC the simple CLR circuit provides a good fit for the frequency range from 300 kHz up to slightly above the resonance point (~24 MHz for this device), but above that frequency the series circuit does not describe the high frequency inductive behavior. Starting with the board resistance and inductance determined from the shorted board analysis, the simple series CLR equivalent circuit fit to the measured S21 data is built in the a 3-part progression. First, the capacitance

value, C_e, is adjusted until the model fits the measured data at the lower frequencies (e.g., 0.3 to 3 MHz). Next, the model's inductance value, L_e, is adjusted until a fit between the model and measured data at resonance frequency is achieved and finally, the model's capacitor resistance, R_e, is adjusted until the magnitude of the resonance matches the measured data. This model fits the measured data very well through resonance, but there is significant deviation between measured and modeled inductive behavior at high frequency (Fig. 5). In order to better describe the both low and high frequency decoupling capacitor behavior, additional terms must be added to the simple series CLR equivalent circuit.

Board + Component Models: Branched CLR Fit

A branched equivalent circuit containing one capacitor and at least three (3) parallel series RL networks is required to obtain a good mathematical fit for the decoupling capacitor across a broad frequency range (Fig. 6). In all cases, the equivalent circuit models use the same board R_s and L_s that were obtained from the shorted substrate. In order to fit the branched circuit model to the measured S_{21} data, an optimizer function incorporated in the *Eagleware* design software is used, where the board resistance and inductance are not allowed to change. The optimizer routine runs iterations comparing the average error between the measured and modeled data sets, and the program is typically stopped when the error term reaches 1-2%. In this case, the IDC is represented by a total of seven variables, one effective capacitance term and three each for resistance and inductance. It is noteworthy that there is no single equivalent "*inductance*" or "*resistance*" for the multi-terminal capacitor that can be used to describe broadband behavior. However, the three individual inductance and resistance equivalent circuit values can be added in parallel to give a single effective L_e and R_e for the device. In general terms, the lumped L_e term relates to the high frequency range of ~0.1 to >1 GHz of the S_{21}, or impedance, behavior; the lumped R_e value relates to behavior at series resonance; and the C_e term relates to low frequency response.

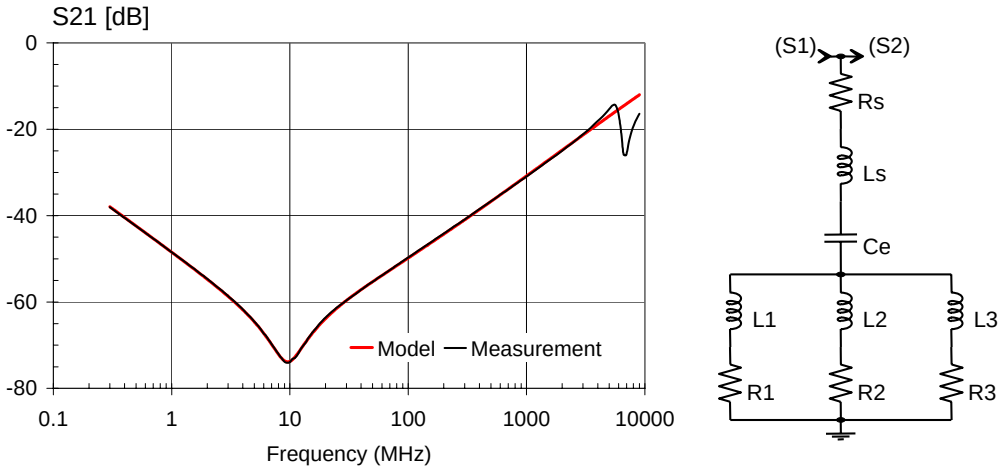


Figure 6. A branched equivalent circuit, with 3 parallel LR networks, fits measured S21 data for a 0508 8T 225 IDC over the entire measurement range, neglecting the parallel LC resonance that occurs above 5 GHz.

Predicting System Performance

The validity of the measurement method can be shown using the extracted S_{21} parameters for a given decoupling capacitor to predict the integrated board-component performance for different circuit board design. Figure 7 shows s-parameter data for two different short-circuited circuit boards, which as shown, have relatively small difference in resistance but large difference in inductive behavior, arising from differences in the internal design of the boards. A typical 0508 8T 225 IDC was mounted and measured on the standard AVX test board, and the component equivalent circuit values were derived by the approach of this paper. At a later date, an improved low inductance circuit board was obtained and the board was characterized by measurement of the open and short-circuited behavior. From these measurements, the equivalent R_s and L_s terms were determined and an equivalent circuit was constructed using the board parameters of the low inductance board and the IDC branched circuit parameters extracted from the standard AVX board. From this circuit, the predicted performance of the IDC on the low inductance board was made (Fig. 7).

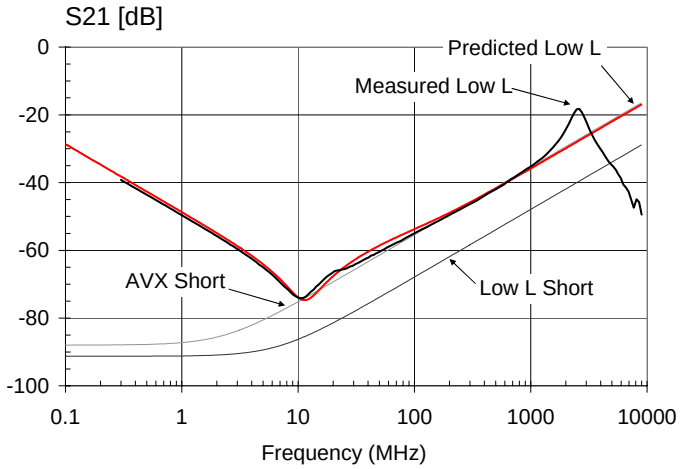


Figure 7. Extracted IDC equivalent circuit parameters can be used to predict measured combined performance of the component on different board types.

Finally, another IDC, with the same design but with a date-lot code 6 months later than the first device, was mounted on the low inductance board and s-parameters were measured. As shown in Figure 7, the agreement between the predicted and actual performance on the low inductance board is very good, showing the general applicability of the extracted IDC parameters.

Conclusions

Using special high frequency, low loss circuit boards, network analyses of multi-terminal decoupling capacitors give a measure of the component performance over a frequency range of 300 kHz to 9 GHz. A branched network equivalent circuit for the capacitor, and terms for the shorted test board resistance and inductance, allows simulation software to separate the capacitor behavior from test board contributions for the S_{21} measurement. This method has been applied to several styles of IDC components (Fig. 8).

	0612 16T 475	0508 8T 225	0508 10T 225	0306 10T 105
C_e (µF)	**3.85**	**1.91**	**1.83**	**0.86**
L_1	86	142	103	111
L_2	52	114	87	83
L_3	126	186	178	84
L_e (pH)	**25.9**	**47.2**	**37.3**	**30.3**
R_1	3.7	4.7	3.5	6.3
R_2	14	31	29	47
R_3	87	108	94	47
Re (mohms)	**2.8**	**3.9**	**3.0**	**5.0**

$1/R_e = 1/R_1 + 1/R_2 + 1/R_3$ $\qquad$ $1/L_e = 1/L_1 + 1/L_2 + 1/L_3$

Figure 8. Extracted branched equivalent circuit parameters for different styles of IDC devices give lumped CLR series equivalent circuit terms that allow easy comparison of the device styles.

The extracted capacitor characteristics therefore represent the performance of the capacitor alone and can be used to predict high frequency behavior of the component when mounted on a different circuit board, given knowledge of the new board's short-circuited behavior. Although neglected in this paper, measurement of the board's open circuit characteristics, i.e., capacitance, can also allow high frequency parallel resonances to be modeled.

Part II. Designing and Measuring Low ESL in Capacitors

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Abstract

A great deal of discussion has taken place at these conferences detailing the techniques and problems in measuring the effective series inductance (ESL) in low inductance capacitors. The most universal method utilizes a network analyzer and the test capacitor mounted as a parallel device in the source-analyzer coaxial line. There are other methods used for this analysis and we will discuss one here. Additionally, the ESL property is normally assumed to be a constant, but we will introduce evidence to show that this parasitic, like its companion parasitic, ESR (effective series resistance), may be changing with frequency. Although discussion of low inductance might appear to be the realm of multilayer ceramic capacitors, we will also detail a surface mount electrolytic capacitor as a low ESL product.

Defining ESL

Discussions about inductance in a capacitor may seem analogous to discussions about screen doors on submarines, but unlike the latter, the former does exist. Any time the current path is defined with a limited directional length, inductance will occur. In most two-terminal devices, the path exists within the structure or body of the device, from terminal A to terminal B. It is a force that is analogous to inertia in a mechanical system. Once a body is at rest, it tends to stay at rest and once a body is in motion, it tends to stay in motion. With inductance, the 'body' is current, and once a current level is achieved (as no current in an "off" state or as sustained current in an "on" state) the current desires to stay at those levels. The sustaining element in this current is the magnetic fields associated with the current and changing the current requires changing the magnetic fields associated with it.

The dimensional aspects of the capacitor may have a huge impact on its effective series inductance (ESL) and also contribute to the effective series resistance (ESR) of the capacitor. As the ESR was continually decreased, the application frequencies moved higher until ESL began to dominate the problems associated with high frequency decoupling and power filtering.

The Two-Terminal Capacitor

The capacitor has evolved from a leaded device to a surface-mount device and, as it's simplest diagram might predict, as a two-terminal device. The terminals may be found at opposing faces of the element as in axial leaded devices, or along a common face as in radial leaded devices. Although it is readily seen that the leads associated with through-hole devices add length and, therefore, inductance to the leaded capacitors, this increased path length is eliminated with the surface mount chip capacitor.

The inductance in any device, be it a conductor, resistor, or capacitor, is determined by the restriction in the width of the device established over the duration of its length. The higher the restriction is (narrower the length) the higher the inductance becomes and, the longer the duration is, the higher the inductance becomes. Consider a capacitor that is long and narrow: the path is defined over a long distance and a narrowly constrained path. This type of capacitor would have a high inductance associated with the dimensions of its structure. If the path was to be made short and wide, both the restraint and the duration is decreased, thus the inductance is decreased.

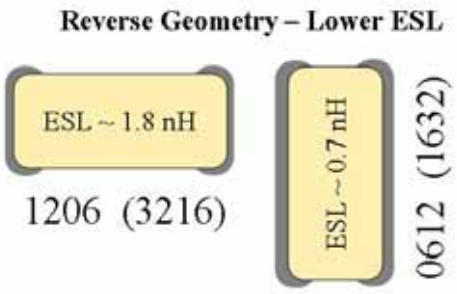

Figure 1. ESL can be improved with shorter and wider current path in the device.

Manipulating these effects for lower ESL would require that the capacitor be built as short as possible and as wide as possible. These devices are represented in the "reverse geometry," low inductance MLC (multi-layer ceramic) capacitor offerings. The 1206 chip becomes the 0612 chip (1206 is 0.120 in. by 0.60 in, and 0612 is 0.060 in. by 0.120 in.). This transposition results in decreasing the ESL by nearly

50%. This manipulation in manufacturing is not without added costs since processing these MLC capacitors is through equipment optimized to handle the traditional devices that are long and narrow, as opposed to being short and wide[1].

The aspect ratio limitation

There is a limitation to how low of an inductance can be achieved with the reverse geometry approach. If we consider the aspect ratio (AR) of the device as the ratio of the length divided by the width, the aspect ratio for the reverse geometry part previously discussed goes from 2 to 0.5 (1206 to 0612). Using the effects established with that conversion, it follows that the reduction of 50% in ESL should decay another 50% for each halving of the aspect ratio.

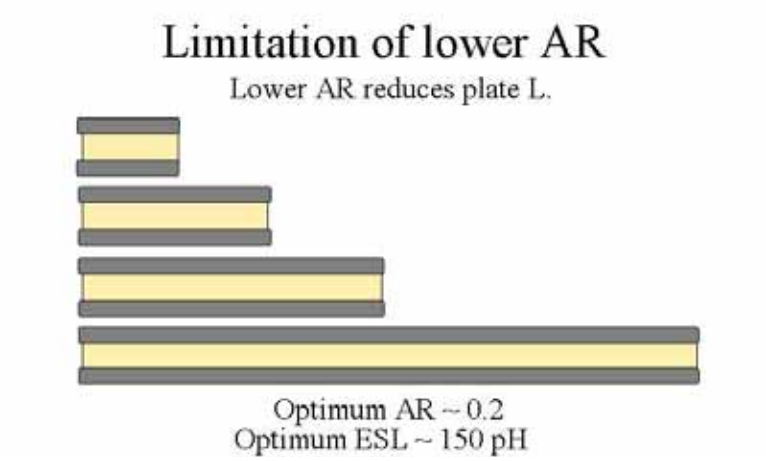

Figure 2. Improvement in ESL is not continuous with decreasing aspect ratios[2].

The problem is that this effect appears to no longer continue once the aspect ratio gets below 0.2 and this diminishing effect may be due to the charge concentrations. On each electrode plate, there is an unequal distribution of charge within the plate area. The peak concentration of charge will appear at the corners of the plate, along the edge that is opposite the termination edge.

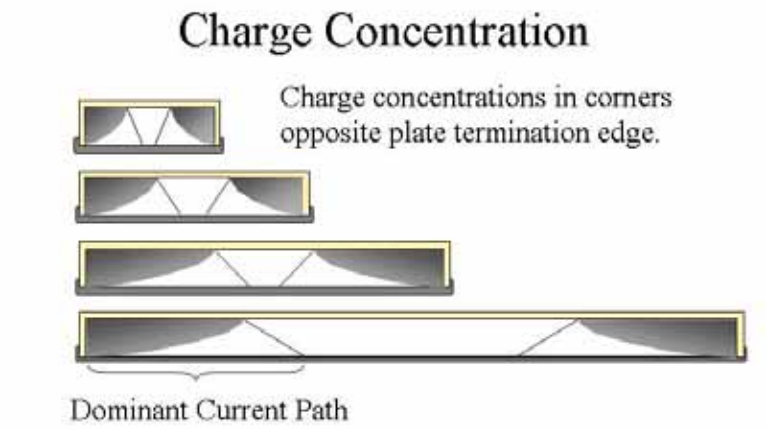

Figure 3. Declines in ESL with reduced aspect ratios may be due to effects on charge concentrations.

As the aspect ratio goes from 0.5 to 0.2, the charge concentrations on each plate may extend further into the center of the edge opposite the termination, allowing the charge and discharge current paths to extend to wider segments of the termination edge. As the aspect ratio goes lower still, the concentrations may cease to increase along the edge opposite the termination at the same rate as the changing aspect ratios above the 0.2 level. The current paths again may grow wider, but at diminished rates.

This effect may also be factored by measurement capabilities. For aspect ratios below 0.2, the calibration of the fixtures and the boards could have been misleading, but in all of our attempts to eliminate these influences, we were unable to see the continuing improvement with reduced aspect ratios.

The best capability we could measure for the reverse geometry devices was in the range of 150 to 200 pH. Mounting these on the PCB presented additional ESL as feed lines (traces) or vias to these capacitors from the power and ground planes added to the inductance apparent to the overall circuit.

Multi-Terminal Devices

These variations of the two-terminal devices allowed MLC capacitors to achieve ESL levels below 200 pH, but were limited there. Consider that the plate charge as depicted in Figure 3, required that the majority of the charge to travel from the termination edge of the electrode plate to the opposite edge of the plate and that the adjacent plates are terminated at opposing faces in the two-terminal capacitor. One plate is charging, and the plates immediately adjacent to it are discharging. The net effect is that the charges are moving in the same direction. Looking at the MLC structure, the initial logic might be that if these plates are inductive, then connecting inductive plates in parallel should create an effect similar to resistors in parallel: as more plates are added, the net ESL of the capacitor should decrease.

The laws of inductors in parallel do invoke a similar principle, but with the caveat that these inductors do not have any magnetic links to each other. These plates are separated by microns or fractions of microns and they do have a magnetic influence on each other (referred to as mutual inductance). This effect shows that, based on the self-resonance frequency, as the capacitance increases with increasing layer counts, the determined ESL (based on capacitance and self-resonance) also increases.

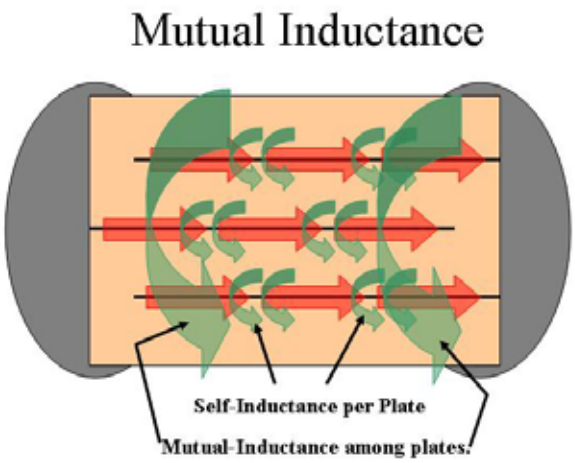

Figure 4. The ceramic MLC contains self-inductance of plates, and mutual inductance by association.

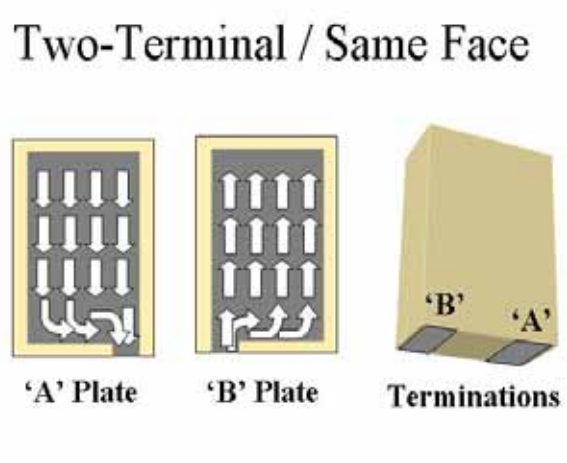

Figure 5. Here is a two-terminal capacitor with the terminations on the same face.

In order to reduce this effect, opposing terminations on the same face of the capacitor may be created. In this device as shown in Figure 5, the adjacent (oppositely charges) plates 'A' and 'B' are terminated along the same edge with each successive layer of ceramic. The terminations for these plates, 'A' and 'B' respectively, will appear along the same face of the ceramic block, once all the layers are stacked and the unit is fired. This arrangement will create some inductive cancellation since the charges on these two plates are moving in opposite directions, allowing the magnetic fields to cancel rather than reinforce each other.

This structure would require the capacitor to be of sufficient height (the dimension along the vertical axis of the drawing in Figure 5) to allow the current to spread out from the neck-down termination edge at the bottom edge to create the cancellation effects. In this instance, the ESL will improve compared to a two terminal device, but the ESR will increase due to the loss of contact length along the termination edge.

Now we referred to the vertical axis in Figure 5 as the "height" dimension, but that does not restrict this device to a board mount where the height is perpendicular to the plane of the board. Rather than sticking up from the board, it may be laid down such that the 'A' and 'B' terminations are arranged to be on a face that is perpendicular to the board, with allowance for both termination 'A' and 'B' to be mounted to adjacent solder pads on the board. In this case, the wrap around effects of the external terminations would allow this device to be mounted to the pads through the wrap-under termination. This presents an opportunity for adding more terminations along the other vertical faces of the capacitor body. These terminations could be repeated along the entire perimeter of the body - allowing for this sequence to be repeated a number of times, creating an interdigitated termination scheme for the device.

This interdigitated capacitor (IDC) scheme changes the charge distribution on the plate structure. As illustrated in Figure 6, the effect of feeding charge from opposing edges of the plate is that the charge concentrations to the opposing edge do not have to come from the terminals on opposite edges. For the two terminals at the top of the illustration, the adjacent edge along the top is also the opposing edge for the terminals along the bottom. The charges do not have to travel across the plate dimensions, thereby reducing the duration of the path. This results in reductions in both the ESL and the ESR. Also, consider that as the charge comes into the plate, it immediately fans out in opposing directions to fill the charge requirements along the feed edge (Figure 7). Charges moving in opposite directions create fields that interfere with each other, instead of reinforcing each other. The termination edges are repeated at multiple points, therefore eliminating the negative impact on resistance as attributed to the device in Figure 5.

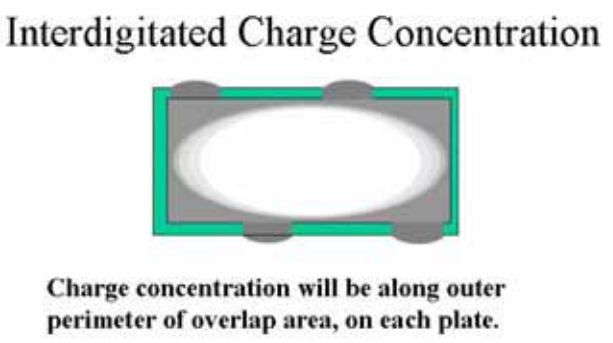

Figure 6. The charge concentration on each plate of the IDC is to the outer perimeter of the plate[3].

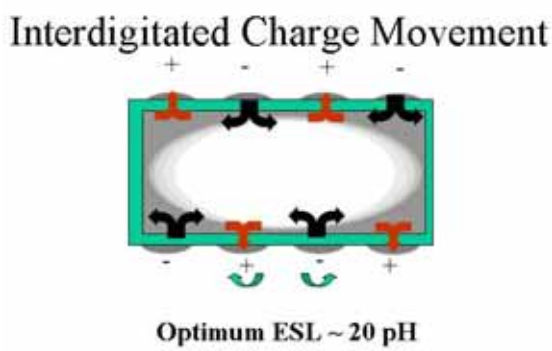

Figure 7. Charge movement within and into the IDC in opposing directions, adheres to cancellation goals[1].

Also, the terminations shown are for one plate. The adjacent plate would have terminations that would be directly across the chip, fitting in between those shown. The perimeter would create an A-B-A-B termination sequence along the top of the chip (left to right), repeated in a circular pattern around the center of the chip to another A-B-A-B sequence at the bottom of the chip (right to left). As illustrated in Figure 7, this presents another opportunity for inductive cancellation, as the feed of charge through the adjacent terminations is in opposing directions.

The Low ESL Conductive Polymer Capacitor

There are other methods used in attempts to minimize the ESL in MLC capacitors that cannot be pursued in this paper. The IDC is the dominant low ESL package that is gaining widespread acceptance and usage. The creation of the low ESL devices in the MLC package grows out of the high adaptability of its structure to these geometric variations of the package and termination designs that makes it so readily manipulated.

The adaptability of the conductive polymer capacitor is not as open as the MLC mainly because of its anodized pellet structure. In the process of creating the dielectric as an oxide of the base metal pellet structure. The anodization process restricts the feeds into the pellet structure to the same singular anode contact, though the contact to the cathode may appear on multiple faces. There are methods of multiple feeds being researched, but today, these are not production ready. As such, this device is pretty much restricted to the two-terminal device; but there are several things we can do to lower the ESL.

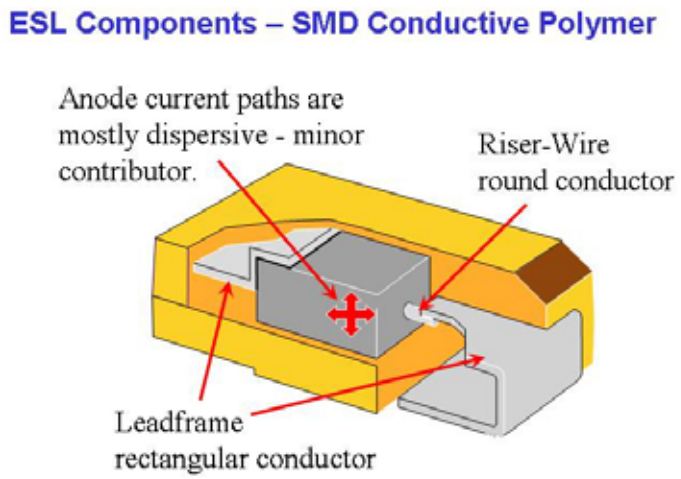

Figure 8. Here is a standard, surface mount conductive polymer capacitor[2].

Consider the two terminal capacitor and the effects created with the reverse geometry structure. Again, the conductive polymer capacitor does not lend itself to changing from a 7343 to a 4373, because of the anodization requirements. This device is packaged in plastic (injection mold process) and a leadframe is used to bring electrical connection from the capacitor's pellet structure out to a high-speed, pick-and-place plastic package for surface mount applications. That leadframe adds a lot of length (duration) to the current path for this device (Figure 8). At the anode connection, the leadframe extends from the middle of the package where it contacts the riser wire to the outside face of the plastic package where it is then bent down and under the end of the plastic body. At the bottom face of the device, this leadframe makes contact with the solder pad on the PCB. The cathode connection starts along the top of the pellet,

is bent down to the middle of the plastic body, then out, down, and under to repeat the solder pad contact. There is a lot of wasted volume created in this design. To be honest, it was that loss of capacitance volume that guided the development of the design without the leadframe. This loss becomes a greater percentage of the package volume as the chip size is reduced. In order to reclaim some of that lost volume the facedown design was created.

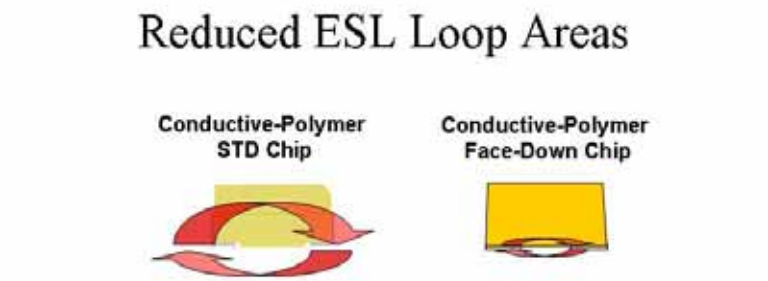

Figure 9. Illustration of reduced current loops afforded by facedown design.

The facedown terminations did allow us to recover that volume, but it was noted that it also created a lower ESL in the component. The reasons are the obvious loss of the leadframe's added length (duration) to the current paths. Looking at this effect as reduced current path loop area is illustrated in Figure 9.

The facedown termination pads created with the device on the right of Figure 9 are in immediate contact with the cathode surface of the pellet structure and the anode plate is contacted through a conductive spacer. The results of the conversion of the "T" case (3528-12) device resulted in a drop in ESL of over 50%. Again, this change was not to optimize ESL, but to increase volumetric efficiency. As a matter of fact, the space separating the anode and cathode termination plates was kept large to assure that this device could be mounted using existing "T" case solder pads.

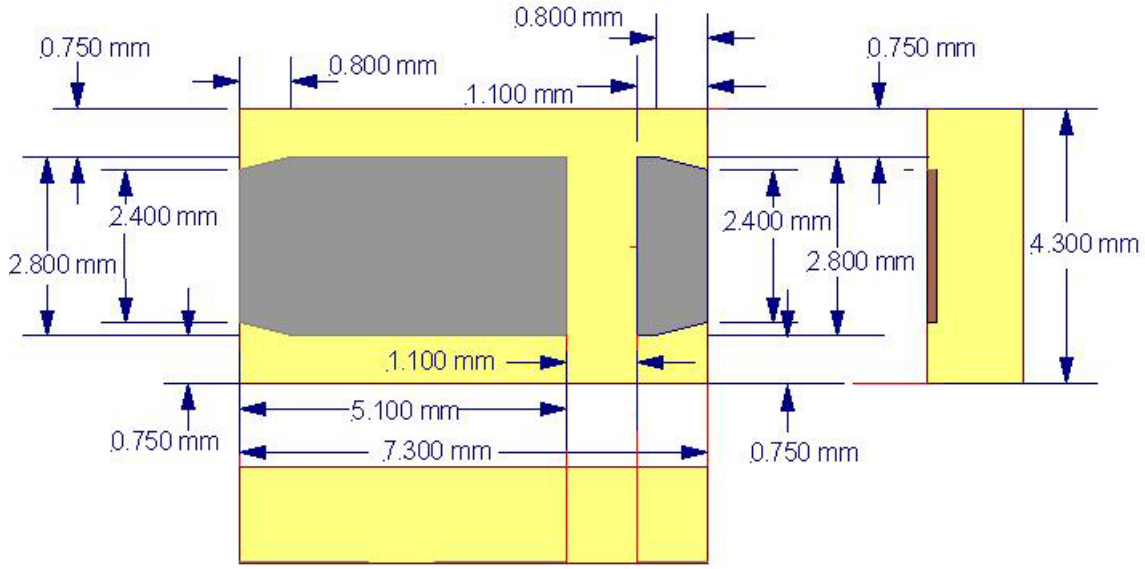

Figure 10. Here is the outline for the 7343FD, low inductance conductive polymer capacitor.

Looking purely at optimizing the ESL, there was a benchmark already in the market – the Sanyo TPL series[3]. This device is a three-terminal, conductive polymer based device with an ESL in the range of

520 pH. The key to this device is the separation space of the anode and cathode contacts at 1.10 mm. The third termination, internally connected to the middle termination, is created for mechanical stability and solder balance.

Our facedown 7343 has only tow terminals for electrical contact to the board, but we will recommend that the users use three solder pads (same as Sanyo TPL) for solder balance. The bottom surfaces of the termination plates are tin plated over nickel plating. The ESL is in the range of 520 pH. The height of the chip will be at 1.5 mm, 1.7 mm, and 1.9 mm maximums.

The recommended solder pads are shown in Figure 11 and there are three pads instead of only two. The reason for this is that if the cathode contact were one, large pad, then the mass of solder created between the solder pad and the termination plate may be large enough to draw together and lift the capacitor, possibly lifting the anode contact away from its pad. By splitting the solder pads into two smaller areas, there will be a smaller mass of solder thus eliminating this.

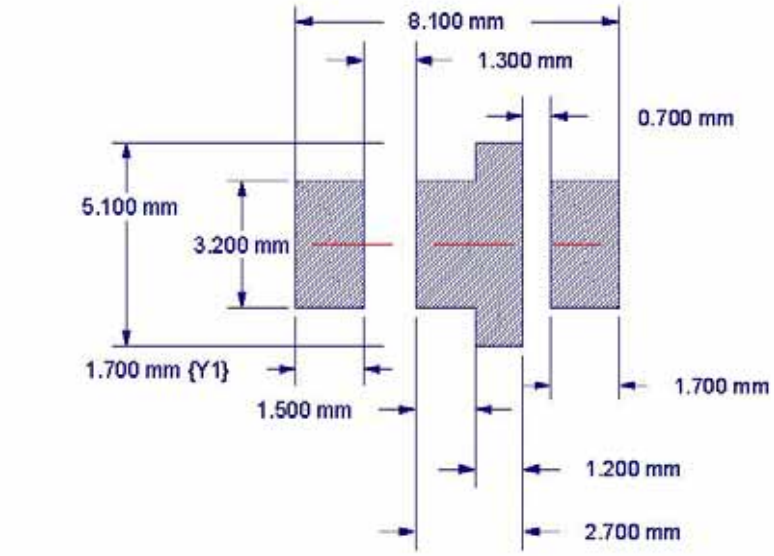

Figure 11. These are the recommended solder pads for the 7343FD, T528 capacitors,

Measuring the parasitics

The movement to eliminate the parasitics in capacitors has followed a sequential pattern. The initial attempts were to reduce ESR, as this was perceived to be the main debilitating factor in circuit response. The measurement of ESL could be obtained in one of two methods. The first is to measure the self-resonance of the capacitor and, based on the formula for the resonance of a series LC circuit, the inductive element could easily be deduced. The second method was to measure the impedance of the device at a frequency well above the self-resonance of the capacitor and, assuming that this impedance was dominated by the ESL element of the capacitor, the magnitude of the reactive element of the impedance was assumed to be the inductive reactance of the ESL at that frequency.

In most instances with MLC capacitors, this can result in different levels of ESL – a high ESL at self-resonance, and a lower ESL at frequencies well above self-resonance. We believe that this difference is attributable to the current being restricted to the lower plates in the frequencies above self-resonance, while the current involves more plates at self-resonance. The effect can be seen as detailed in Figure 12.

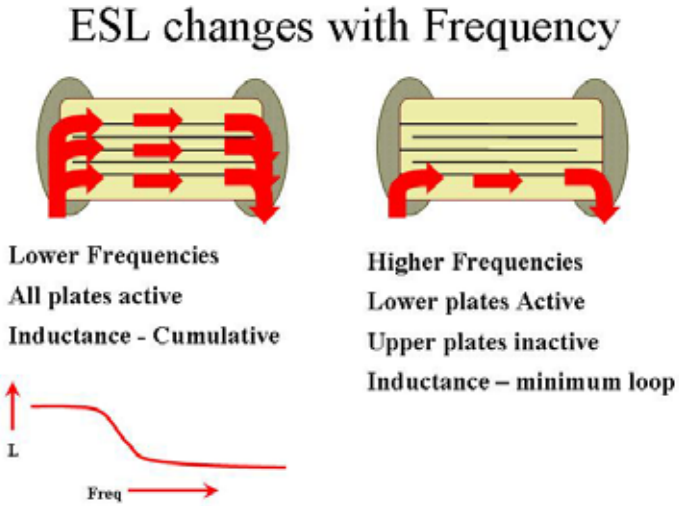

Figure 12. Two distinct ESLs are apparent if measuring at self-resonance and well above this frequency.

The added impedance in getting the currents into the higher plates is due to the added resistance and inductance created by the vertical elements of the terminations as they rise above the board to connect the upper electrodes. Eventually, all capacitors of the same design (e.g., 0603 or 0805) have their currents defined by the smaller loop – and they all appear to have the same ESL.

We do not believe this transition to be a step function, but a gradual effect. We plan on incorporating this effect in the KEMET Spice models, but we are trying to see if we can define the transition in a clearer manner.

Network Analyzer

From previous reports presented at this and other conference, we think that the work in this area has been excellent. We are concerned with one aspect that has been touched on lightly, and that is standardization. The geometries of the mounting fixtures are paramount to universal replication. There needs to be a standards committee taking this up. At one time, the EIA was trying to put a standard together, but we have not heard of any developments.

One more complaint: Following the practices that were beaten on us though our science classes, our results were always to be within the significant figures measured. Today, the readings may be flashed up on a screen as 200.015 pH. Does this system truly have a resolution of 0.001 pH? (That is 1 fH.) Repeat the reading, without moving the piece, immediately after the first reading and the reading now is displayed as 200.356 pH. Is the inductance growing with bacterial contamination? Be careful of what you see. These resolutions may seem comforting, but it is a false comfort. Take the 200 pH as the reading and leave the bouncing numbers off.

Pulse-Current-Injection

We believe that the best way to verify any claim is to use multiple methods to test the claim that result in the same measurement. Another method of testing for ESL, ESR and effective capacitance is by using a current pulse injection system. A pulse can be verified with no capacitor by terminating the pulse generator with its characteristic impedance. We use a pulse generator from HP (HP-2148) for

transitions down to 10 nS, and a model 200 Pulse generator from Pico Pulse Labs with a transition time less than 500 pS. The current pulse transitions from zero current to the output level of the pulse generator and will hold, at that level, for the duration of the pulse.

By injecting the current pulse into the device, the resultant voltage across the device can be analyzed to determine the capacitive, resistive, and inductive elements of the device.

In a perfect resistor (Figure 13 upper left), the resultant voltage pulse would be similar in shape to the current pulse. It should mimic the transition current from zero to the constant current mode, and then hold at a specific voltage during the constant current mode.

For a perfect capacitor (no ESR and no ESL as in Figure 13, upper right), the voltage will show an exponential growth during the current pulse transition time (tr), and then should reveal a constant dv/dt during the constant current phase (I_{Const}). The calculation for the exponentially rising voltage for any time (t_i) during the transitions is as follows:

$$V_{C(i)} = \frac{I_{Const}}{Cap} \times \frac{t_i}{2} \quad (0 \le t_i \le tr) \qquad \text{Equation 1}$$

For a pure inductor (Figure 13, bottom center), the voltage will be increasing (V=L*di/dt) as the current is in transition and should drop to zero once the current reaches its constant mode. What disturbs this effect is that the voltage cannot immediately drop to zero as the combination of inductor, capacitor, and resistor (including source and load resistors) creates a loop that will allow this voltage to ring down to zero.

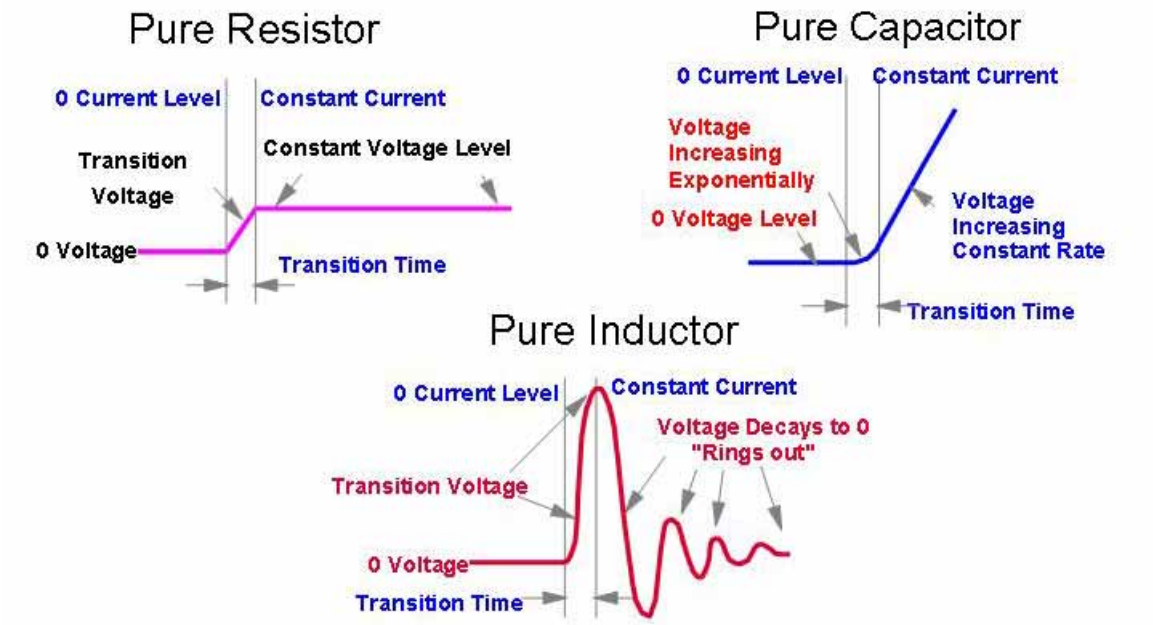

Figure 13. Voltage response for pure elements to the current pulse injection.

The cumulative pulse response to the capacitors is a combination of all of the pure elements as shown in Figure 14. In this analysis, the capacitance is first derived from the constant dv/dt slope, after the ringing effect has died down. At the time values t1 and t2, the voltages v1 and v2 are extracted, and the

capacitance is calculated using these values and the known constant current. Once this capacitance is derived, the voltage at the transition time can be calculated using Equation 1 with t_i set to be equal to the transition time (tr). The difference between this voltage and the extrapolated voltage based on the dv/dt extension from the points (t1,v1) and (t2,v2), will define the resistive offset voltage.

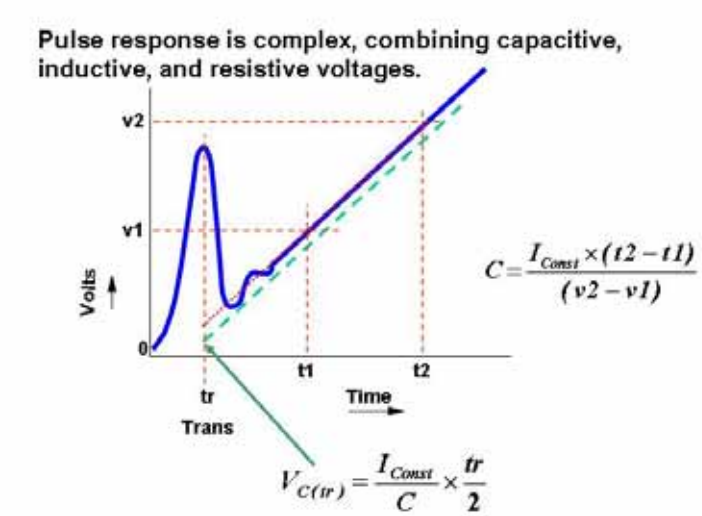

Figure 14. A typical voltage response from a capacitor subjected to current pulse.

The remaining voltage at the transition time is that created by the inductance and the inductance is then calculated as follows:

$$L = V_L \div (di/dt) \qquad \text{Equation 2}$$

For electrolytic capacitors, the capacitance will appear to have an RC-Ladder structure. In frequency scans, the capacitance begin to decay after a specific frequency is exceeded. Lowering the ESR in these components does shift the frequency where this decay begins at a higher frequency range, but it still occurs. With some of the low ESR conductive polymer devices, this decay has been moved to frequencies above the self-resonant frequency. With this current pulse injection method, the constant dv/dt slope appears to be not constant. The slope is steep at the beginning (low capacitance) and the slope decays until it appears constant. Once this slope appears constant, the nameplate voltage is normally derived. Figure 15 is the image captured from a conductive polymer capacitor with very low ESR. The changing dv/dt slope after the ringing has decayed is very minimal – almost imperceptible. The equipment required to make these measurements is definitely not as expensive as network analyzers with high precision and wide frequency range. The storage oscilloscope for capturing these voltage responses may already be sitting on a bench in you facility.

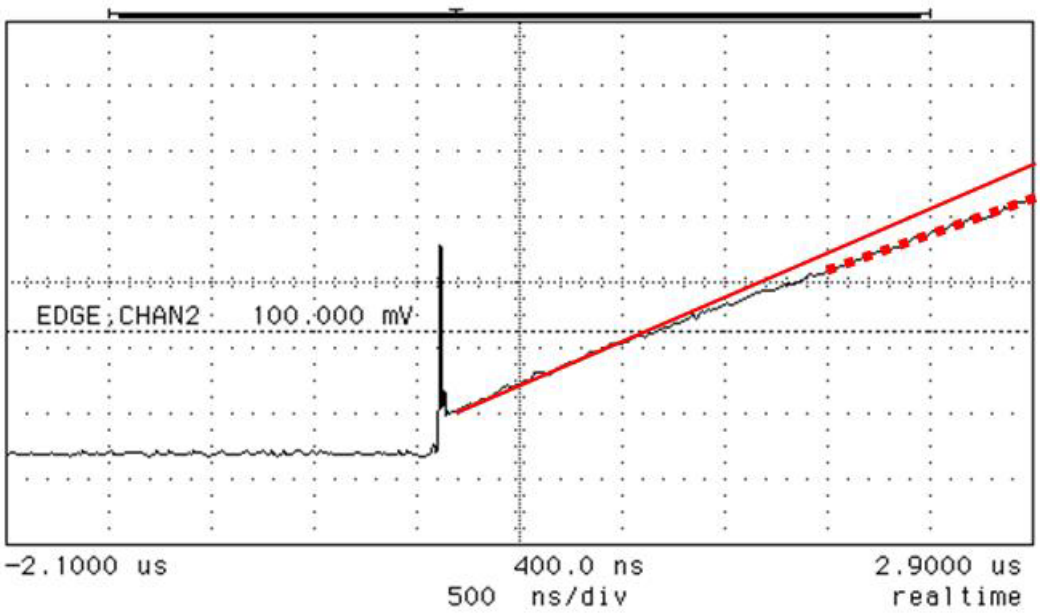

Figure 15. Cumulative voltage response from conductive polymer capacitor to current pulse.

Summation

The goals of reducing the parasitic elements in capacitors are constantly being pursued and constantly moving to ever decreasing levels. Within the capacitor manufacturing community, there is an ongoing clash between engineering fact and marketing one-upmanship. Can the user achieve ESLs that match the claims of the component manufacturer? Because we tend to measure the component by itself, a match with in circuit response is unlikely; but it should not be vastly different. We do not incorporate the lead traces or the vias required to mount these components in a vast variation of circuit designs. Be careful of the claims of two manufacturers making the same device with vastly different claims on performance. The name on the shipping label cannot create these differences in like components. The best analysis of what a component does in a specific circuit is the response of those components in that circuit.

Bibliography

[1] Prymak, John D., "Advanced Decoupling Using Ceramic MLC Capacitors," AVX Technical Information, August 1990

[2] Prymak, John D., "Getting the L out of Capacitors," Intel Power Symposium, September 2001

[3] Sanyo Poscap Capacitors, SANYO Electric Co., Ltd., Oct. 2004, p. 13.

Part III. Bypass Capacitor Inductance, Data Sheet Simplicity to Practical Reality

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Steve is an independent consultant with over 20 years plus industry experience with a broad range of expertise. Steve holds 17 US patents, and has architected a number of TDM and packet based switching products, consults on patents and is a frequent contributor to the SI-list signal integrity reflector.

Abstract
Capacitor ESL is a common, and long reported parameter reported by capacitor manufacturers, and an important consideration to the design of power bypass networks. However, ESL specification and interpretation remains an issue of some controversy that industry grapples with. We compare methods of obtaining ESL values, and the useful application of their results.

A Capacitor By Any Other Name

Bypass capacitors function as shunt impedances in power delivery systems.

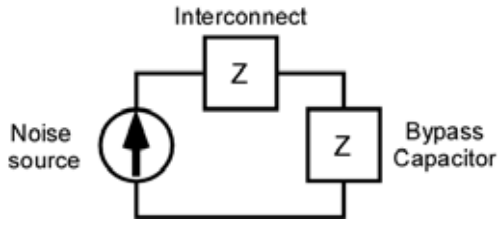

Figure 16, Simplified Bypass Network

Three element and four element models often depict capacitors. While these models successfully represent the basic response of a given device, Novak[1], and Smith[2] both show that the primitive characteristics: ESR, ESL, and C are all frequency dependent.

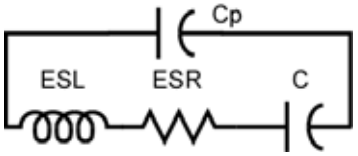

Figure 17, Simplified Model, Bypass Capacitor

Smith [2] proposes a ladder-based model that is shown to reproduce measured behavior at high frequency. Novak [4] proposes a black-box S parameter model. Each approach serves to refine representation of capacitor performance at high frequency where ESL dominates the impedance. Which method we use to obtain high frequency performance is not particularly important so long as it provides an accurate prediction of bypass capacitor shunt impedance in a given application. Above the capacitor series resonant frequency, capacitor shunt performance is completely dominated by inductive effects.

An Inductor Divided Cannot Stand

Our problem with defining capacitor inductance is complicated not only by the fact that inductance varies with frequency, but that inductance expresses the voltage potential required to induce current change through a loop of which the capacitor is only a part. The way that we define the physical loop in our test fixture greatly defines what it is we are measuring. As relative capacitor geometry between one device and another becomes more disparate, it becomes increasingly difficult to define a physical environment that is an exact, or sometimes even a close equivalent between devices in all respects.

Our first problem is to define what we really mean by “device” inductance. Is it:

- The inductance extracted from a coplanar waveguide, or microstrip fixture?
- The difference between the observed inductance of a shorted pad pattern and the device?
- The inductance extracted from a fixed multilayer board geometry?
- Something else?

Until we understand what it is we are comparing, specifications will be of little use in our applications.

Approaching "Device Only" Measurements

We can for example obtain very repeatable and consistent measurements of the incremental inductance between a well-defined calibration structure and a given capacitor. Test fixtures that use transmission line structures such as those developed by InterContintental Microwave set the standard for this measurement approach. The fixtures consist of a fixed and a moveable block. DUT, and calibration test cards insert between the blocks. Each block contains coaxial waveguides with SMA launches. In the fixture, a DUT shorts a section of 50 ohm microstrip.

These fixtures use small test cards, (< 1" long) with reference planes either 10 mils or 20 mils from the DUT surface tightly stitched to flood on the surface. Lead-in, and lead-out waveguides to the SMA launches are carefully built to 50ohms. Fixture loss is low. Precisely manufactured calibration, and DUT test cards assure very repeatable results. These fixtures may be configured for two or four port operation. Figure 18, and
Figure 19 shown here courtesy X2Y, LLC and InterContinental Microwave depict a four-port fixture and calibration fixtures to support TRL calibration.

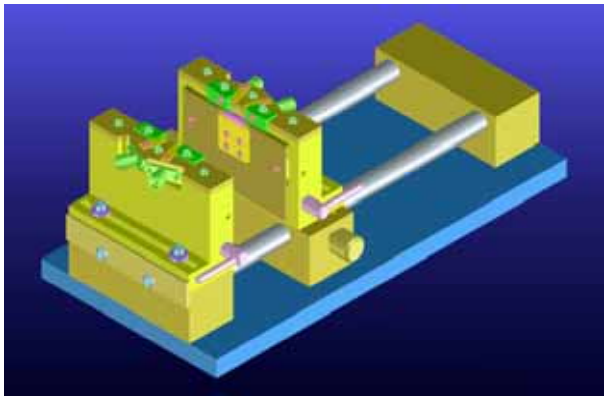

Figure 18, ICM Capacitor Test Fixture

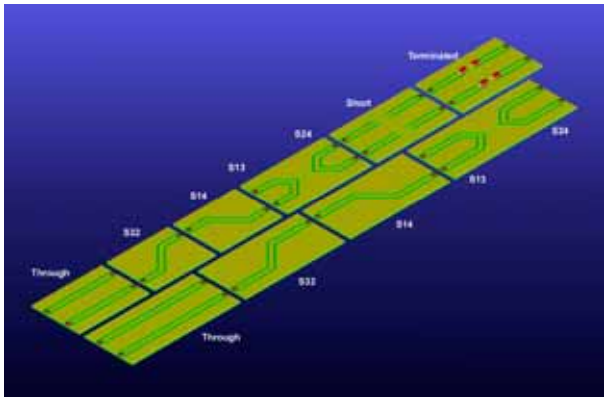

Figure 19, ICM Calibration Cards

Exemplary results 0805 size capacitors demonstrate the excellent quality results available from these fixtures.

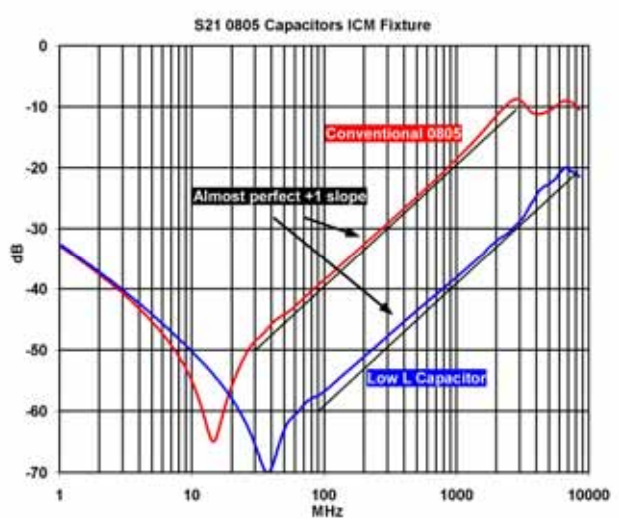

Figure 20, Example 0805 S21 Insertion Loss, ICM Fixture

Note that the measurement demonstrates very low ripple, and an almost perfect +1 slope from 50MHz to 2GHz. When comparing devices of like size and terminal configuration, these fixtures provide superlative repeatability over four or more decades of bandwidth. But what do these results really tell us? They tell us how effectively capacitors divert energy from microstrip transmission lines.

The practical limitations of such fixtures versus bypass evaluation lie in two areas:

- The length of the DUT oriented in parallel to the transmission line affects loss, and
- The fixture does not account for via attachments to planes, typical of most bypass applications.

The first issue means that in general, longer parts insert more loss than shorter parts of otherwise identical geometry. In a bypass application this difference may be muted if present at all. This effect can be somewhat deembedded through deployment of different length DUT test cards.

The second issue is very significant to most bypass applications. To predict the performance of a capacitor, particularly low-inductance capacitors attached to planes, we need fixtures that incorporate mounted loops representative of the application.

Plane Cavities, and the Mounted Capacitor

Common bypass application mounts a bypass capacitor on one side of a circuit board, joined to planes. At frequencies above a few MHz, skin effect converts the upper most plane into a very effective RF shield [3]. In half ounce copper, the cut-off occurs near 16MHz. This shield isolates the plane cavity from the bypass capacitors and their associated interconnect above the uppermost plane. Noise current circulates in a loop formed by the upper surface of the uppermost plane, the Z axis interconnect, and the lower plate structure of the capacitor. The area of this loop determines the mounted inductance of the capacitor as seen at the plane attachment. See Figure 21. Note particularly, that high frequency current can only escape and return through openings in the upper plane.

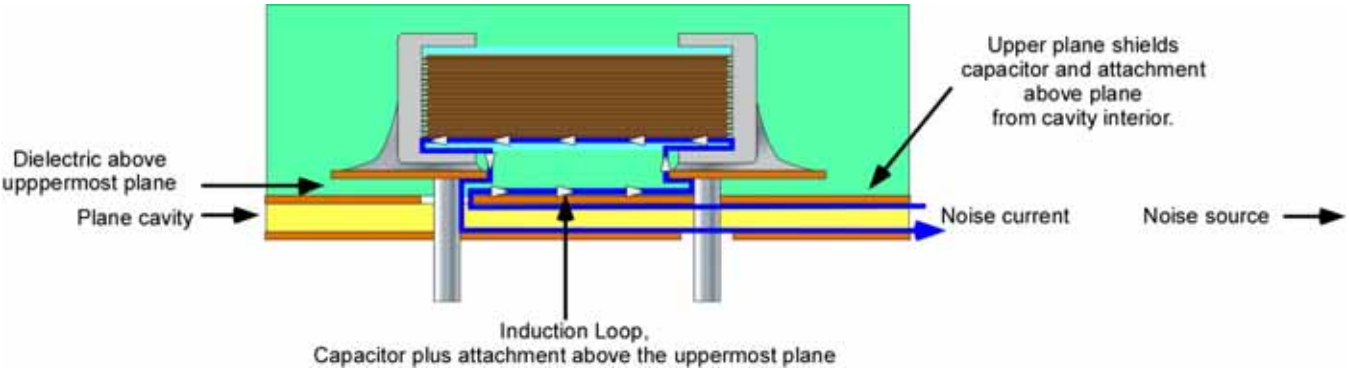

Figure 21, Mounted Bypass Capacitor Induction Loop

This induction loop above the plane cavity is a function of no fewer than nine independent variables a number of which are completely beyond the control or even knowledge of the component maker:

- Capacitor size,
- Capacitor terminal configuration,
- Capacitor bottom cover layer thickness,
- Via extension height above the uppermost plane,
- Via count,
- Via diameter,
- Via separation,
- X-Y plane offset of vias from device pad,
- Etch configuration of the surface layer.

To accurately manipulate all or even several variables arbitrarily requires a full 3D field simulation. However, the cost and complexity of these simulators such as: Ansoft HFSS, and CST Microwave Studio make such an undertaking too complex and costly for day-to-day work. It is also unlikely that the capacitor industry will soon be undertaking evaluation of thousands of configurations of capacitors that may or may not make their way into customer systems. So, for the time being, the user community will need to deploy evaluation vehicles of their own.

Analog Models

We can still evaluate the performance of at least single capacitor(s) by carefully constructing test fixtures that are physical analogs of real substrates. The Intel Universal Capacitor Test Vehicle, is one example of such an analog used to evaluate one capacitor at a time. When designing such an analog, it is critical to understand the variable limits the model can faithfully represent. With a well-designed physical analog we can over a limited range both:

- Compare the relative performance of two or more device(s), and/or
- Predict in-system performance

To achieve either goal, it is important to design the test fixture such that it adds minimum coloration versus how capacitors will actually be mounted. While it may be tempting to attempt to somehow normalize disparate capacitor configurations, fully six of the available physical variables are at least partially independent of the capacitor. Therefore, we believe to obtain the most practical benefit, that any test vehicle should employ the best mounting and attachment configuration for any given capacitor style that is compatible with manufacturing rules. The fixture should:

- Optimize device placement and orientation to noise source(s) (usually ICs), for each DUT
- Optimize surface etch features, for each DUT
- Optimize via: drill, pad, and antipads for each DUT
- Exactly reproduce PCB stack-up above the uppermost plane in the cavity(s) bypassed by the DUT.
- Provide reliable deembedding of interconnect through the plane cavity up to the device attachment vias.
- Ensure sufficient plane coverage beyond both DUTs and launches to prevent both field fringe issues and unexpected current paths.

For example, conventional geometry 0201, 0402, 0603 etc capacitors with two terminals are typically attached with a single via per pad. If the application is bypass of a single IC, then measurement with the vias located on the near side of the source and receiver makes sense. If they will be used to bypass a board in general, then measurement configurations with the vias on both the near and far sides are called for. Similarly, multi-terminal capacitors, such as array capacitors, IDC™, or X2Y performance are all sensitive to location of the noise source and voltage monitor point. Impedance to noise injected and monitored both on one side of the device will be significantly higher than the noise injected on one side and monitored on the other.

Once the device mounting pads, via configuration and surface etch have been configured, the second step is to design the vehicle to be as immune to the test connector attachments and plane parasitics as possible. Teraspeed in collaboration with Dr. Howard Johnson, of Signal Consulting, Inc, has developed such a vehicle for X2Y, LLC using multiple test cards. Each card consists of surface mount SMA connectors on the underside of a three-layer PCB structure as depicted in Figure 22:

The bottom two layers form a 12mil height plane cavity. The DUT mounts on the top copper layer above a dielectric layer, the thickness of which is selected to match surface layer to uppermost plane in the real-world PCB being modeled. The overall board size is kept small raise the modal resonance as high as possible, as well as minimize parasitic capacitance and thus board to DUT PRF. The 12mil plane height is a compromise between extractable resolution for low-inductance capacitors and a high board to DUT PRF for conventional capacitors. SMAs located on the fixture back-side utilize the planes as shields to minimize potential interaction between instrument cabling and the DUT. Within narrow limits, this style fixture can also evaluate small device arrays.

For each DUT configuration, a duplicate calibration fixture with DUT vias internally shorted to both planes provides a through calibration reference for the plane cavity only. This reference lets us deembed the combined capacitor and mount above the uppermost plane from the spreading inductance of the cavity using the via configuration specific to the DUT. Result extraction may be performed as detailed by Novak[1] to a theoretical accuracy of a few percent almost to the PRF. Once we have characterized a DUT with this style fixture, we can reliably predict single capacitor performance for a wide range of plane cavity configurations, not just the 12 mil cavity of the fixture.

SPICE simulation performance of the fixture is well behaved as seen in Figure 8. (Measured results were not available at the time of publication, but may be found on the Teraspeed web site: www.teraspeed.com.) The simulation is based on a nine-element bedspring representation, on a 50mil cell pitch that includes skin effect, but does not include dielectric absorption. Low inductance capacitor measurements have several dB separation from the reference short, and all measurements exhibit wide quasi-linear responses that afford repeatable extractions for different styles of capacitors.

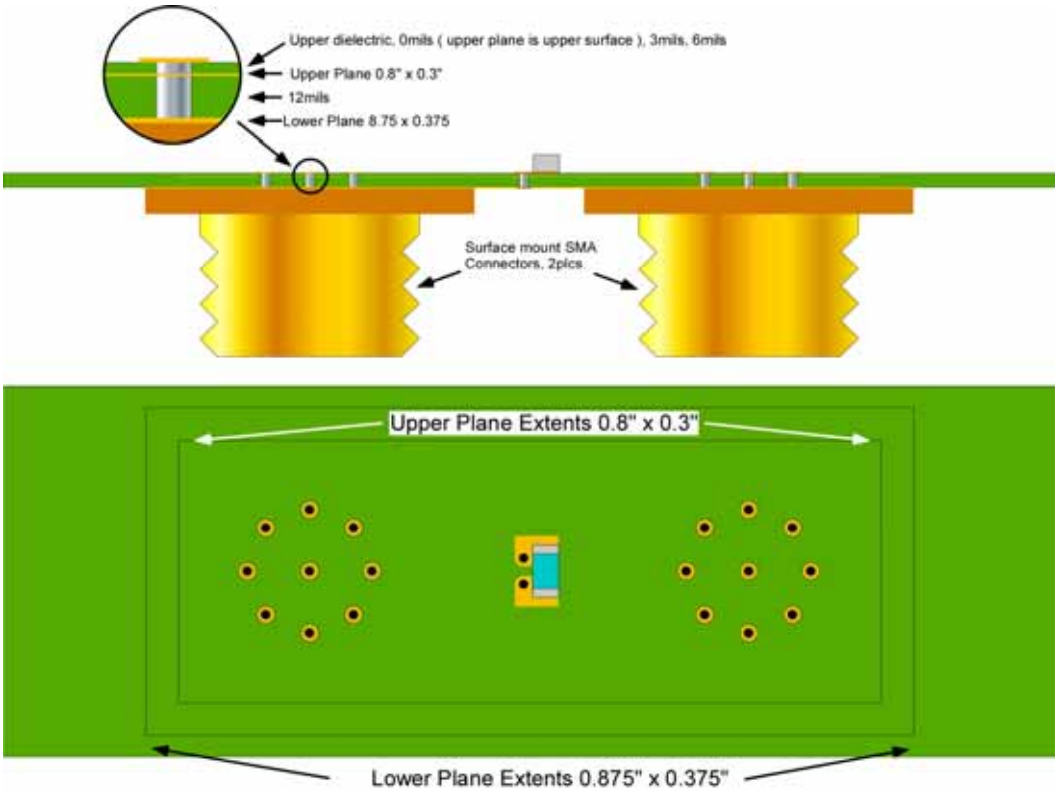

Figure 22, Backside SMA Launch Evaluation Vehicle

The primary limitations to this fixture approach are:

- A separate fab is required for each thickness of top dielectric.
- The assembly evaluates impedance looking across the DUT.
- The assembly is somewhat delicate.
- The spatial extent of the planes limits low inductance resolution.

As it stands, this fixture can only evaluate a single component height above the uppermost reference plane. Consequently, a new fab must be made to evaluate each upper dielectric configuration of interest.

As with the ICM fixture, insertion loss evaluates across the DUT as compared to Novak[1] where the transmit and receive launches are through the test fixture PCB. The key advantage of Novak is that it is a direct analog of how most ICs orient to their respective bypass capacitors.

The two potential disadvantages of Novak are:

- Discontinuity of the 50 ohm transmission line.
- Potential top-side probe interaction with the DUT / site.

Novak has been careful to address both issues and demonstrate good accuracy. Users attempting reproduce Novak must be very careful in the construction and calibration of probes, most particularly, the top-side probe.

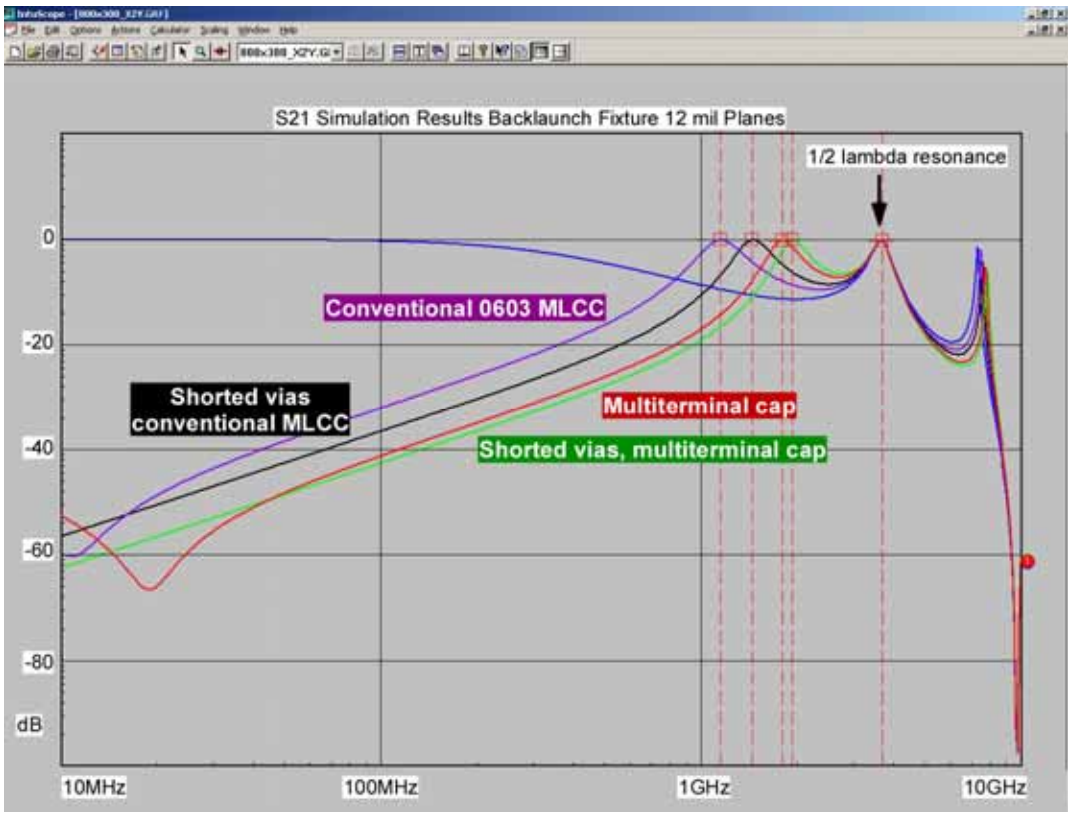

Figure 23, Backside Launch Evaluation Vehicle Simulation Results

Conclusions

Capacitor inductance is not a device only dependent parameter. In common bypass applications, interconnect from capacitor to the nearest shield plane is integral to actual in-system performance.

Vendor capacitor inductance standards such as those moving through JEITA that emphasize a "device only" ESL, and afford value for comparative ranking of similarly packaged capacitors. These specifications are however only a starting point towards prediction of actual in-system performance.

Evaluation of disparate capacitor geometries requires either full-wave 3D models, or carefully designed and evaluated physical analog models. Carefully designed analog models that reflect actual device attachments, and provide reliable fixture deembedding will reward the user with a precise assessment of device performance that cannot be found in any data sheet.

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Part IV. Decoupling Capacitor Specification in Xilinx FPGAs

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Abstract

This paper focuses on the constraints and objectives Xilinx faces with respect to decoupling capacitor selection. A discussion of Power Distribution System (PDS) impedance requirements comes first, as this defines the electrical objectives. This is followed by discussion of the PCB and device package environments and the limitations they impose on decoupling capacitor selection. Practical implementation of decoupling in each environment follows. Common electrical specification and control over capacitor Equivalent Series Resistance (ESR) are identified as two possible areas for improvement.

Introduction

Selection of decoupling capacitors for high performance FPGAs is a unique task. Unlike most other silicon vendors, the FPGA vendor specifies not only the capacitor part numbers for use within the device package (where present), but must also specify the PCB-level decoupling networks for use in a highly varied user space. Explanation of the various challenges and some of the solutions are presented here.

Decoupling for FPGAs

In general, the task of specifying a decoupling network for an FPGA has similar goals for both package and PCB. The ways of achieving these ends differ, due to the differing constraints of the two scenarios.

From the point of view of the FPGA die, the power system impedance must be relatively low over a broad range of frequencies, and must be well-behaved with regard to resonance (free of high-impedance spikes). Achieving low impedance is the first goal.

How Low is Low?

The question of target impedance for PDS is a complex one in most cases, and this is certainly true of FPGAs. When it comes to relatively simple structures like single-ended output drivers, transient current estimates can be obtained from simulation and measurement, as can IO power system noise sensitivity. This makes for straightforward calculation of PDS target impedance.

However, core resources such as the FPGA fabric, clock trees and other elements pose a different challenge. While it is possible to determine core power system noise sensitivity, it is very difficult to estimate the transient current characteristics of a large FPGA.

Since it is also difficult to determine the precise characteristics of the distributed core power system, determination of core current transients based on measured noise voltage under device operation has limited accuracy. For these reasons, core PDS target impedance is not as stringent a design specification as PDS design rules based on prior measured device performance. Functionality testing beyond corner conditions and measurement of system parameters such as clock duty-cycle distortion and jitter are the indicators used here.

Capacitor Specification for Package Design

Most Xilinx FPGAs in the high-performance device families use discrete capacitors inside the device package, mounted to the package substrate. See Figure 1.

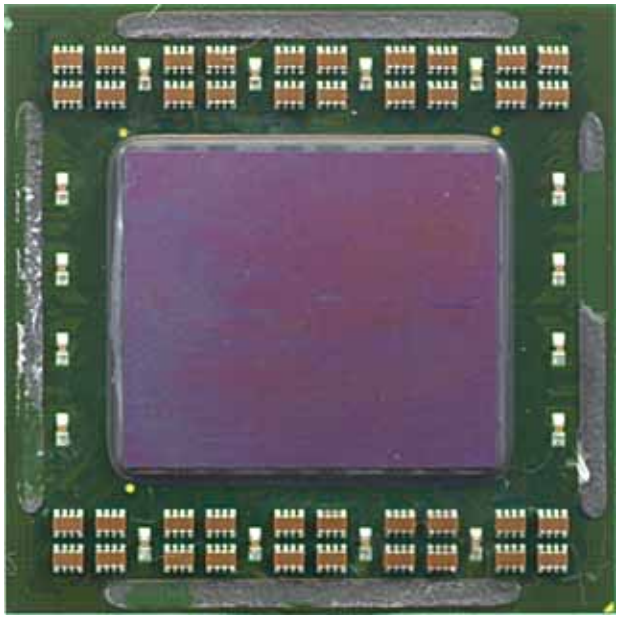

Figure 1: Photograph of a Xilinx FPGA with lid removed, revealing decoupling capacitors mounted to device substrate.

Determination of capacitor style, value, quantity and mounting is a complex process. While it would be nice to design the substrate decoupling capacitor network such that it was tailor-fit to the precise needs of the FPGA silicon, this is not possible. The basic space constraints of conventional device packaging prevent the inclusion of a complete decoupling network capable of maintaining PDS impedance at adequate levels across relevant frequencies. This may change in the future, but today this is the case.

Given the understanding that the target impedance cannot be reached with just the package capacitors, the task is to design a substrate decoupling capacitor network that is as good as possible while maintaining relative PDS consistency across the device family.

"Good" in this case is as follows for the various decoupling capacitor characteristics:

C	Capacitance Value	As high as possible
L	Parasitic Inductance Value	As low as possible
R	Equivalent Series Resistance	Moderate, controllable
A	Footprint Area	As small as possible
H	Case Height	Not taller than silicon die
T	Thermal Operational Range	Same or better than FPGA
V	Voltage Operational Range	Greater than twice the max rail voltage
$	Cost	As low as possible

Obviously many of these are in conflict, which necessitates compromise. Fortunately, some factors are more important than others, narrowing the options.

Height (**H**), for example, has a hard limit. The cost of integrating a capacitor whose mounted height is taller than the silicon die mounted height is very high relative to the other factors. This requires changes to the package construction such as lid milling, and ultimately leads to a taller device package. Thermal and Voltage operational ranges (***T, V***) also have a hard limit. The capacitors within the package must

work reliably and within spec over the temperature and voltage ranges of the packaged FPGA. These 'make or break' limits narrow the pool of part choices.

In high-performance FPGAs, capacitor cost (***$***) is one of the less important characteristics. The incremental cost for a capacitor with better electrical characteristics tends to be small when compared to the finished device.

That leaves capacitance (***C***), inductance (***L***), resistance (***R***) and area (***A***). ***C*** is essentially defined by the manufacturer. The largest available value is used. ***L*** defines the capacitor style and body size. Since multiple capacitors in parallel can increase ***C*** and reduce ***L***, ***A*** has a symbiotic relationship with these two.

R is a very useful parameter to have control over. Unfortunately, the current state of the industry doesn't offer a lot of resistance options within the high-performance ceramic capacitors with low ***L*** and high ***C***. Currently ***L*** and ***C*** trump the need for a particular ***R***. However it is conceivable that increases in ***C*** values with a blind reduction of ***R*** could lead to higher-Q devices that would no longer be appropriate for use as decoupling capacitors. A packaged device with a high-Q resonance is more difficult to design into a PCB decoupling network, as there is greater possibility of creating a high-impedance anti-resonance peak [1] [2].

A is an important parameter best minimized, as the package substrate decoupling capacitors need to fit in a small, fixed area. ***A*** tends to dictate ***L*** for traditional two-terminal MLC capacitors. This is less true of Inter-Digitated Capacitors (IDC) and array capacitors, where ***L*** typically scales with the number of terminals.

The comparative selection of the package substrate decoupling capacitors is done based on capacitor electrical characteristics. In the absence of consistent vendor-supplied specifications, Xilinx has relied on in-house measurements and helpful information from the industry.

IDC capacitors are currently used with great success in Xilinx FPGAs. The small case size currently available allows them to be used with great versatility while offering the reduced inductance benefits of a multi-terminal capacitor.

Space Constraints

The space available inside the FPGA package is limited, fixed for a given silicon die and package combination. Within a given FPGA family there are numerous silicon die sizes, and many package size options. Not all combinations are available, but for each device package there are a number of silicon die sizes that must fit inside. The mechanical constraints of package construction (lid attach glue area, die underfill keepout area) dictate the amount of area left free on the package substrate for discrete decoupling capacitors. In a given package, a larger silicon die leaves less area for discrete decoupling capacitors. This is illustrated in Figure 2.

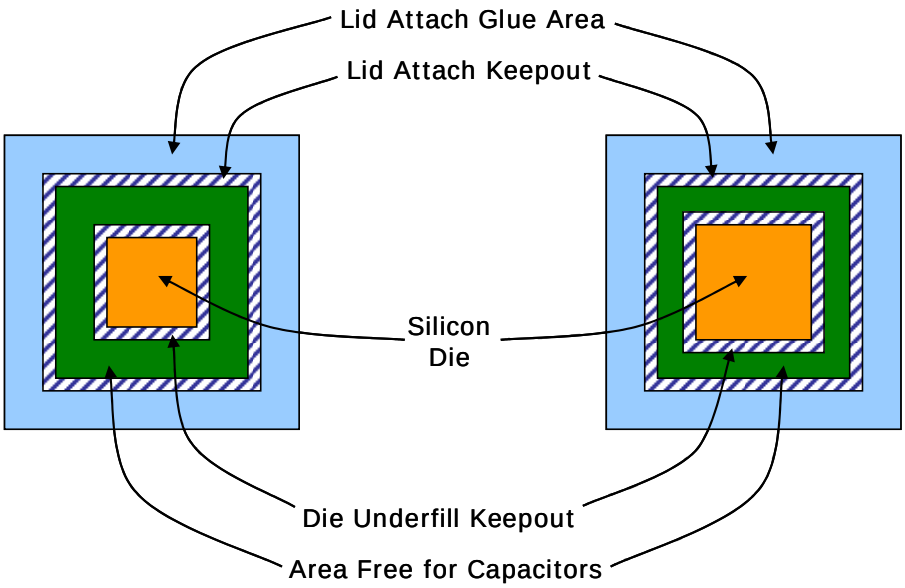

Figure 2: Comparison of two hypothetical die sizes in one package size. Smaller die on left with more area free for capacitors, larger die right with less area free for capacitors.

This is an unfortunate fact when it comes to capacitor quantity selection. Ideally, substrate decoupling capacitor design rules keep capacitor quantity proportional to the resources they are serving (e.g., 1 capacitor per X CLBs, 2 capacitors per full-size IO bank). In most devices, die area is higher for more core resources, and package area is higher for more IO resources. This means that in a given device package, a device with more core resources may have less area available for substrate decoupling capacitors.

Capacitor Specification for PCB Design

Since the properties of the PCB Power Distribution System (PDS) determine whether a device is functional or not, specification of appropriate decoupling rules is essential for silicon vendors.

While some silicon vendors can depend on a well-constrained design space for these systems to help define the rules, others, including FPGA vendors, cannot. Part of the FPGA value proposition is that it is "anything to anybody." The PCB used by "anybody" might be 26 layers in a supercomputer farm or 6 layers in a plasma display panel controller. Not only do the electrical aspects of the PCB change across this range, the passive component styles and manufacturing techniques vary as well. PDS design rules for this space must accommodate these varied possibilities.

There are many ways to attack such a challenge. Most differ in how much design responsibility is put on the user versus the vendor. Xilinx has found that a prescriptive method works well for most users. Such a method defines minimum design conditions that must be met, offering a fixed set of options considered to be within acceptable limits.

Within such a rule structure there are many ways to define these limits, with differing levels of design freedom and constraint. Rather than specify a target PDS impedance appropriate for each of the elements of the FPGA and leave passive device selection to the user, the prescriptive method specifies a network of decoupling capacitors (values and quantities) along with guidelines on PCB geometries for a

particular supply rail of a given member of an FPGA family [3]. While the prescriptive method more tightly constrains the options available to the system designer, it is much less work to implement and doesn't require expertise in filter design. This method is used for mainstream design with some amount of necessary guardbanding.

While conservative guardbanding can be good for system robustness, it comes at the price of leaving performance on the table or raising system cost. Guardbanding should not be excessive.

One way to reduce the need for guardbanding is to increase the accuracy of the prescriptive method definition. While there are many critical metrics involved, one of significance is the electrical characteristics of the decoupling capacitors. With consistent, standard characteristics, significant fat could be trimmed from the prescriptive design rules specified by FPGA and other silicon device vendors.

Another possibility lies in the ESR of these capacitors. If designers and vendors could depend on tighter control of capacitor ESR, it would be possible to exercise more control over the network impedance, leading to a more optimized network with less chance of an unpredicted anti-resonance.

Conclusion

In any complex optimization problem there is always room for improvement. This is true of decoupling capacitor usage with FPGAs, as with other modern silicon devices. Improvement in two particular areas would reap significant benefits: standards for consistent electrical characteristics and control over capacitor ESR. This allows for tighter, lower cost fitting of decoupling capacitors to FPGAs while reducing the risk of aberrant PDS behavior.

Acknowledgements

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Part V. On the Uniqueness of the Inductance of Bypass Capacitors

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Abstract

Bypass capacitors beyond their series resonance frequencies become inductive. The lower the inductance, the more efficient is the bypass capacitor at high frequencies. The inductance, however, comes in loops, and the bypass capacitor is only part of the loop. Capacitor manufacturers, not knowing the geometry that will be put around the capacitor, don't have an easy way of characterizing their capacitors in terms of inductance. The paper gives an overview of the major possibilities of characterizing the inductance of bypass capacitors. It is shown by measured data that inductance of a given capacitor piece does depend on the fixture and method of measurement, which makes it harder to compare data from different vendors.

Problem definition

A simple equivalent circuit for bypass capacitors has three major elements that users need to consider (Figure 1): Capacitance (C), Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). C and ESR are primarily determined by the capacitor itself, but since inductance is a loop property, ESL strongly depends on the geometry of application (Figure 2). The illustration shows a multi-layer ceramic capacitor (MLCC) mounted to a plane pair in the printed-circuit board (PCB), where the inductance parameter may be of the highest importance to the user. The vertical cross-section sketch shows the MLCC part soldered to pads and connected to planes with through holes.

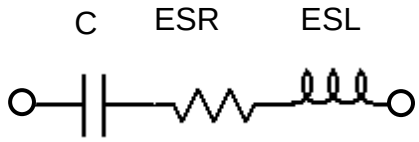

Figure 1. Simple RLC equivalent circuit of a capacitor.

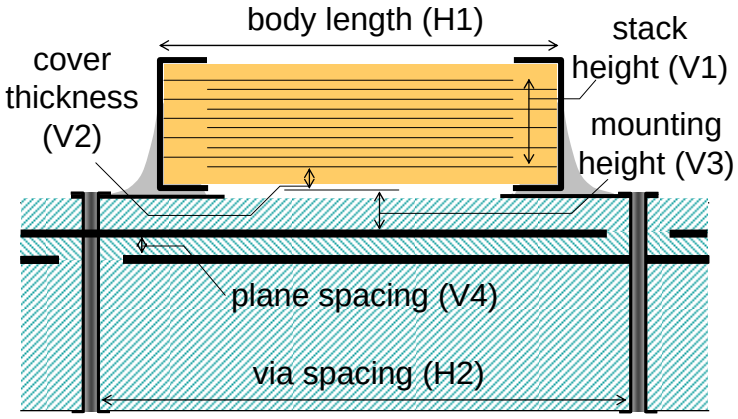

Figure 2. Vertical cross section of an MLCC mounted to PCB planes.

On Figure 2 we identify two horizontal and four vertical parameters, which primarily determine the loop inductance of the mounted capacitor in this configuration. At the Series Resonance Frequency, the loop inductance is determined by all four vertical geometry parameters: V1, V2, V3 and V4. At high frequencies, asymptotically the significance of the capacitor stack height and PCB plane separation diminishes, and the inductance is determined by only V2 and V3. From the horizontal dimensions, H1 and H2 are part of the loop at all frequencies, though asymptotically, at high frequencies, the H1 body length contributes less, since it adds to the loop size only through a height of V2.

The low and high-frequency current-loop approximations are illustrated in Figure 3. The low-frequency loop shows the center-of-gravity lines for the horizontal current flow inside the capacitor plates and between the PCB planes. Note that on the sketch H1 < H2 is shown, but with aggressive low-inductance mounting, H2 < H1 is also possible. Not shown in the cross-section sketches is the width (depth on the sketches) of the current loop; deeper (wider) current loop results in lower inductance.

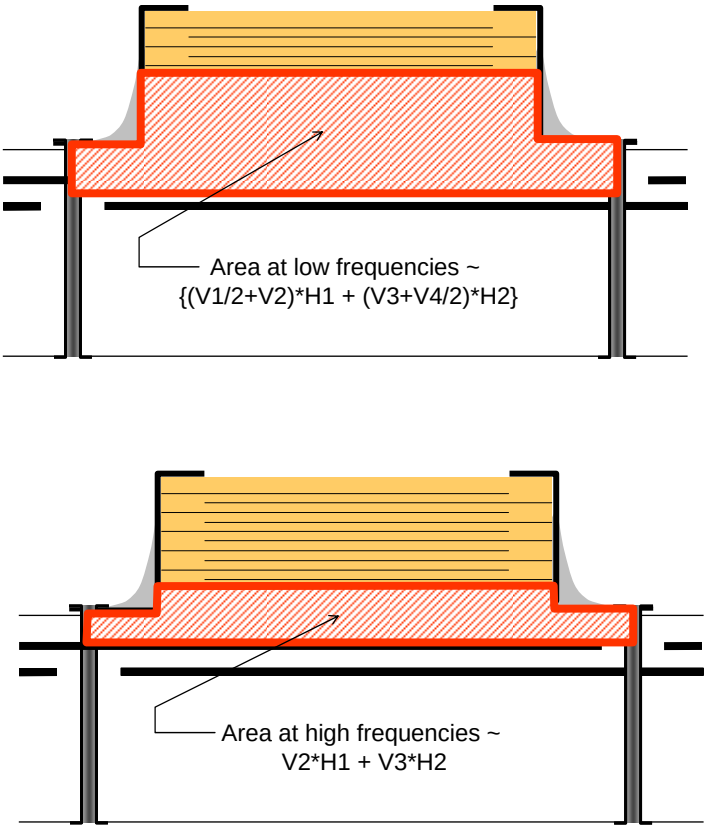

Figure 3. Illustration of approximate current-loop shapes and cross-section areas. Top sketch: low-frequency model. Bottom sketch: high-frequency model.

Note that when the capacitor is not connected directly to planes, but rather it may be connected to pins of an integrated circuit, the geometry parameters influencing the loop inductance may be significantly different. This, however, does not negate the conclusion that the inductance is determined by both the capacitor's internal geometry (set by the capacitor manufacturer) and the external geometry set by the user.

Besides of ESL is being application dependent, for various reasons, all three parameters in the equivalent circuit of Figure 1 are usually frequency dependent. Figure 4 shows an illustration of frequency dependency: a 10uF 0508 capacitor measured in a small test fixture.

In real PDN applications, the geometry could become even more complex and convolved, but the same dilemma remains: how to characterize and measure the inductance of the bypass capacitor so that the number is meaningful and useful for designers and at the same time it is repeatable and unique.

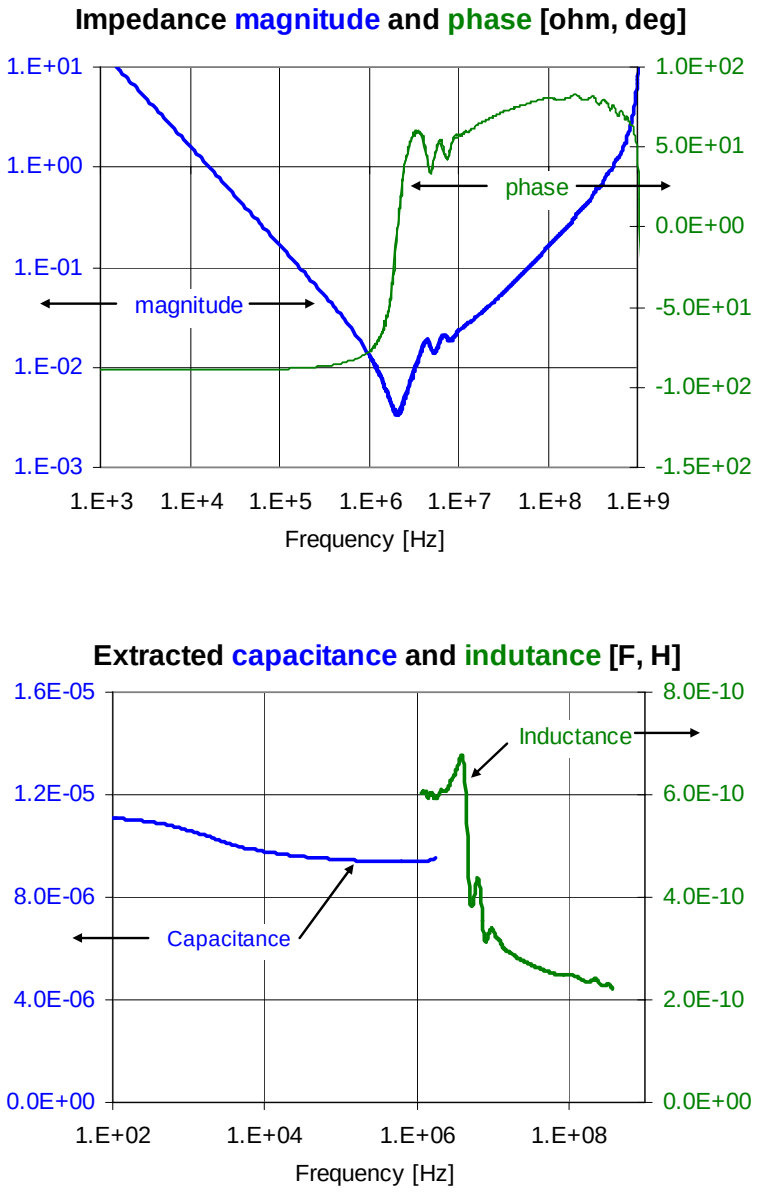

Figure 4. Characteristics of a 10uF 0508 reverse-geometry MLCC part measured on a small-size PCB fixture. Top graph: impedance magnitude and phase. Bottom graph: extracted capacitance and loop inductance.

From [1] the conclusion was that there is no known way to measure and extract ESL uniquely, only repeatable solution is to give/specify the capacitor stack and cover height and do numerical simulations. The figure here shows an MLCC part, but the basic concept and dilemma is the same for all bypass capacitors, including metal-can electrolytic and polymer as well as brick-housed tantalum and similar capacitors. At low and high frequencies, the current loop contains both capacitor-determined and user-determined geometry contributors.

Options to characterize inductance of bypass capacitors

Partial self inductance of capacitor

From the current-loop cross section, we can easily get the *Partial Self-inductance* of the capacitor if the loop size is big enough that the mutual inductances become negligible.
Pros: the partial self inductance is a unique property of the capacitor's geometry, and as such, it could be a figure of merit to compare capacitors' performances.
Cons: it does not depend on and therefore does not capture the cover thickness, which is a major influencing factor of the ultimate high-frequency inductance in low-inductance mounting.

Mounted Inductance

The *Mounted Inductance*, as defined for instance in [2], is the loop inductance of a capacitor in a particular mounted situation.
Pros: loop inductance is easy to measure.
Cons: the measured values depend on the vertical *and* horizontal application geometry as well as the PCB planes.

Attached Inductance

As was shown in [3], *Attached Inductance* can be obtained by curve fitting data to find the equivalent inductance presented by the vertical capacitor geometry to the planes, which yields the same loop inductance when the PCB model is attached. This way we break the current loop at the planes, and the resulting inductance figure becomes independent of the plane geometry: plane separation, plane thickness and location on the planes horizontally.
Pros: This was shown to be independent of the plane separation and of the horizontal location on the plane.
Cons: All of the other application-geometry dependency still remains.

Added Inductance

As described in [4], *Added Inductance* could be the closest of what dedicated instruments and fixtures measure. We first characterize the fixture, open and shorted. The inductance of the shorted fixture is usually considered as the zero reference for later measurements. Next the capacitor is mounted on the fixture and we measure the combination of fixture and capacitor. The calibration removes the impedance of the shorted and open fixture.
Pros: eliminates a big portion of the external loop inductance.
Cons: as shown below, due to mutual inductances between the capacitor body and fixture, this inductance reading is still not unique.

As it was shown in [5], vertical resonances may build up in tall MLCC parts, which show sudden inductance and resistance changes above SRF. This, however, is more of a function of the capacitor construction itself.

Measured data in [6] suggested that when using calibrated fixtures to extract capacitor parameters, we may include a fixture-dependent constant offset value to get agreement with other measurement methods. If the offset was dependent only on the fixture, and not on the capacitor to be measured, this would give a good opportunity to obtain unique inductance values of the capacitors. Unfortunately, as shown by the following figures, in general this is not doable.

To see how the measured inductance obtained from a calibrated fixture may depend on the fixture construction, measurements were done on several different fixtures and capacitor constructions. In one measurement series, D-footprint low-profile polymer capacitors [7] were measured on three different test fixtures. One of the fixtures had blind-via connections (labeled as C4051 in Figure 5) to the nearest planes in the fixture stack up. The other two fixtures had through-via connections with the same horizontal geometry, but going to planes in different depth in the stack up. The fixture labeled C4057 had through-hole connections to the same near planes as in fixture C4051. Fixture C4058 had the same escape pattern as C4057, except the through-via connections go to planes far from the surface.

Ten capacitors were selected for the study. The parts were numbered for easy identification, and all ten parts were measured on all three fixtures. The parts were attached to the fixtures without soldering: silver-filled uncured epoxi paste was put on the terminals, and the parts were pressed onto the pads with a clip, which provided repeatable contact force during the measurements.

The measured loop inductances were extracted as a function of frequency. Figure 5 shows the extracted inductance at 100MHz for each sample, separately in the three fixtures.

A second set of tests were conducted with ten pieces of 0306-size reverse-geometry 1uF MLCC parts. Two fixtures were used: one with blind-via connection, another with through-hole connection to the same planes in the stackup. The ten samples were individually identified and their ‘top’ and ‘bottom’ sides marked. To make sure that the measured data does not contain uncertainty due to solder-fillet height, and ‘top’ versus ‘bottom’ differences, all samples were hand soldered to the fixtures in the same orientation (‘bottom’ facing the fixture) by pressing the parts in the melted solder all the way to the fixture pads.

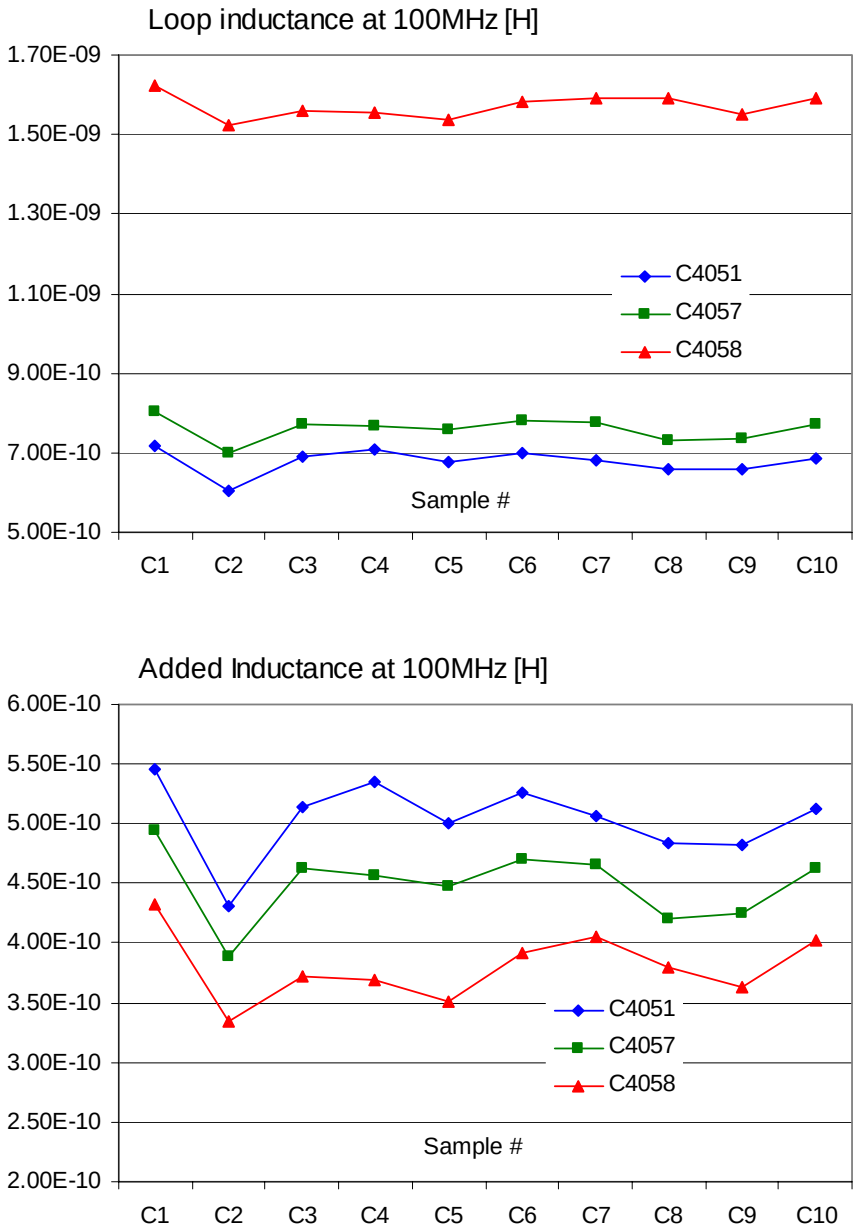

Figure 5. Extracted inductance values for ten face-down D-footprint low-profile capacitors in three different fixtures. Top graph: loop inductance. Bottom graph: Added Inductance.

Data in Figure 5 shows that the blind-via connection results in the lowest loop inductance, the through-via connection to the near planes is next, while the highest loop inductance results from the through-via connections to the far planes. Interestingly, the Added Inductance, which is the difference of loop inductance and the inductance of the shorted fixture, shows the opposite trend: the highest Added Inductance is associated with fixture 1, which has the lowest loop inductance. The difference in Added Inductance among the three fixtures is approximately 200pH. Note that the traces on the two graphs run in parallel, indicating good resolution and repeatability of data.

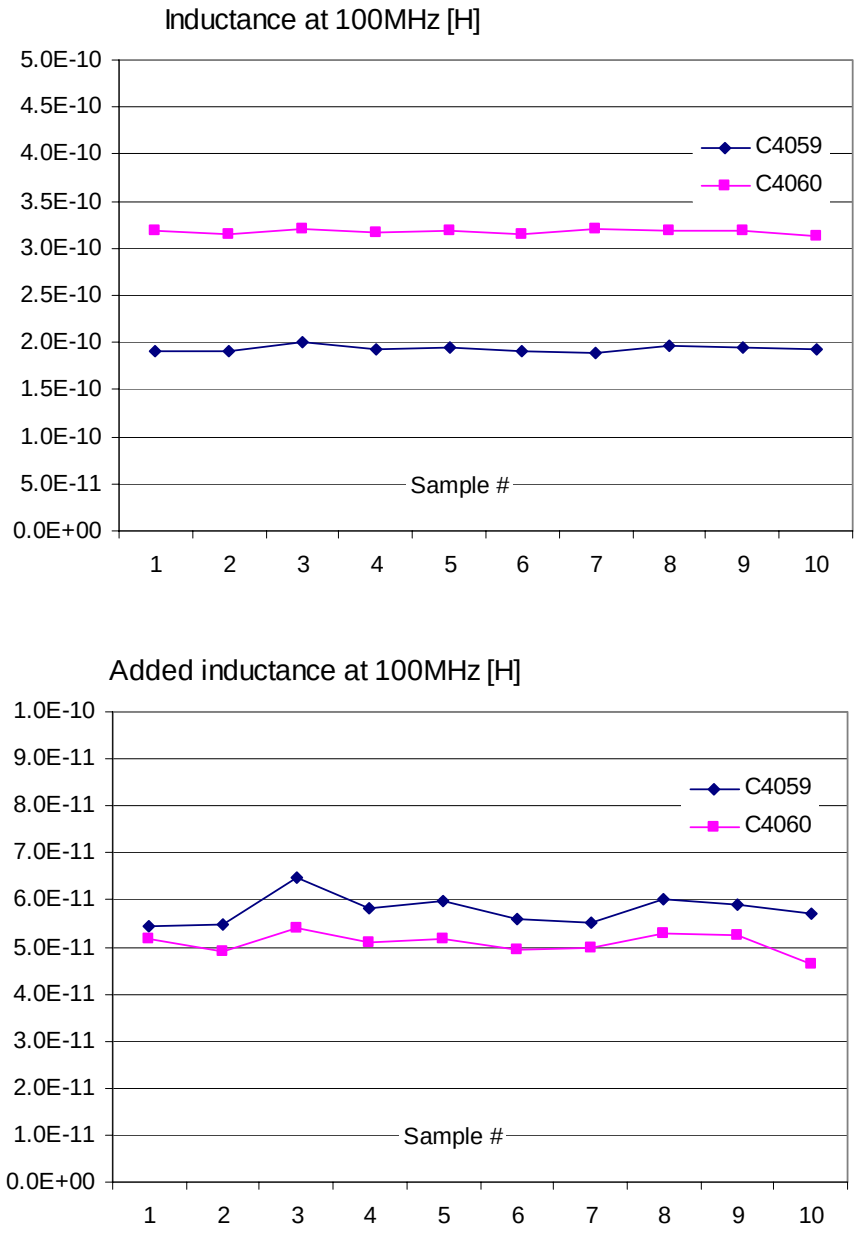

Figure 6. Extracted inductance values for ten 1uF 0306 reverse-geometry MLCC capacitors in two different fixtures. Loop inductance on the left, Added Inductance on the right.

The same trend is shown on Figure 6, which shows the extracted inductance values of ten pieces of 0306-size reverse-geometry MLCC parts. The parts were soldered on two different fixtures. Fixture C4060 had blind-via connections and resulted in lower loop inductance. C4059 had through-hole connections to the same planes. Note that the inductance extracted at 100MHz shows that the blind-via fixture results in higher Added Inductance.

The above measured results prove that (due to mutual inductances between the fixture and capacitor body) the inductance obtained on calibrated fixtures (called Added Inductance above) is ***not unique***.

Towards standardized fixture and data sheet info

It was concluded during [1] that providing the internal geometry data of the capacitor is equally good (in fact, technically this option is the best). To enable the user to simulate the inductance of the capacitor in various mounted configurations, it would be enough to give the geometry numbers of the capacitor-plate stack envelope (details inside the stack matter less). Though the geometry data is available from some of the vendors upon request, this solution works only for large OEMs, where the characterization of selected parts by detailed field-solver simulations may be practically doable.

From a user's perspective, the following requirements are important:

- for each capacitor body style, the fixture should give a defined connection boundary (mechanical and electrical)
- the fixture should leave the flexibility of using different constructions for the internal details (such as via connections, plane location, separation and depth of planes in the stack up)
- a few standard and publicized fixture options should be generated so that data sheets can refer to those standard fixtures (with known geometry)
- the standard fixtures should be made available for customers
- the data extraction method should be standardized

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