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SUN's Experience with Thin and Ultra Thin Laminates for Power Distribution Applications

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Abstract

This paper gives an overview of thin laminate applications at SUN's Scalable Systems Groups, Horizontal Systems (formerly Volume Server Products) business unit. The paper summarizes some of the experimental engineering tests with various thin laminates on test boards and production boards, and gives a brief overview of the application of 1-mil laminates in a recent product.

I. Introduction

Thin and very thin laminates for power-distribution applications have been extensively described in the past. For low-power and low-current applications, the static plane capacitance is the important parameter; thin laminates for such applications are marketed as embedded capacitance [1]. For high-power applications, and above the series resonance frequency of power/ground planes, the inductance is the primary electrical quality parameter [2]. The static capacitance of laminates is usually specified at 1MHz, whereas the inductance is usually calculated as the high-frequency limit inductance, which assumes that the current penetration of the conductive planes is negligible compared to the dielectric thickness. For thin and very thin laminates, however, as it was shown and documented in [3], the inductance, and/or capacitance may be a non-negligible function of frequency.

Power/ground planes in printed-circuit board stackups can be either assigned to non-adjacent layers, such that signal-trace layers can be placed between them, or to maximize the static capacitance and minimize the inductance, the planes can be assigned to adjacent layers. In this latter case, the minimum spacing between the planes depends on the kind of dielectric and copper. In large rigid boards, with regular glass-reinforced resin laminates and ordinary copper with a couple of μm rms or higher tooth profile, the planes cannot be placed closer than about 75um without the danger of eventually developing a short between the planes. Wide-spread commercial use of glass-reinforced laminates with 50μm dielectric became commercially available in the early 90's. This became possible by using low-profile copper and proper treatment and processing of the thin laminate. Until very recently, this was the only commercially available thin laminate for large rigid board applications, though several other options were under development. Moreover, thin materials of 1-mil thickness and less have been around for a while for smaller-size build-up and flex-circuit applications. In the past two years, unreinforced, unfilled and lightly filled thin and very thin laminates became commercially available ([4], [5], [6]).

SUN VSP had the first 50um laminates for power distribution applications in the V880 servers, introduced in the late 90's. Its successor multi-core families, introduced in 2004 and 2005, have 1-mil laminates in the CPU board. This paper gives a brief overview of the electrical tests and experiments leading to the introduction of the 1-mil laminate into these products.

Figure 1.: SUN's V890 server and its CPU module. The CPU module has 1-mil unreinforced laminates on some of its power rails.

II. Electrical testing of thin laminates

The search for a suitable thin laminate at SUN VSP started in 1998. The first requirement was to develop a testing methodology, which could properly measure the electrical behavior of thin laminates, so that various laminate options can be compared and ranked. One challenge lies in the very low inductance of the thin laminates, combined with the fact that in a finished printed-circuit board the thin laminates are typically minimum one layer below the surface. By accessing the thin laminate from the surface through plated through or blind vias, the via inductance can overwhelm the measured impedance, masking out differences among the various laminates. Another challenge is the overall low impedance; conventional impedance analyzers are not suitable for accurate measurements of sub-ohm values in the hundreds of MHz frequency range and above. Both challenges can be overcome by using a Vector Network Analyzer (VNA) in two-port connections, similar to four-wire DC resistance measurement configurations [7], [8].

Port 1 of the VNA sends out a calibrated constant voltage behind its 50-ohm source impedance. The current generated by the source voltage creates a voltage drop, which is being picked up by Port 2. When we use the same pair of vias from opposite sides of the board for connecting Port 1 and Port 2, effectively the via inductance is removed from the picture up to a few GHz. At the same time, using Port 2 to pick up the voltage across the unknown impedance guarantees a high dynamic range. This allows us to properly measure, characterize and compare the various thin laminates. The method is also convenient for laminate testing [9].

Figure 2 illustrates and compares the results of these options. Two 10"x5" test boards were measured. Both boards had one plane pair, 3 mils from the top surface and 90 mils from the bottom surface. When the impedance is measured through the 90-mil long vias from the bottom (labeled: far side), the impedance fluctuations are completely masked out by the large via inductance, and we see no performance difference between the 50-μm and 8-μm laminates. When measured from the top (labeled: near side), the via interferes much less with the measured self impedance, but in case of the 8-μm laminate, the inductance at high frequencies is still three times higher than by measuring from opposite sides.

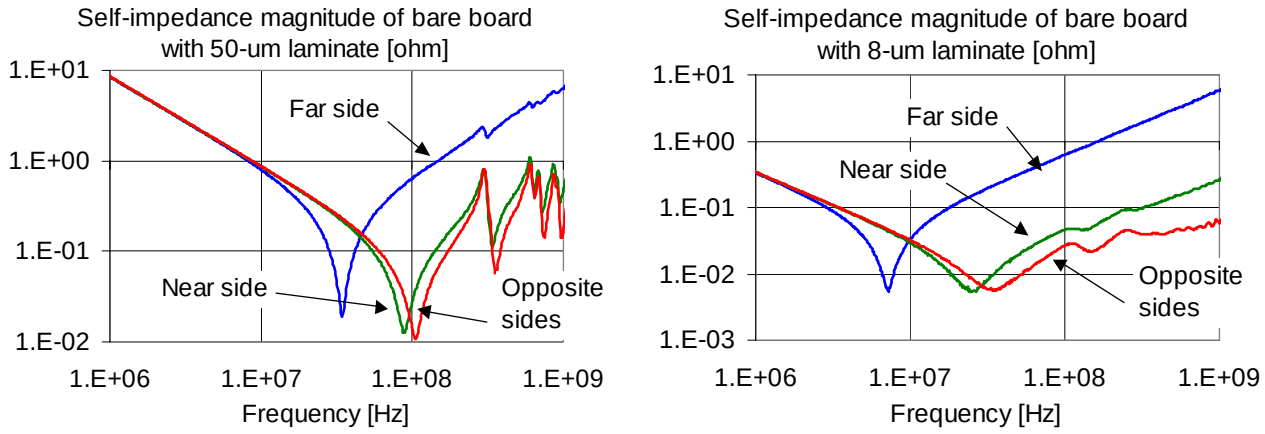

Figure 2.: Difference between laminate impedances measured from the same side versus opposite sides. On the left: 50µm laminate; on the right 8µm laminate.

III. Test boards and engineering tests

Between 1998 and 2003 a large number of laminates have been tested in various engineering test boards. The very first successful test boards of 20”x10” size with 1-mil laminates were made in 1998-99. These boards (Figure 3) were fabricated with DuPont’s 1-mil polyimide laminate.

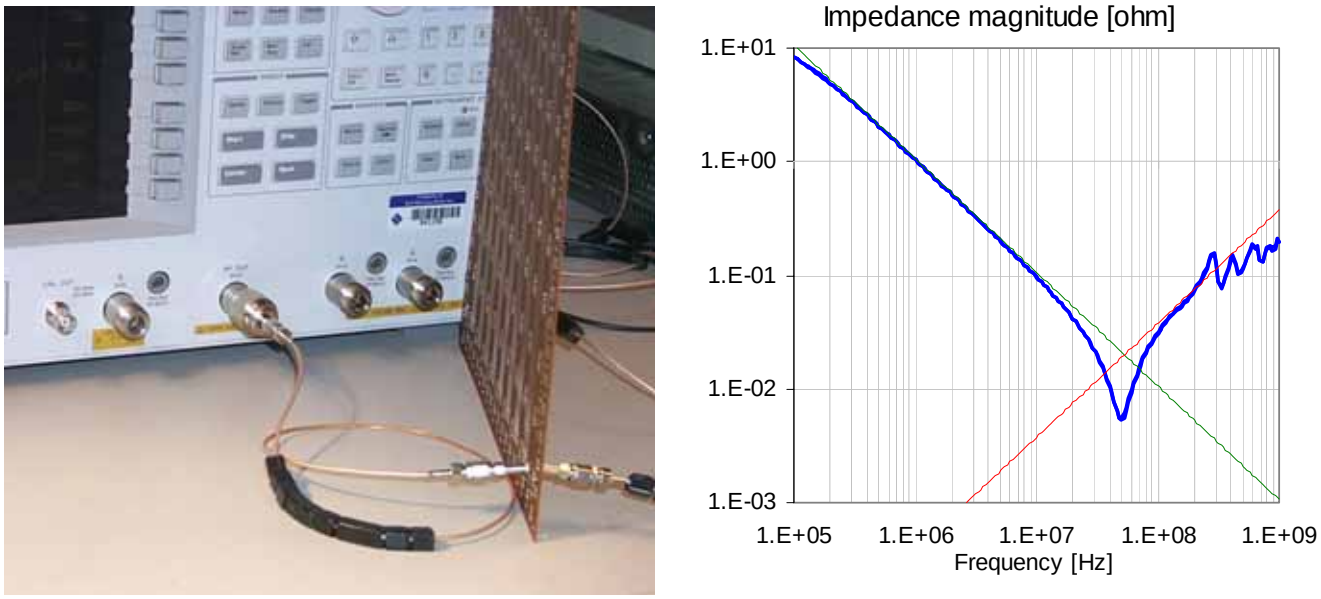

Figure 3.: One of the first SUN test boards with ultra-thin laminate. The board was designed in 1998, the finished board was received and tested in 1999. The photo on the left shows the instrumentation, and the VNA connections. The impedance plot on the right shows the self-impedance magnitude at one of the test via pairs. The thin straight green line represents the impedance of the board’s static capacitance (0.15µF). The thin red line corresponds to the impedance of 60pH inductance.

Later smaller-size (10”x5”) test boards and experimental versions of production boards with thin and very-thin laminates were fabricated. Figure 4 shows the extracted inductance versus frequency curves of

thirteen different laminates fabricated with the same 10”x5” test-board construction [3]. The inductance was obtained from the imaginary part of the measured self impedances of the shorted boards. The shorted capacitor sites were along their perimeters at one inch intervals.

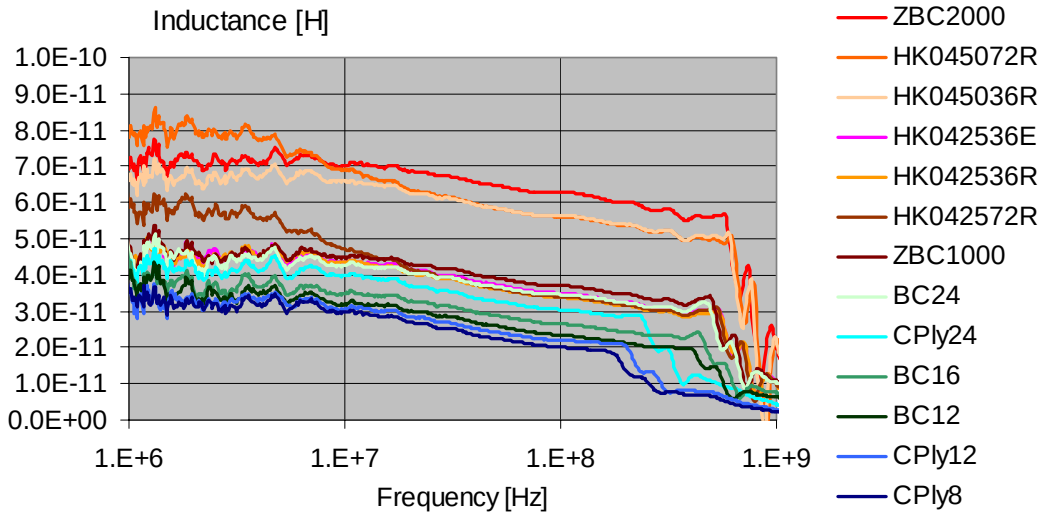

Figure 4: Inductance versus frequency curves of various laminates from Matsushita (ZBC2000 and ZBC1000), DuPont (HK04), Oak-Mitsui (BC) and 3M (CPly). The sequence of legend on the right corresponds to the top-down sequence of curves.

Figures 5 and 6 show some of the results of the engineering tests on a production board. The board was a CPU card with an approximate size of 6”x 4”. The card had several power-ground plane pairs on two major Power Distribution Networks (PDN). Impedance measurements showed that at high frequencies, where the bypass capacitors become inductive, the resulting PDN impedance was approximately proportional to the laminate thickness. It was also demonstrated that modal resonances from the power/ground plane cavities become more dampened as the plane separation gets below 1 mil, and almost completely disappear with laminate thicknesses of 0.5 mils or less, as explained in [12].

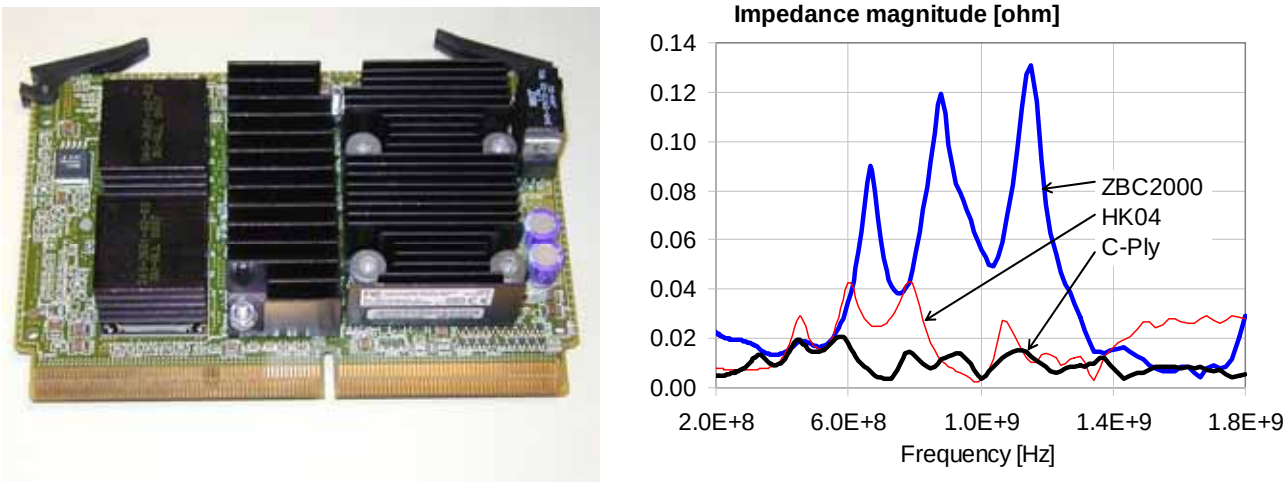

Figure 5.: Photo and impedance magnitude plots of an experimental fully populated server CPU board with three different thin and very-thin laminates.

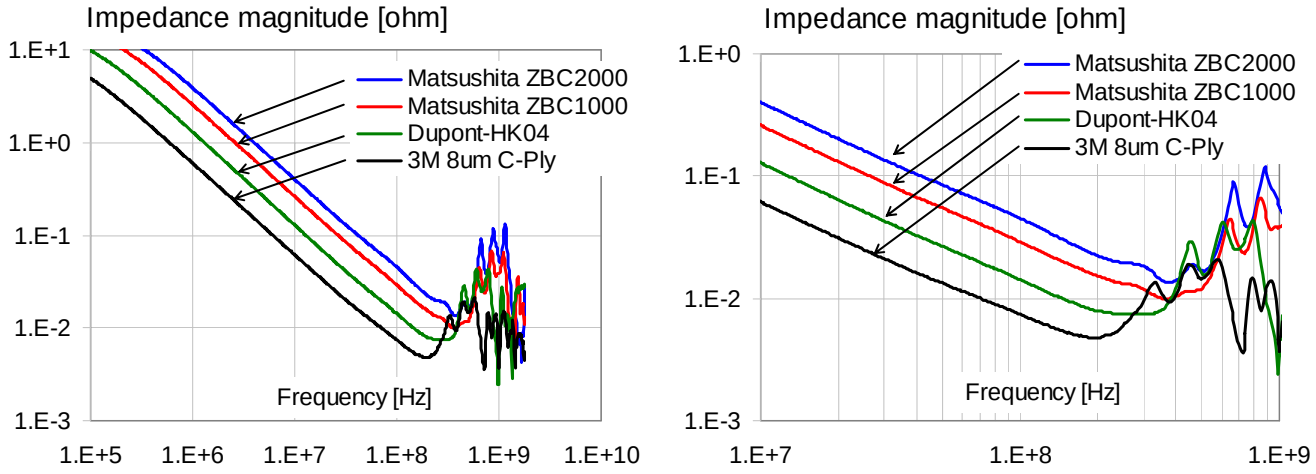

Figure 6.: Measured impedance magnitude of the unpopulated boards from Figure 5 with two Matsushita, one DuPont and one 3M laminates. Left: full 100kHz-1800MHz frequency range. Right: zoomed 10-1000MHz frequency range.

IV. Product application

After the extensive electrical testing, the chosen 1-mil laminate was put through qualification testing in the target product. PCB fabrication quality tests, reliability and assembly tests were performed first with DuPont HK042536E, later also with the Oak-Mitsui BC24 laminate. The photo in Figure 7 shows the bare board of the CPU module of a V890 server with one of the PDN rails measured. Figure 8 shows transfer impedance and self impedance plots on two other PDN rails of the same boards, comparing impedance values with 2-mil and 1-mil laminates. Figure 9 shows the board measured at the CPU area with PicoProbe connections. The photo shows the setup for measuring transfer-impedance along the diagonal of the core area.

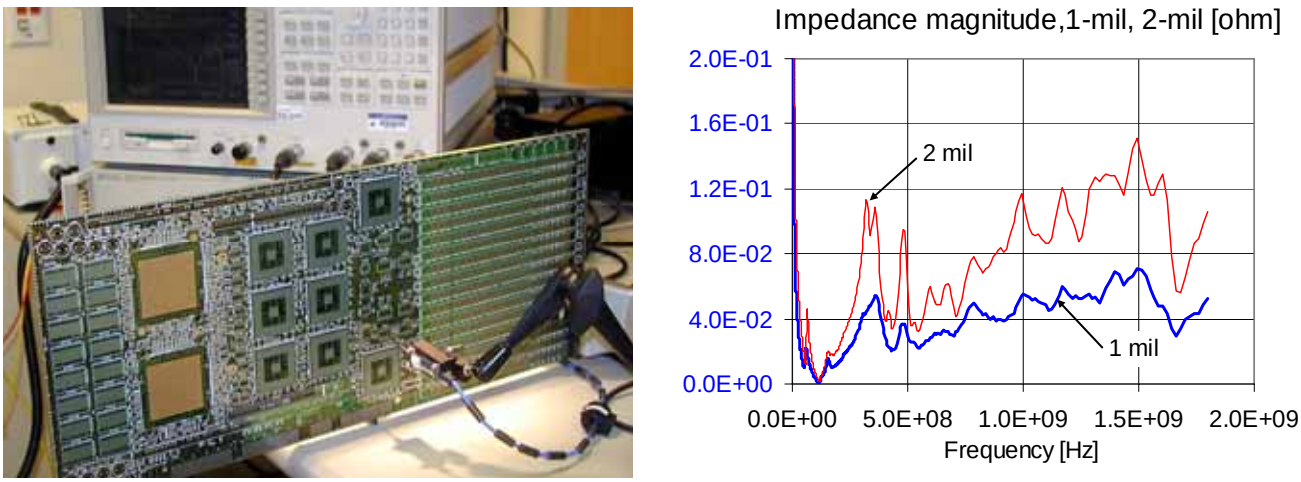

Figure 7.: Photo of impedance testing setup with semirigid coaxial probes. The DUT is the bare CPU board of a V890 server. The plot on the right shows the impedance magnitudes at one of the test points measured on two variants of the same board; one with 2-mil, the other with 1-mil power-ground laminates.

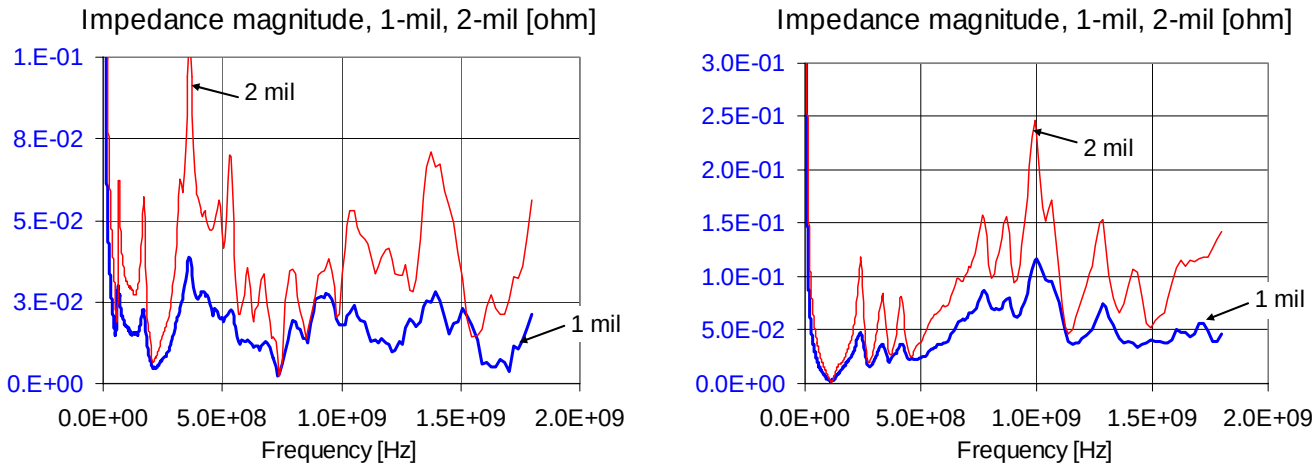

Figure 8.: Transfer-impedance example on the left, self-impedance example on the right, comparing the impedance performance with 2-mil and 1-mil laminates. The two plots refer to different PDN supply rails.

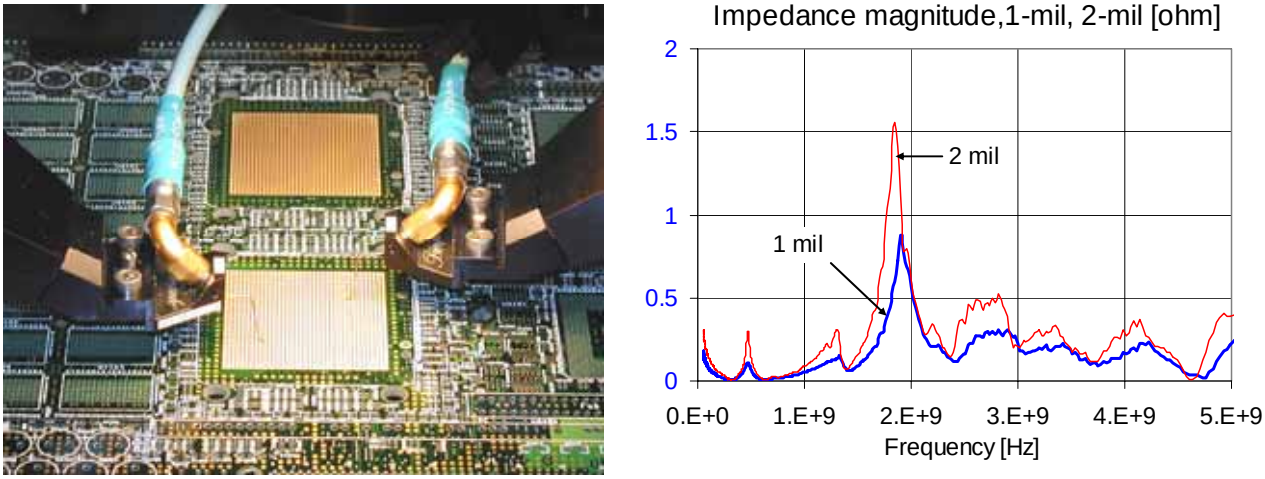

Figure 9.: Measurement connection with PicoProbes, to measure the transfer impedance along the diagonal of the core via-array area. The plot on the right compares the measured transfer impedance magnitudes with 2-mil and 1-mil laminates.

Figures 10 and 11 show cross section photos, courtesy of Benchmark. Copper plating adhesion to the polyimide laminate, and copper plating adherence to copper planes around via joints were tested with 6x solder shock. The photos indicate good adherence and no sign of delamination.

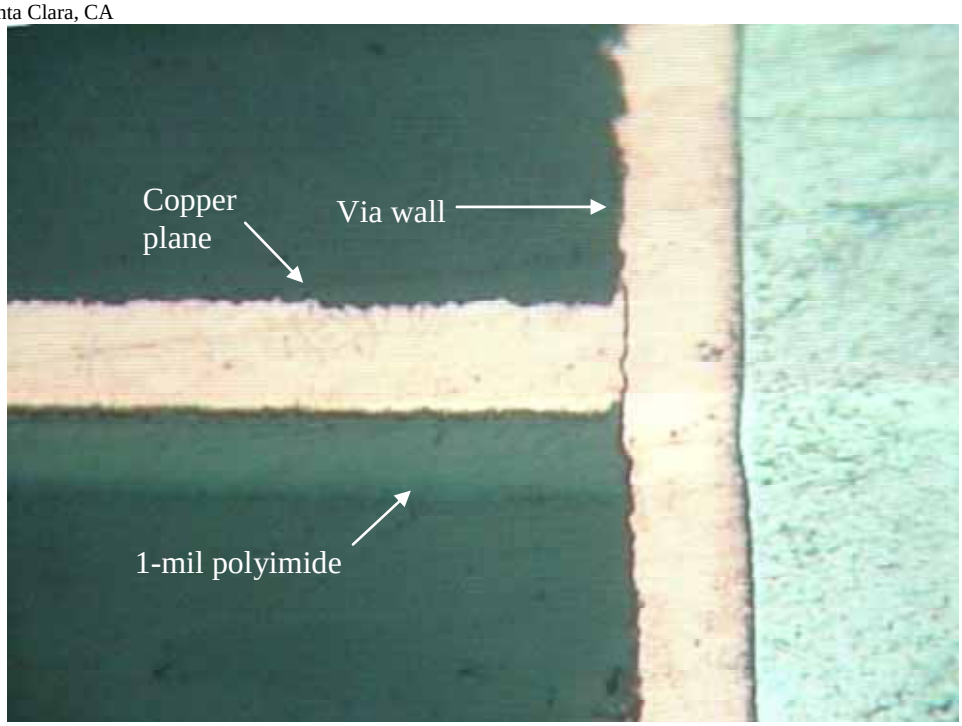

Figure 10.: 1-mil HK04 laminate and via joint after 6x solder shock. Photo courtesy of Benchmark.

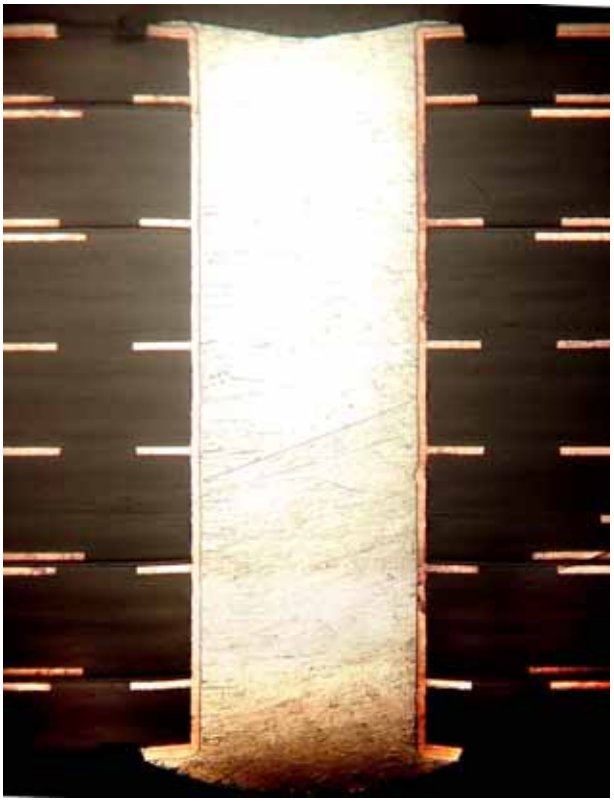

Figure 11.: Cross section at a via with 1-mil HK04 laminate after 6x solder shock. Photo courtesy of Benchmark.

V. Benefits of thin laminates

The often cited benefits of thin power-ground laminates are:

- Reduced power-rail noise
- Reduced EMI radiation
- Reduced number of bypass capacitors, hence reduction in cost and board real-estate for PDN

Note that while the reduced high-frequency power-rail noise is easily quantifiable by comparing impedance profiles, the EMI radiation is usually the result of multiple sources, and each radiating source on a board may have different activities, and therefore proving the EMI benefits of thin laminates on an actual product is not straightforward. Similarly, multiple design choices exist for PDN designs, and therefore comparing the numbers of bypass capacitors on a design with and without thin laminates is not straightforward either. For the above reasons, this summary report includes only impedance-profile comparisons.

Conclusions

The V890 server successfully introduced the first 1-mil laminate at SUN Microsystems for PDN applications. The impedance tests of the boards with different laminate thicknesses clearly showed the electrical benefits of reduced resonances and lowered high-frequency impedance.

Acknowledgements

The test boards mentioned here were fabricated by Altron (now Sanmina-SCI), Merix and Sanmina-SCI. Interra, FaradFlex, ZBC2000, ZBC1000, C-Ply are trademarks of DuPont, Oak-Mitsui, Sanmina, Sanmina, and 3M, respectively. The qualification of the 1-mil laminate was headed by Karl Sauter, SUN Microsystems. Assembly tests were carried out by Benchmark.

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