History of Controlled-ESR Capacitors at SUN

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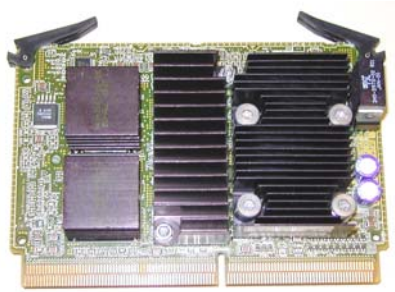
Outline

- Introduction
  - The need for controlled-ESR capacitors
  - Solution: Distributed Matched Bypassing
- Possible implementations
  - Discrete
  - Embedded R
  - Controlled-ESR MLCCs
  - Controlled-ESR bulk
- Summary/conclusions

The Need (1)

Evolving landscape:

- Higher density
- More independent power rails
- Shrinking supply voltages and noise margins

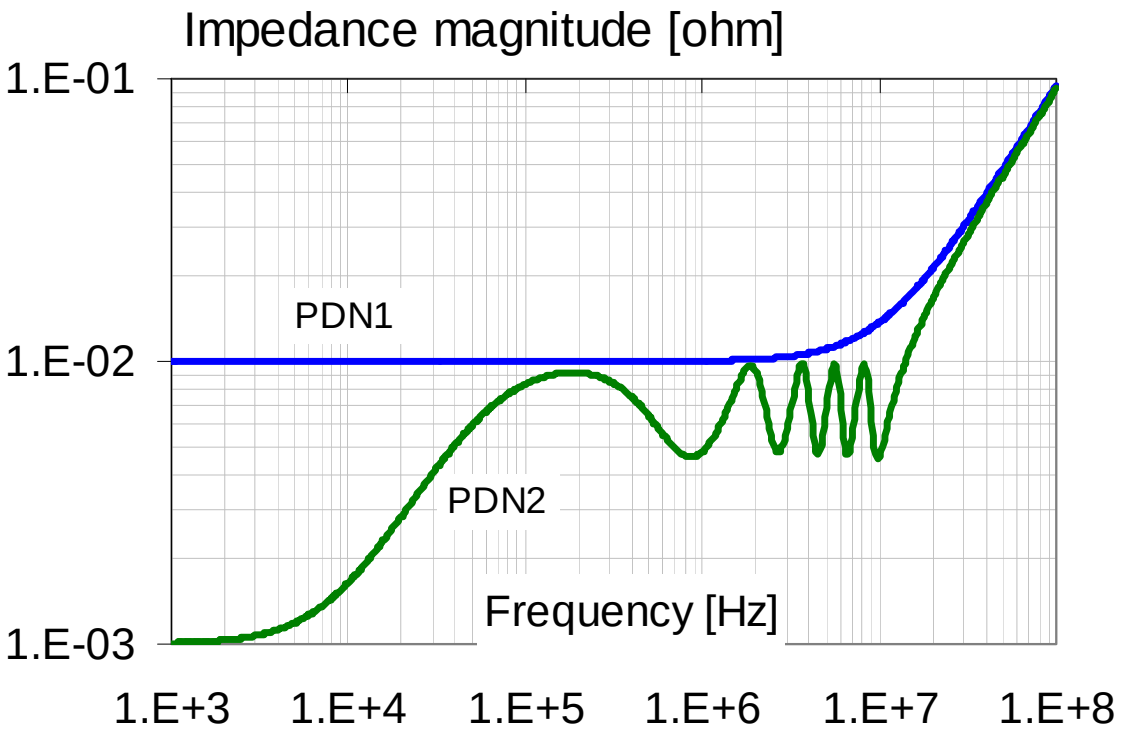


CPU module from early 90's

CPU module from 2000

The Need (2)

- PDN design is usually done in the frequency domain
- Target impedance is specified
- PDN is considered better if Z is lower

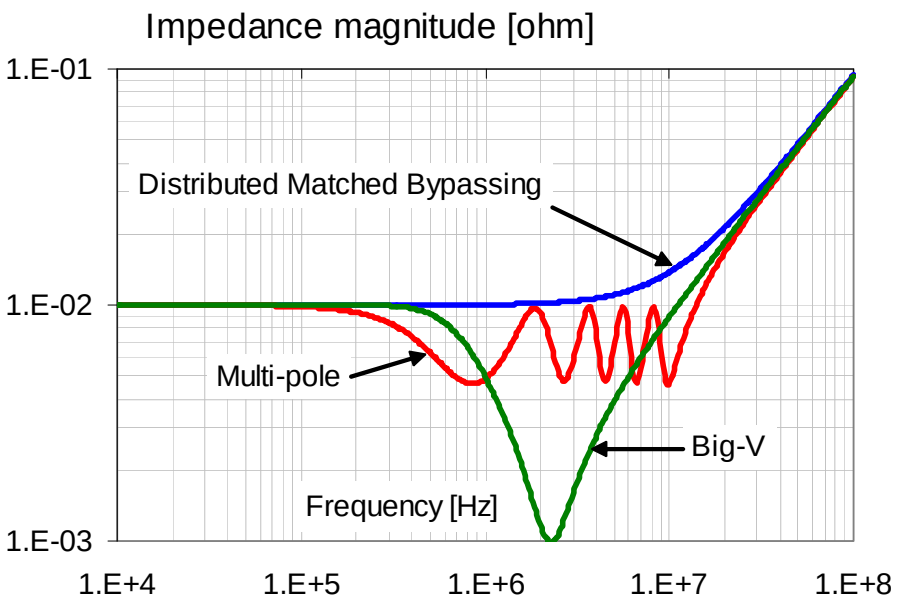


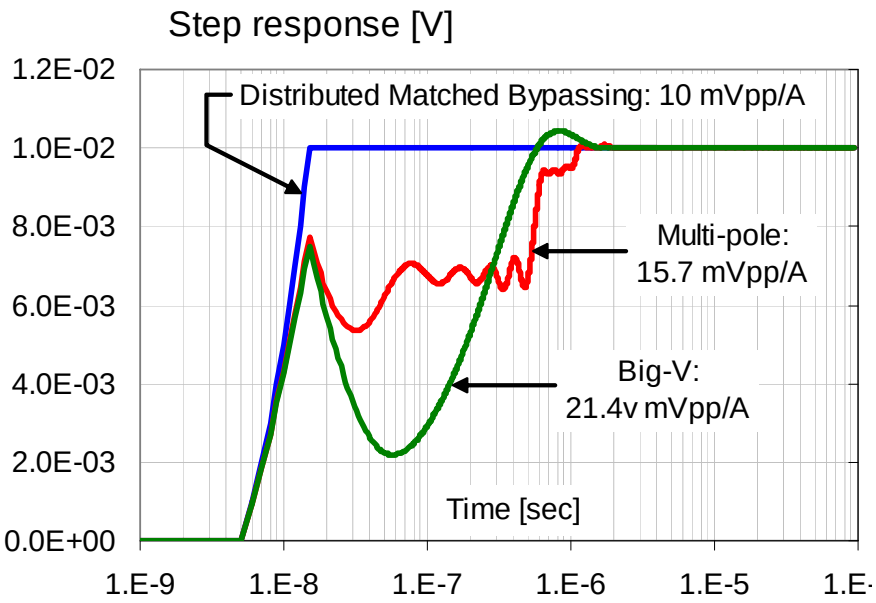
PDN2 is better than PDN1

Or is it???

The Need (3)

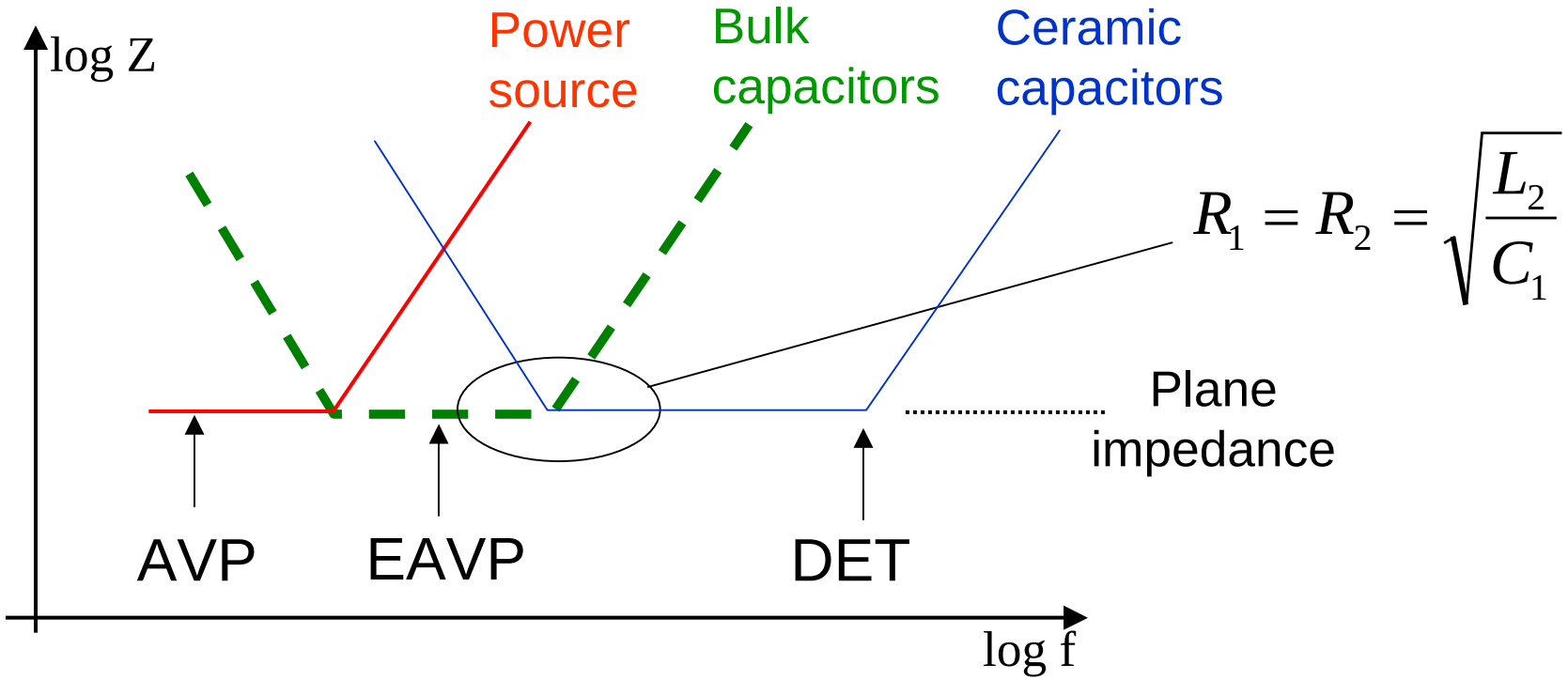
- The worst-case transient noise is the lowest for flat R-L impedance
- The goal should be to minimize impedance ripple





The Solution: DMB

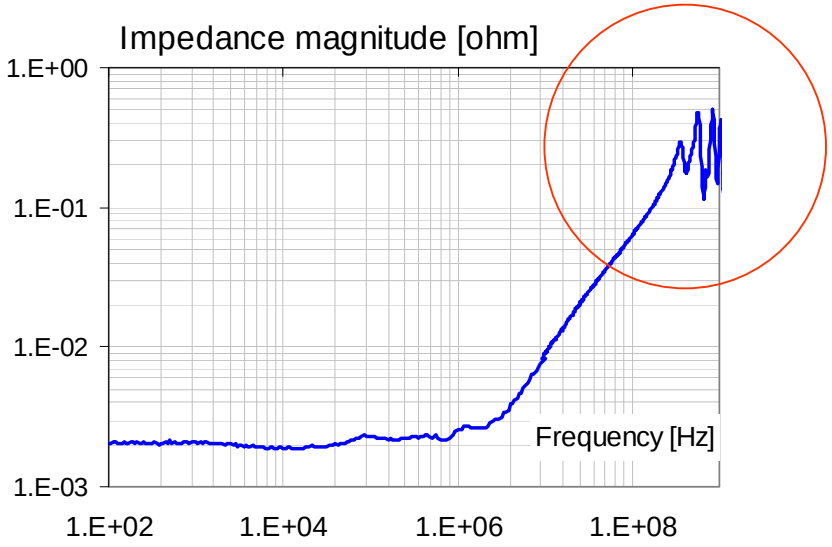
- Distributed Matched Bypassing (DMB) creates flat impedance by
  - > Using low-Q components distributed evenly
  - > Matching the adjacent banks along frequency
- DMB assumes known ESR (+- tolerance)

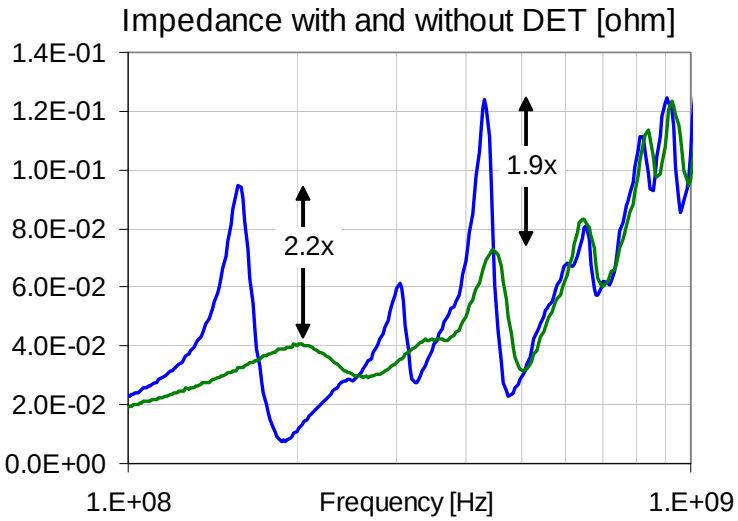


Possible Implementations: Discrete

For ohms ESR, discrete series R is doable:

- R-C pairs
- Distributed along plane periphery, or
- Distributed over the plane area

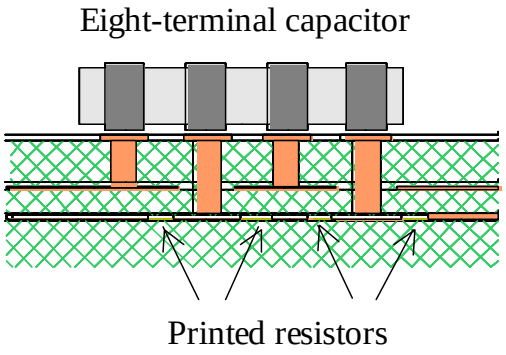


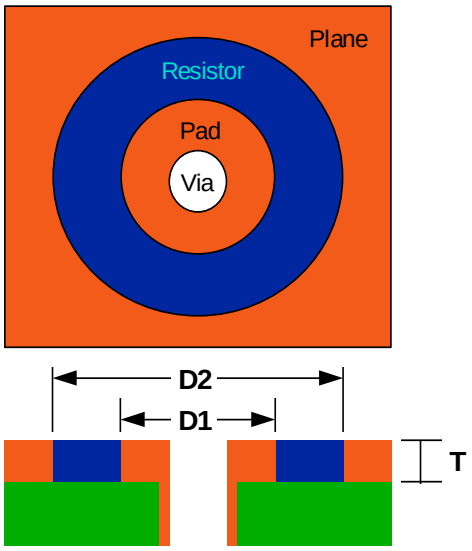


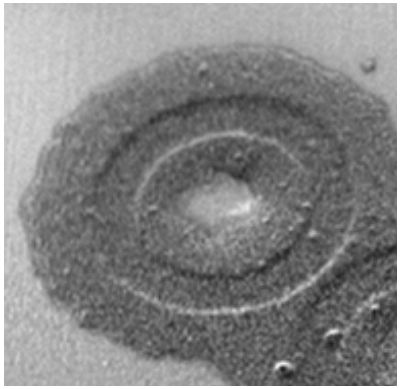
Possible Implementations: Embedded

ESR or regular multi-terminal capacitor is raised:

- Thick-film printed resistors
- Annular ring construction

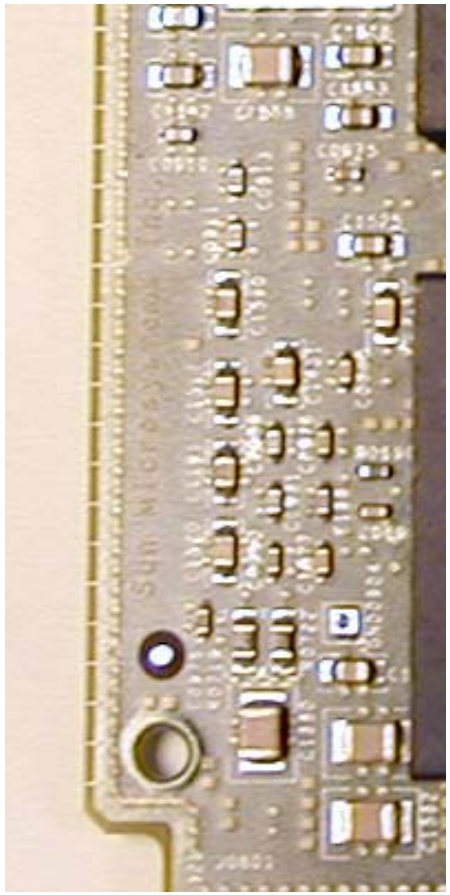




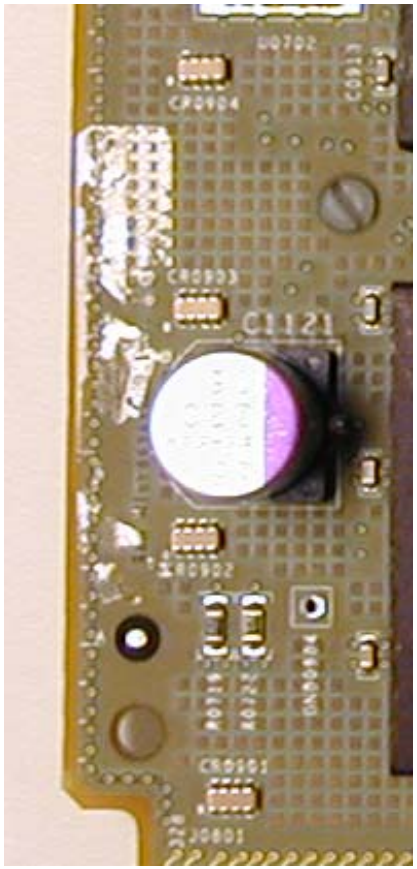


Embedded Implementation

Conventional bypassing



DMB with annular ring resistors

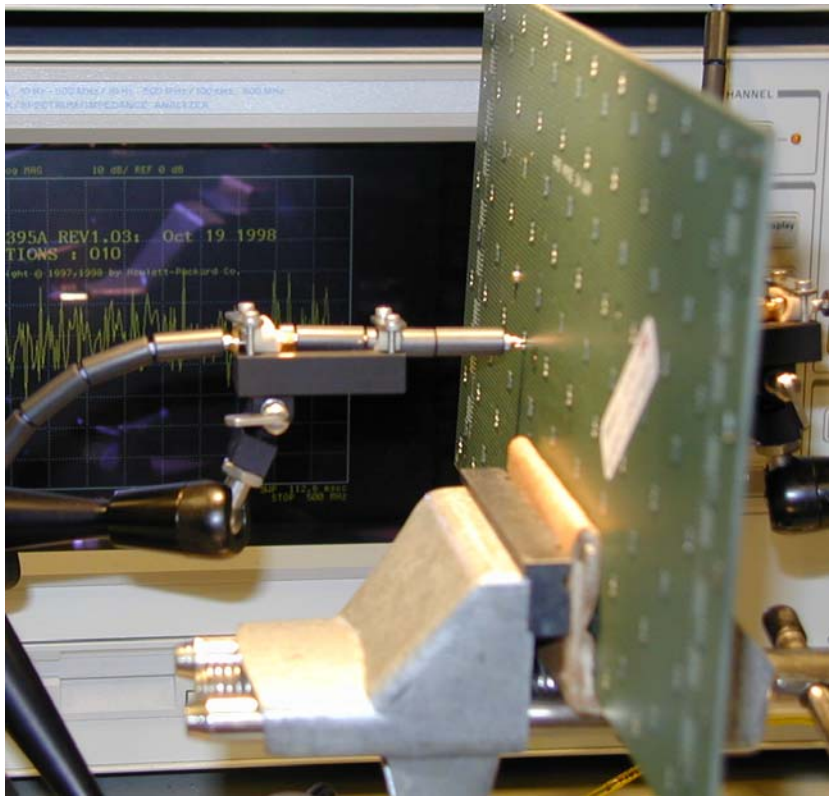


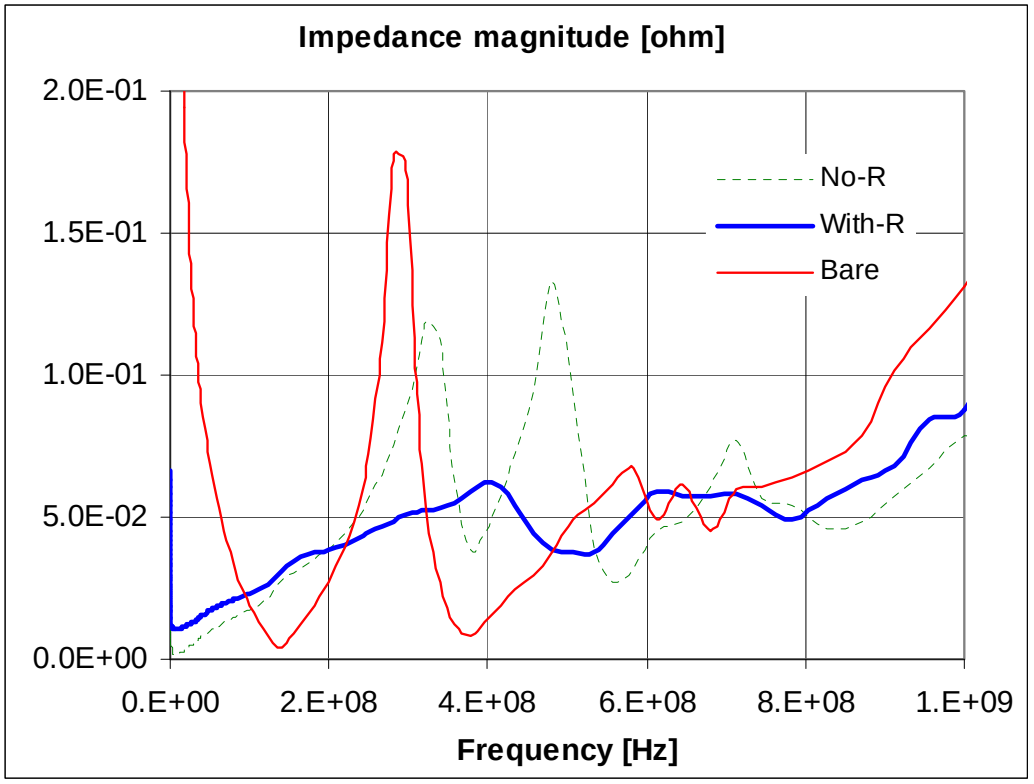
Simplified PDN:

304 >>94 capacitors

Flat impedance profile

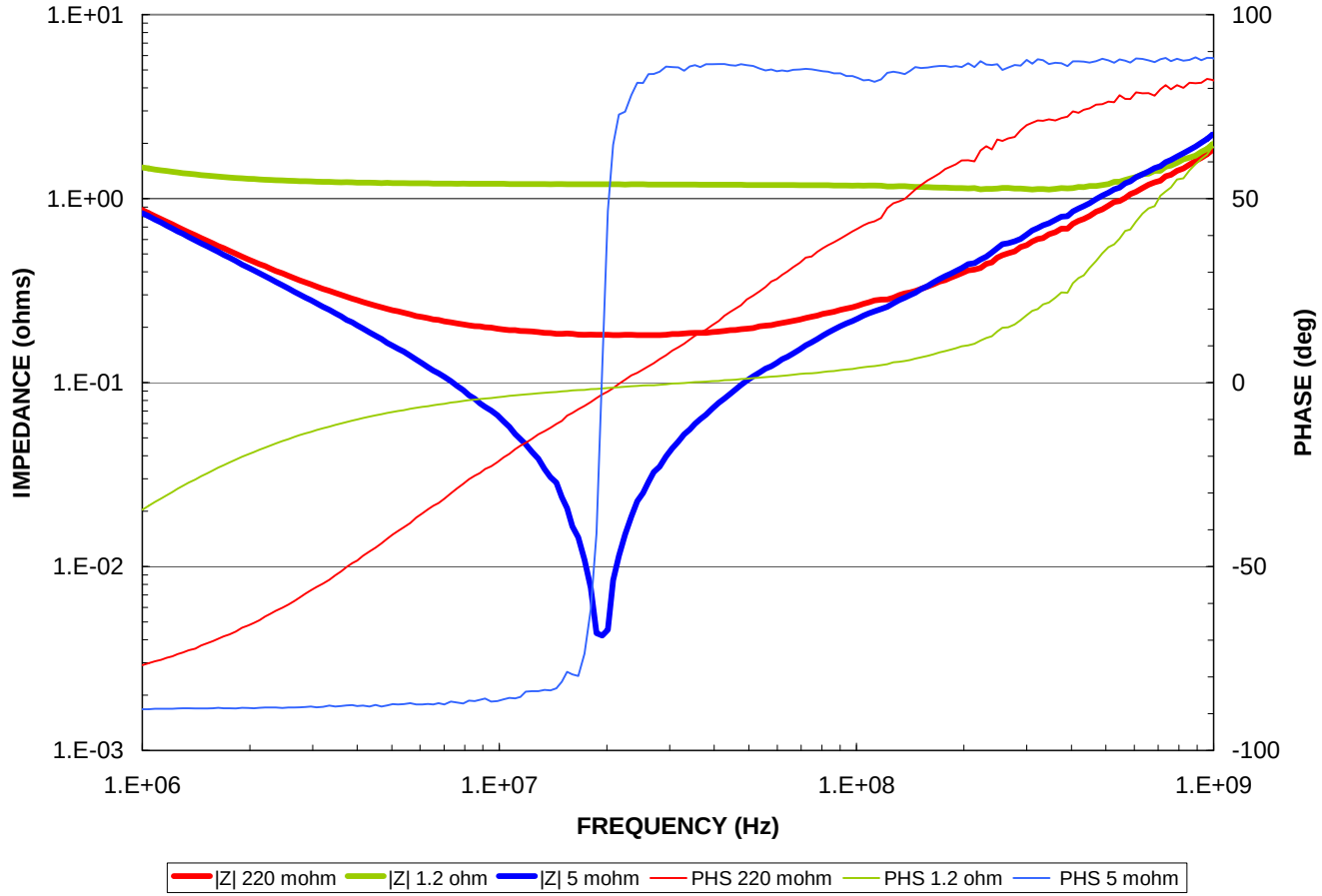
Embedded Implementation: Results



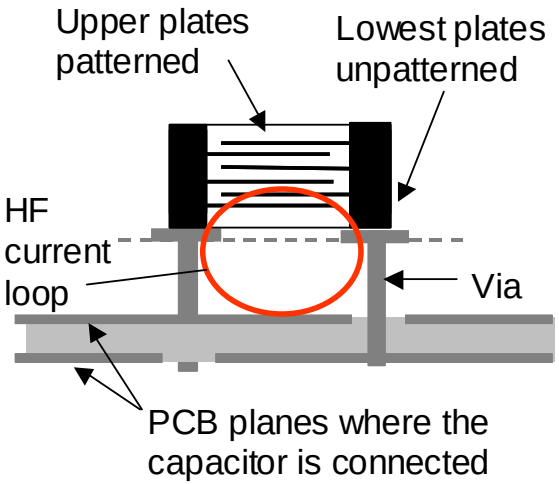


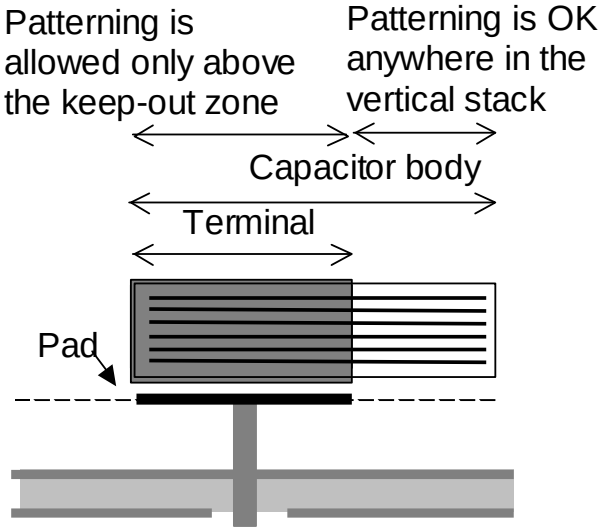
Controlled-ESR MLCC Capacitors

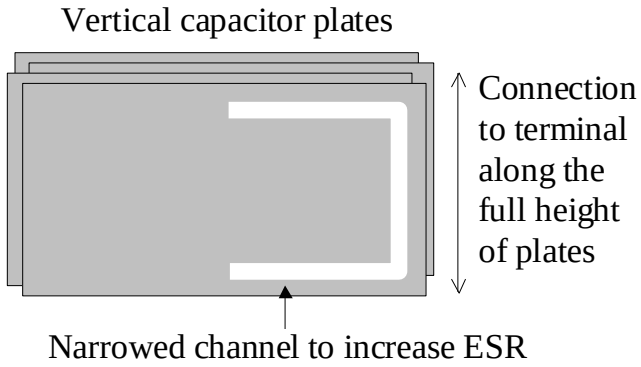
AVX test results

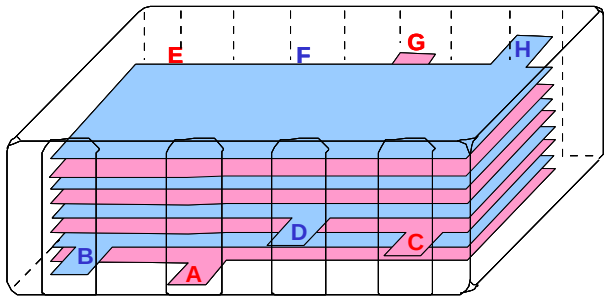


Controlling ESR By Patterning







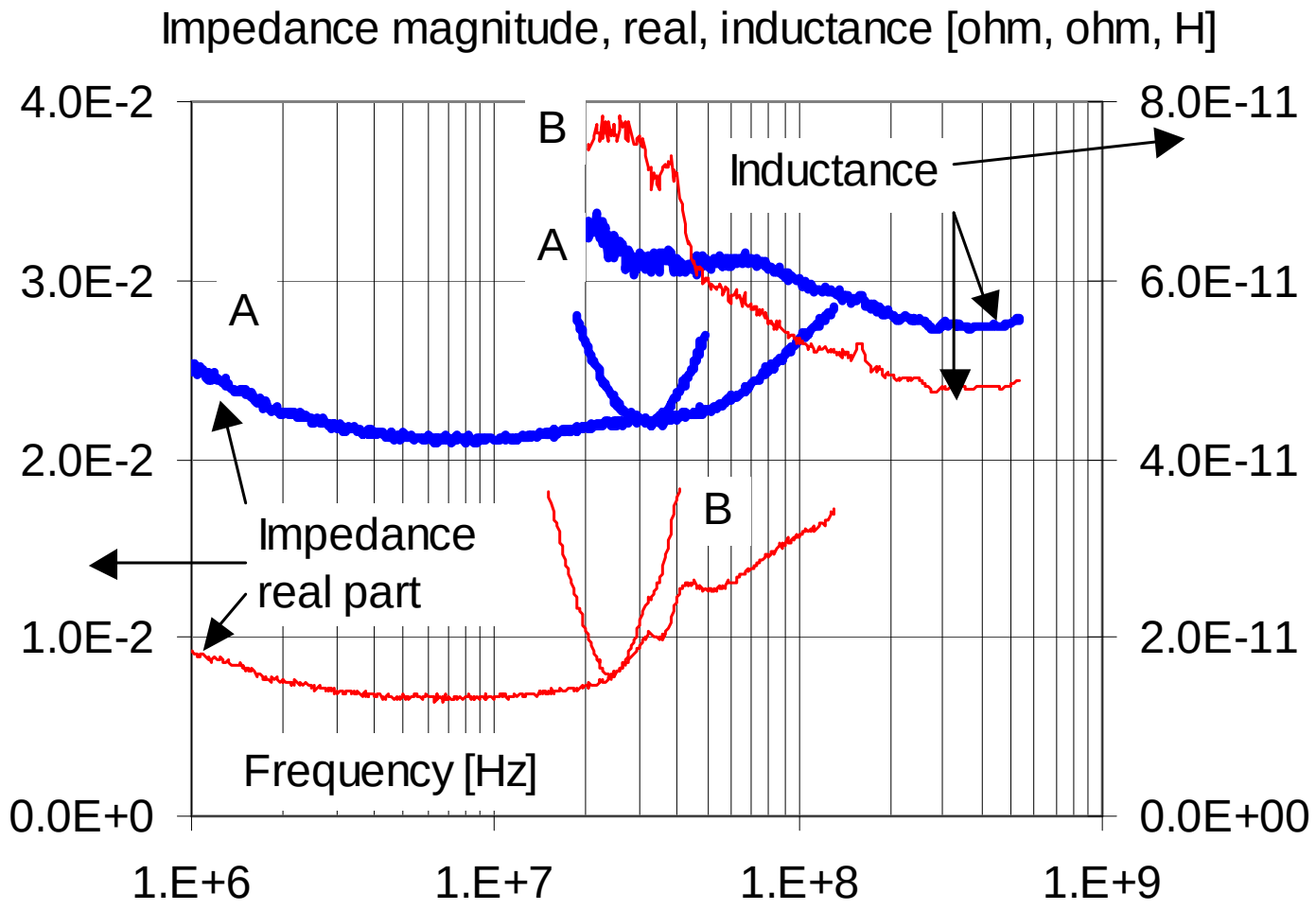


ESR and ESL can be (almost) independently changed by:

- Patterning plates inside and outside of the HF loop
- Changing plate connections to terminals
- Changing the aspect ratio(s) of the part

Patterning Results in MLCCs

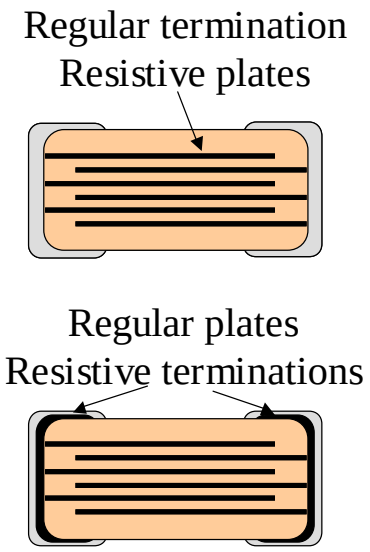
ESR adjustment in 8-terminal part by changing connections to terminals

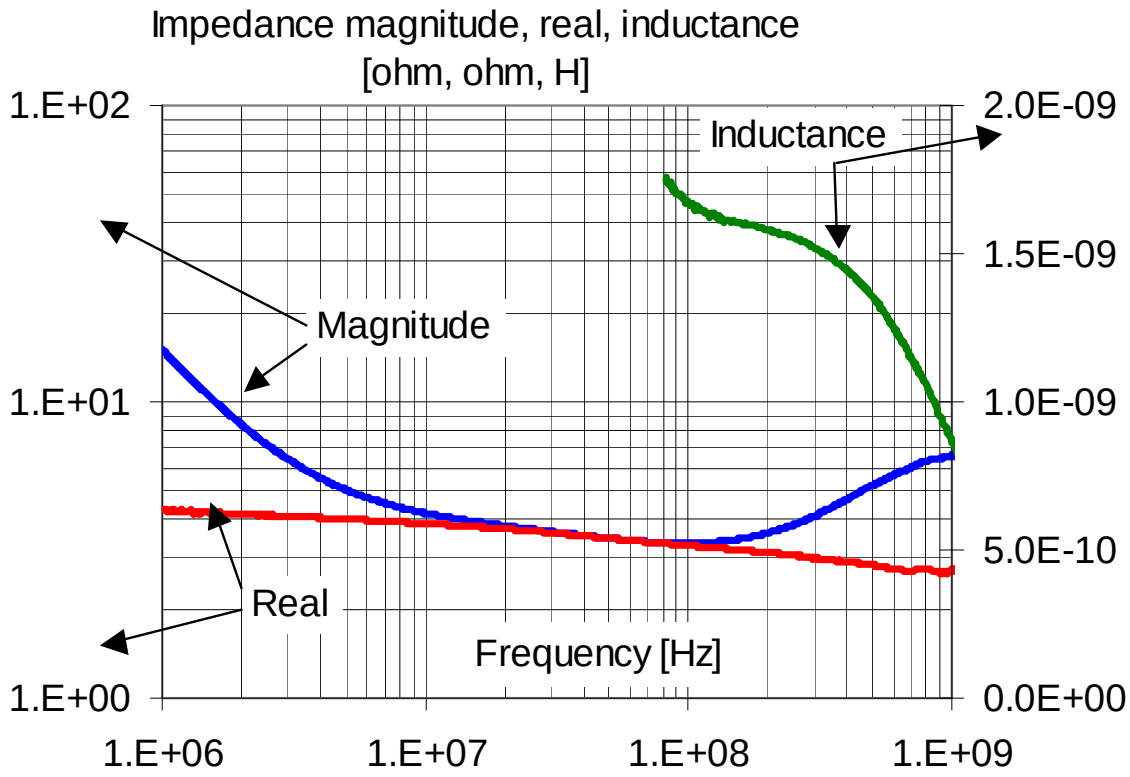


Controlling ESR by Resistive Plates

ESR can be increased by raising the resistivity of:

- Capacitor plates, or
- Terminals

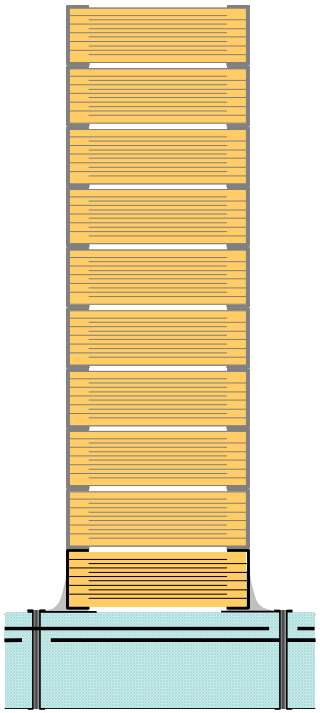


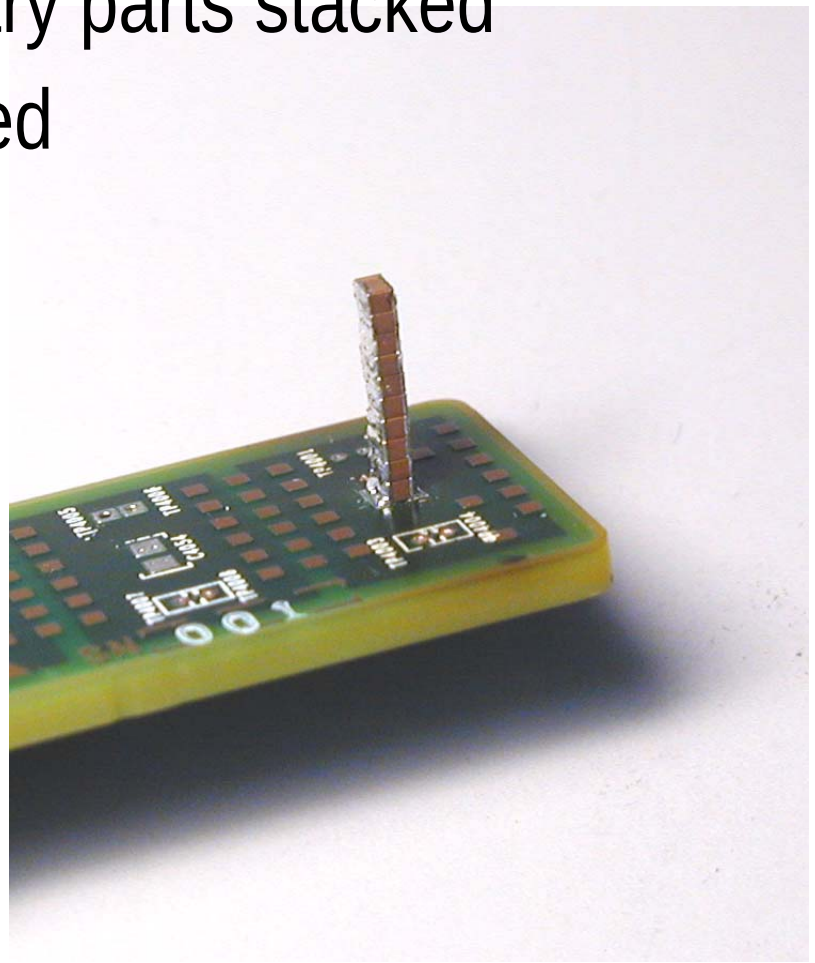


Controlling ESR by Aspect Ratio

Tests with stacked capacitors:

- One to ten reverse-geometry parts stacked
- Impedance profile measured

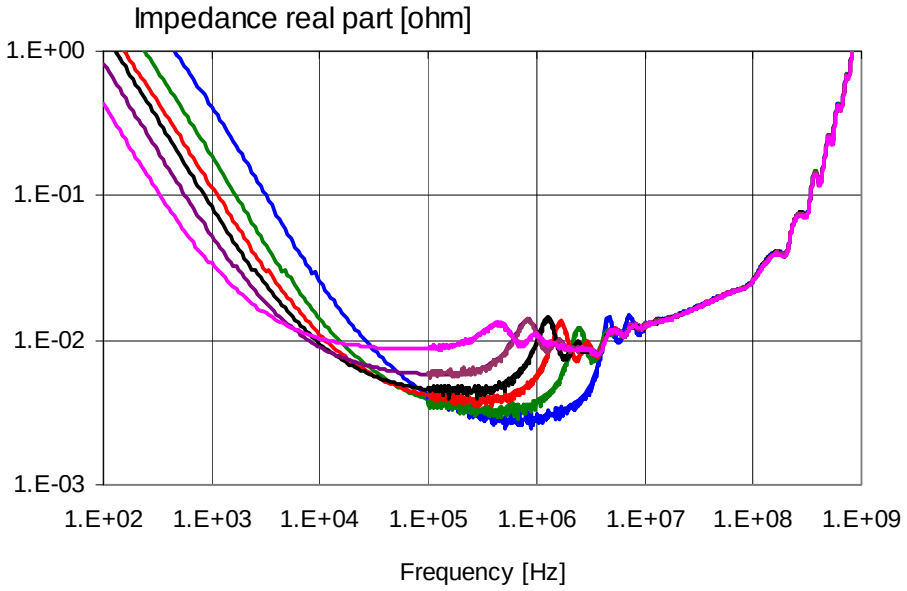


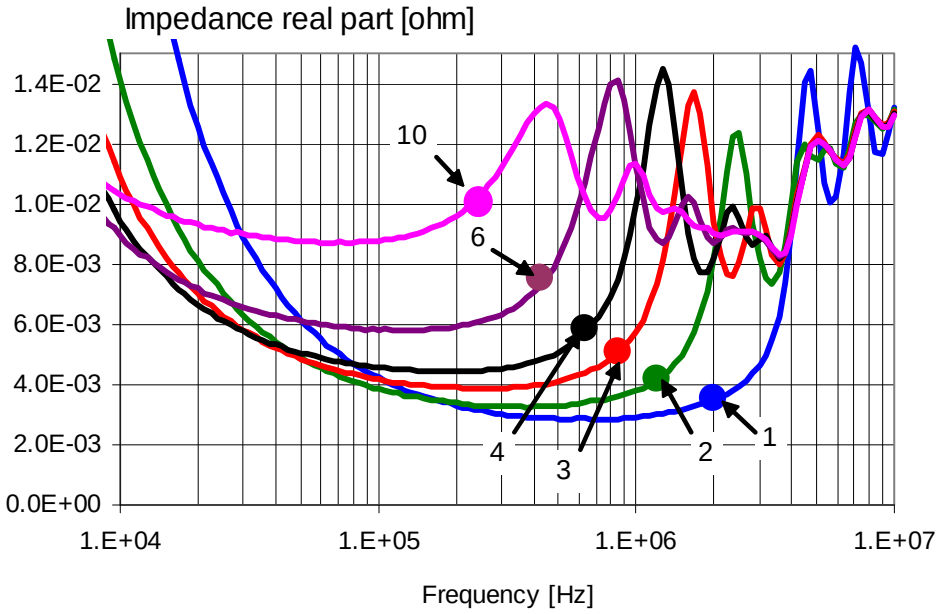


Changing Aspect Ratio: Results

ESR goes up as height of part increases!

Inductance does not change beyond the secondary resonances

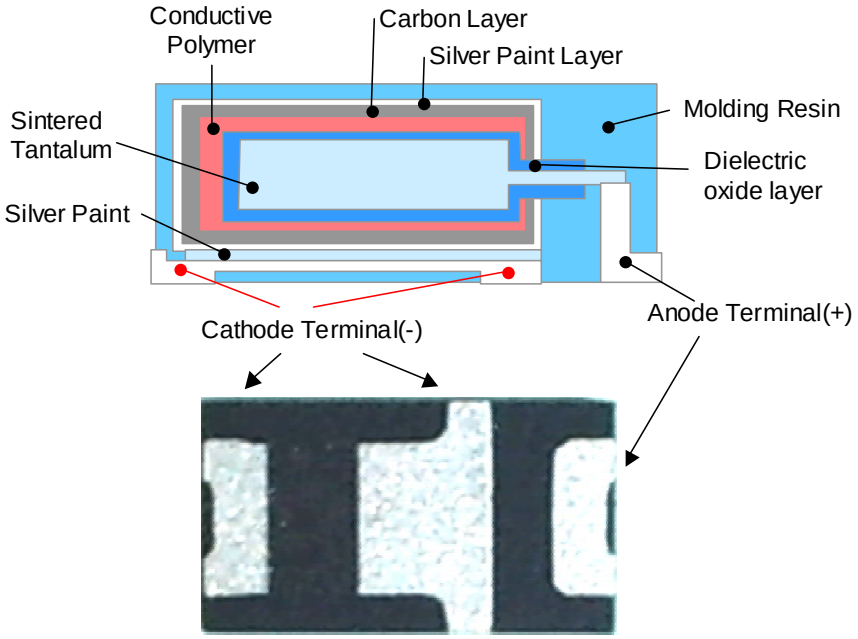


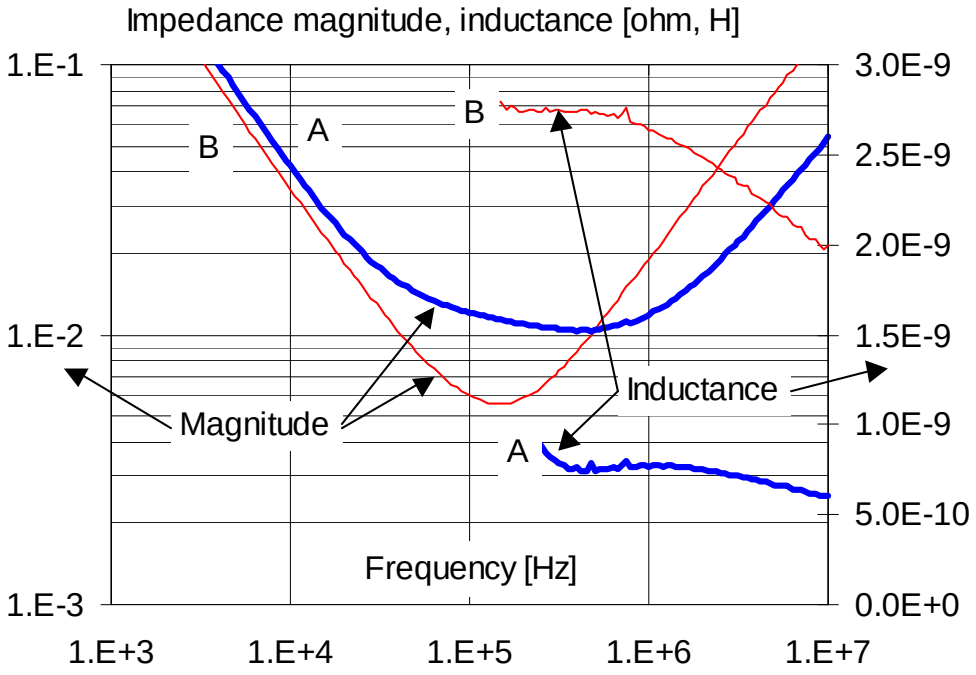


Controlled-ESR Bulk Capacitors

Low Q can be achieved by

- Low inductance, and moderate ESR
- ESR has to be tested for Max





Summary

- Optimum PDN is achieved with matched capacitor banks
- Known +- tolerance of ESR helps PDN design
- ESR can be adjusted and controlled in several ways
  - > Added discrete resistor
  - > Embedded resistor
  - > Resistive terminals
  - > Resistive plates
  - > Patterning of plates
  - > Adjusting aspect ratio and connection geometry

Conclusions

- Low-Q bypass capacitors can be created in both bulks and MLCCs
- Increased ESR does not increase inductance (if done properly)
- Low-cost manufacturing options make controlled-ESR parts affordable

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THANK YOU