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Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range

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Abstract

This paper discusses practical solutions for improving the quality and accuracy of frequency-domain Power Distribution Network (PDN) component measurements in the near-DC to MHz frequency ranges, which is gaining increasing importance in PCB-level applications of today's low-voltage digital circuits. The paper discusses and illustrates how to measure the characteristics of DC-DC converters more accurately by understanding measurement accuracy, the limitations and error sources of different measurement systems. It also shows how to accurately characterize Multi-Layer Ceramic Capacitors (MLCCs) and inductors/ferrite beads that have AC-signal and DC-bias dependences. The paper introduces new approaches to the milliohm impedance measurements and AC/DC-biased impedance measurements with a new 5 Hz-to-3 GHz Vector Network Analyzer (VNA).

Author Biographies

Istvan Novak is signal-integrity senior staff engineer at SUN Microsystems, Inc.
In addition to signal-integrity system design of high-speed serial and parallel buses, he is engaged in the methodologies, designs and characterization of power-distribution networks and packages for workgroup servers. Istvan has thirty years of experience with high-speed digital, RF, and analog circuit and system design and has twenty two patents. He is Fellow of IEEE for his contributions to the signal-integrity and RF measurement and simulation methodologies.

Yasuhiro Mori is a senior product manager for the Component Test Division of Agilent Technologies in Kobe, Japan. He is responsible for product marketing and application developments for the network analyzers. During his 18 year carrier in Agilent, he experienced a variety of roles in the marketing fields related to the network analyzers and impedance analyzers. Most recently he worked for the new LF-RF network analyzer and its applications including PDN measurements.

Mike Resso is the Signal Integrity Measurement Specialist in the Component Test Division of Agilent Technologies and has over twenty-five years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high speed digital interconnects using Time Domain Reflectometry and Vector Network Analysis. He has authored over 30 professional publications including a book on signal integrity. Mike has been awarded one US patent and has twice received the Agilent "Spark of Insight" Award for his contribution to the company. He received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

1 Introduction

The frequency-domain PDN impedance characterization is of increasing significance in the trend toward lower voltage operations, and VNA-based impedance measurement techniques are widely used among PDN designers. The fundamentals of this measurement methodology has been well-established ([1], [2], [3]), but still there are some challenges to be solved for more accurate measurements, especially in the near-DC to MHz frequency range.

An ongoing challenge in the near-DC to kHz frequency range is the difficulty to have confidence about the accuracy of measuring extremely small impedances of DC-DC converters or shorted conductor structures that may go to sub-milliohm values. To be confident about the measurement accuracy, it is necessary to understand the characteristics of the measurement system (including not only the VNA itself but also other test accessories being used), the limitations of the low impedance measurement range, and also it is desired to have a practical method for verifying the measurement accuracy and error-floor of the system. The two major limiting factors, the cable-braid ground loop [1] and instrument noise floor are addressed with the new 5 Hz-to-3 GHz vector network analyzer that offers convenient milliohm impedance measurements by eliminating the need for external magnetic cores or isolation transformers.

This paper first explains how the cable-braid loop creates an error floor in Two-port Shunt-through connections, and how it can be eliminated. We show how simple, but high quality calibration pieces can be created. We also introduce two different kinds of reference pieces, one which performs well, and one, which has significant errors. The reasons for the errors are described and modeled and the correct approach of creating the reference piece is explained.

The next sections cover MLCC measurements under various DC and AC bias conditions. We show that measuring MLCCs over a wide frequency range with the default impedance-bridge or VNA setups results in a largely varying AC voltage across the DUT as frequency varies and this may distort the measured capacitance value. We present setups and measurement results with constant AC voltage across the DUT. The next sections cover ferrite-bead and inductor measurements with DC bias current, including a new high-current PI circuit to measure inductors with up to 40A DC bias current.

The last sections cover DC-DC converter measurements stand-alone and in system boards. It is shown that the usual loop-stability measurements may be sensitive to the correct level setting. Full-system PDN measurement setup and results close the paper.

2 Frequency-Domain PDN Measurement Methods

Design validation of PDNs in the time domain is less practical, because the measured time-domain noise depends not only on the PDN we want to validate, but also on the (usually highly uncertain and unknown, and many times also non-linear) time-domain noise injection of the active circuitry on the PDN. The frequency-domain validation offers a straightforward path, because with a few exceptions, PDNs can be mostly treated as time-invariant and linear networks. Since a good PDN should provide stable voltage for the electronics, this means its impedance should be much lower than the impedance of the connected devices it feeds. This tells us that the primary validation output we are interested in is impedance, which can be computed as the open-terminated response voltage of the PDN to an injected test current. At low and mid frequencies, where the self-impedances of DUTs often reach sub-milliohm values, a fundamental challenge is the connection to the DUT. Unless we measure a single component in a well-constructed fixture, a single connection will introduce too much error in the milliohm range. The solution is to use the AC equivalent of the DC four-wire Kelvin measurement approach. This is illustrated in *Figure 1*.

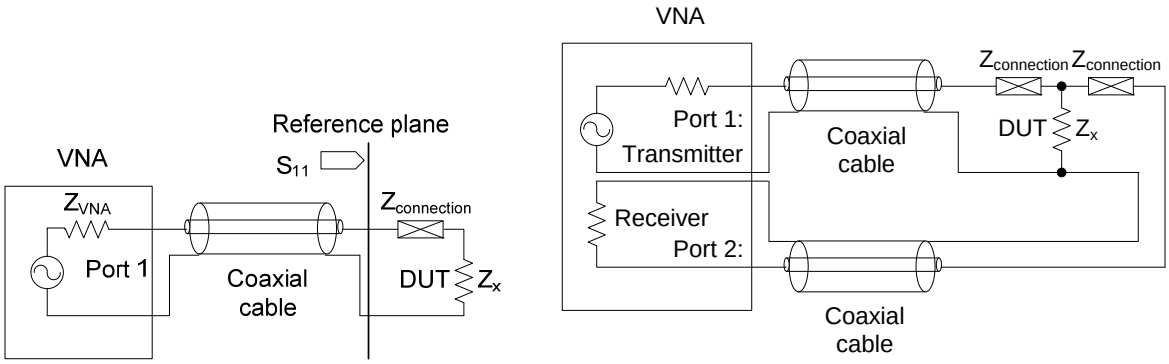


Figure 1: *Illustration of connection error with a single connection to the DUT (on the left), and block schematics of Two-port Shunt-through measurement on the right.*

The Shunt-through connection works well for very small impedances, but fails again for very high impedances. For very high impedances the DUT can be connected in series between the hot wires of the cables, thus creating a Two-port Series-through connection scheme. For the two setups, the DUT impedance can be resolved from the measured S_{21} parameter as follows:

$$Z_{DUT} = \frac{Z_{VNA}}{2}\frac{S_{21}}{1-S_{21}} \quad (1)$$

$$Z_{DUT} = 2Z_{VNA}\frac{1-S_{21}}{S_{21}} \quad (2)$$

where Z_{DUT} is the unknown complex impedance to be measured, Z_{VNA} is the reference impedance of VNA (50 Ohm) and S_{21} is the measured complex response by the VNA.

2.1 Handling the cable-braid loop error

The Two-port Shunt-through connection is a good fit for Vector Network Analyzers or Frequency Response Analyzers, which inherently have at least two ports, one being the source at any given time. However, by using two connections attached to the same DUT, now we just created a new problem: unless one or both ports are floating, the reference connections going to the two ports form a ground loop and we end up with a significant error floor. This is explained in *Figure 2*. We assume very low frequencies (or DC), so that we need to consider only resistances. The test current flowing through the DUT (for sake of simplicity, it is represented by a Short) created a V_e voltage drop across the parallel equivalent of the two cable-braid resistances: R_{b1} x R_{b2}. Instead of the expected zero, the reading at Port 2 will be this V_e voltage.

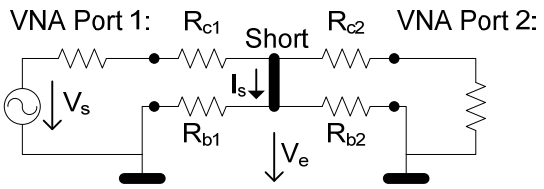


Figure 2: *Illustration of cable-braid loop error.*

This cable-braid error floor gradually diminishes as the inductive reactance of the cable opens up the loop. One possible remedy is to artificially increase the inductance by adding ferrite beads or threading the cable through a ferrite toroid so that we push the cable braid's corner frequency to below the lowest frequency we measure.

The E5061B LF-RF network analyzer takes different approach by semi-floating inputs at its Gain-Phase test port. The equivalent low-frequency impedance is approximately 30 Ohms and this reduces the cable-braid loop's error significantly. The concept is illustrated in *Figure 3*, and its results are shown in *Figure 4*.

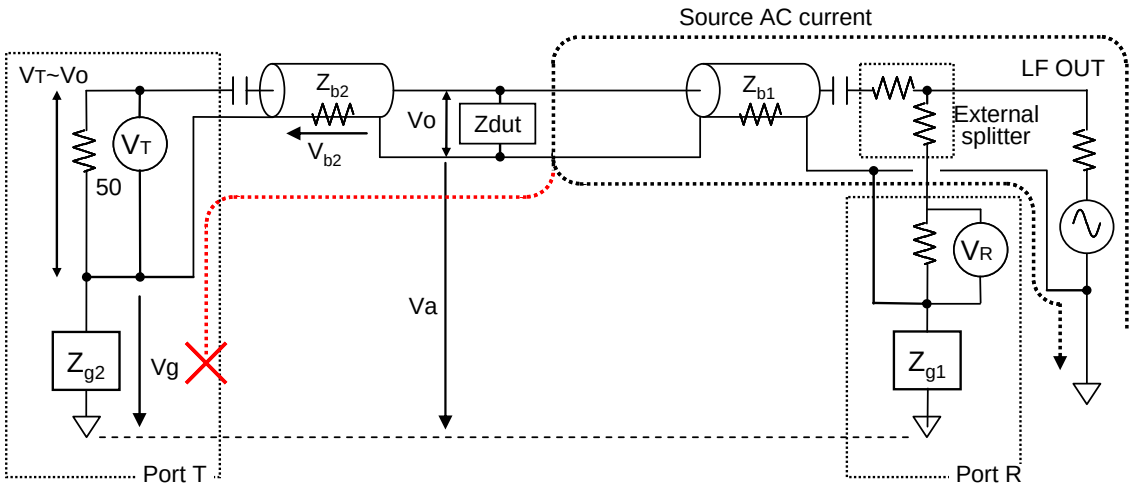


Figure 3*: Concept of semi-floating ground.*

Assuming that the Z_{DUT} impedance is much lower than 50 Ohms, the Va error voltage, created by the test current as it flows through the cable-braid impedances, is similar in magnitude to Ve in *Figure 2*. In contrast to *Figure 2*, however, the received V_T voltage will contain only an attenuated portion of the error voltage, V_{b2}. From the Va = Vg + V_{b2} vector triangle we can calculate the actual V_{b2} error voltage as

$$V_{b2} = V_a \frac{Z_{b2}}{Z_{g2} + Z_{b2}} \tag{3}$$

Since $Z_{g2} >> Z_{b2}$, the voltage at the T input is close to the correct value: $V_T \sim Vo$.

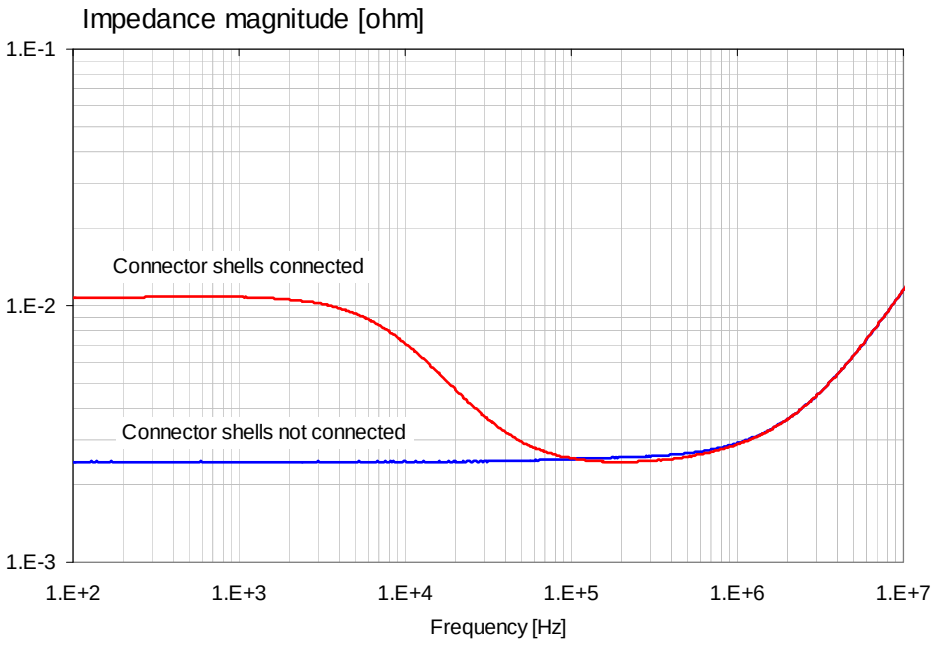


***Figure 4**: Illustration of effectiveness of semi-floating ground.*

Data for *Figure 4* was collected with the Gain-Phase test port, using an in-line style 2.5 mOhm reference piece, shown on the right of *Figure 7*. When the shells of the BNC connectors of T and LF Out are tied together temporarily with a heavy copper braid, we basically eliminate or bypass the semi-floating ground circuit. This way we can see what would be the instrument's reading with conventionally grounded connections. When the connector shells are not tied together, the low-frequency reading is flat at the correct 2.5 mOhm value. This shows the ability to accurately measure the milliohm impedances of DC-DC converters, without using magnetic cores to increase the inductance of cable braid.

2.2 Calibration process and reference pieces

Many PDN measurements require cables to connect to the DUT. Single components, like bypass capacitors and ferrites/inductors could be measured in fixtures directly attached to

the VNA, but even for single components often times the stackup and escape geometry of the user environment makes enough difference so that the part should be measured in an in-situ environment ([4], [5]). Power-converter modules, PDN subsystems or full systems most of the time require cabled connections.

Calibration options

At low frequencies, up to about 30 MHz, approximate measurements can be done without calibration. When more accurate data is required, a simple Response/Thru calibration is the quickest to perform. There is also a 1-Port through calibration option with the Gain-Phase setup. In all three options, the instrument can display directly the impedance by calling up the appropriate Analysis functions that perform *Equations (1)* and *(2)*. *Figure 5* explains the connections for the 1-Port through calibration.

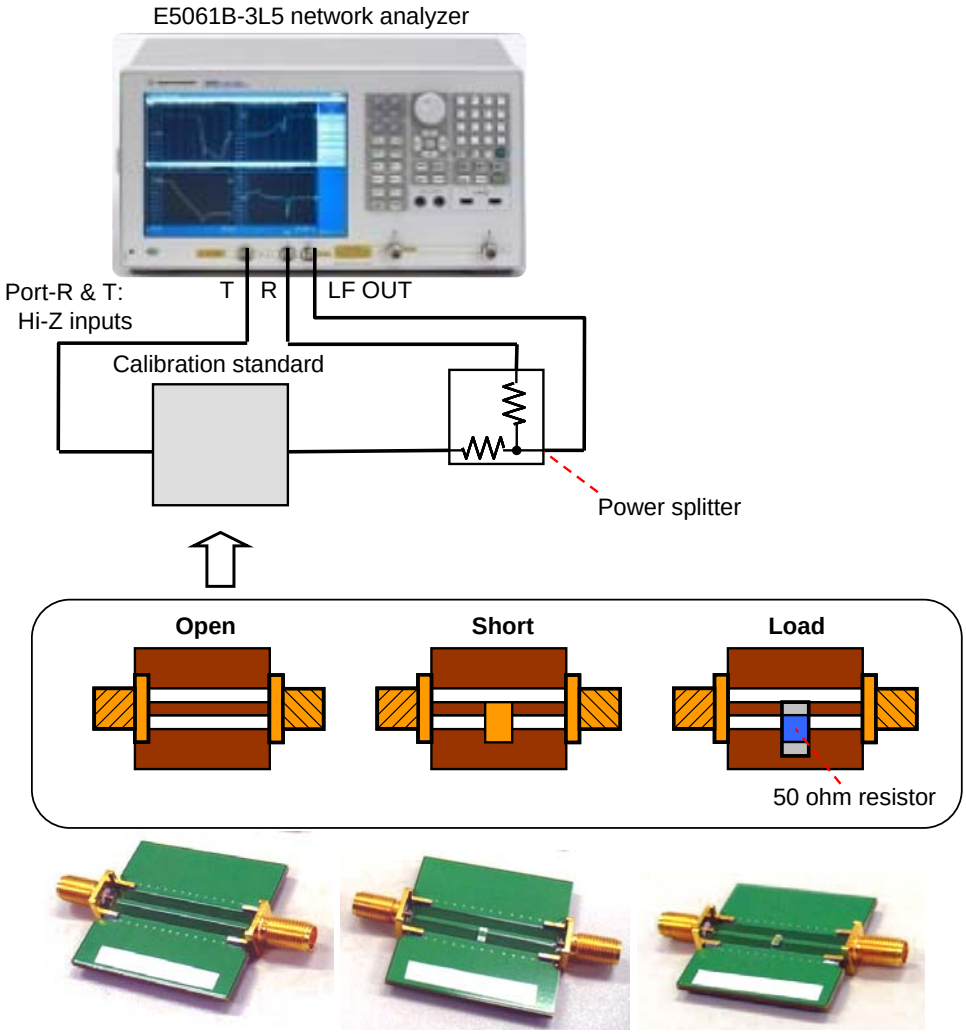


***Figure 5**: 3-term calibration with the E5061B-3L5 in Gain-Phase test port.*

The three calibration standards can be created, for instance, on small PCBs, as shown on the photos at the bottom of *Figure 5*. To eliminate the need for PCB fabrication, a pair of

back-to-back soldered PCB-mount female SMA connectors can also be used. *Figure 6* shows the photos of simple home-made calibration pieces made of SMA connectors. Note that the Open calibration piece for the 1-Port calibration is the same as the Thru piece for the Response/Thru calibration.

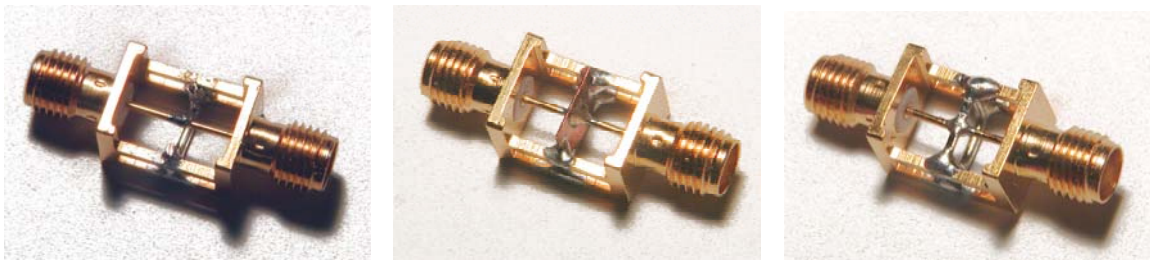


Figure 6: *Left to right: home-made OPEN, SHORT and LOAD calibration standards for 1-Port 3-term calibration.*

Reference pieces

In traditional VNA measurements, traceable coaxial standards and reference pieces do exist. For low-impedance PDN measurements, however, there is no reference piece commercially available for the user that would enable the checking of the setup for accuracy. Similar to the home-made calibration standards, low-impedance home-made reference pieces can also be constructed. If we take an OPEN calibration standard and mount to it a known small impedance in the shunt path, we get a reference piece that can be used either between the SMA connectors, or at low frequencies it can be directly measured with semirigid home-made probes (for construction, see [3]) across the shunt piece. The reference piece can be a short wire that we adjust to the required value with a 4-wire DC micro-ohm meter, or precision current-sensing resistors can also be used without the need for further trimming. *Figure 7* shows two home-made devices; two different constructions of a 2.5 milliohm reference pieces made of four ten-milliohm +-1% current-sense resistors.

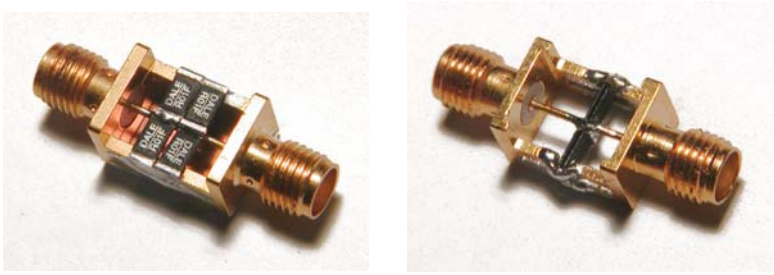


Figure 7*: Home-made low-impedance reference pieces. 2.5-mOhm tile-style (on the left), and 2.5-mOhm in-line style (on the right).*

We can gain useful insights into the proper construction of reference pieces if we measure these two pieces. *Figure 8* shows the impedance magnitude and phase plots for these two devices after performing a Response/Thru calibration in Gain-Phase setup.

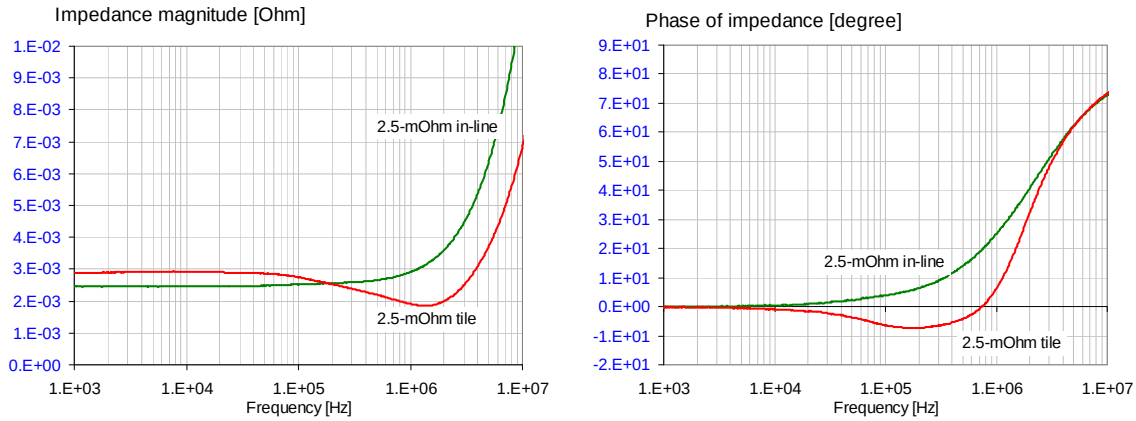


Figure 8: *Measured impedance profiles of the two reference pieces shown in Figure 7.*

The low-frequency impedance of the in-line construction is as expected: very close to the required 2.5 mOhms. Its inductance is around 300 pH at 10 kHz. The tile construction, however, shows unexpected behavior in two respects: the low-frequency impedance value is 2.9 mOhm instead of 2.5 mOhm and the impedance profile has a dip slightly above 1 MHz and the dip comes with negative phase. If we calculate the equivalent inductance from the imaginary part of the impedance, we get negative inductance: -600 pH at 10 kHz. This is clearly not the impedance profile we wanted to create.

To understand this behavior and how to correct and avoid it, we need to look at the current path and the dimensions of the construction. The photo on the left of *Figure 9* shows the reference piece from the top. The OPEN calibration piece, which forms the basis of the reference piece, has 0.4" distance between the SMA face-plates. Half of this distance, 0.2", is covered by the resistors side by side, connecting the center pins to the ground frame.

If we TDR the OPEN calibration piece, we can measure the Zo characteristic impedance and Tpd propagation delay through the open pins. The loop inductance along the 0.4" path can be calculated as Zo*Tpd. If we ignore the capacitance and resistance of the lines, and represent each slice of two paralleled resistors by three R-L legs, we arrive to the simplified equivalent circuit on the right of *Figure 9*. The equivalent circuit helps to understand what went wrong: instead of a Two-port Shunt-through connection, we now have a distributed R-L ladder network: at higher frequencies the series inductances of the pins gradually isolate the input and output connections and more current closes through the shunt leg closer to the source. This is a typical skin-effect phenomenon; we just created it around discrete circuits at low frequencies. This simple model does not account for the finite resistances of the center pin and frame (which raises the low-frequency resistance of the tile-style reference piece), but we can still get a reasonably good correlation between the model and the measured values, as shown on the bottom of *Figure 9*. The in-line style reference pieces do not exhibit this problem, because their connection along the frame is more point-like and the vertical position of the resistors limit how much the size of the current loop can change with frequency.

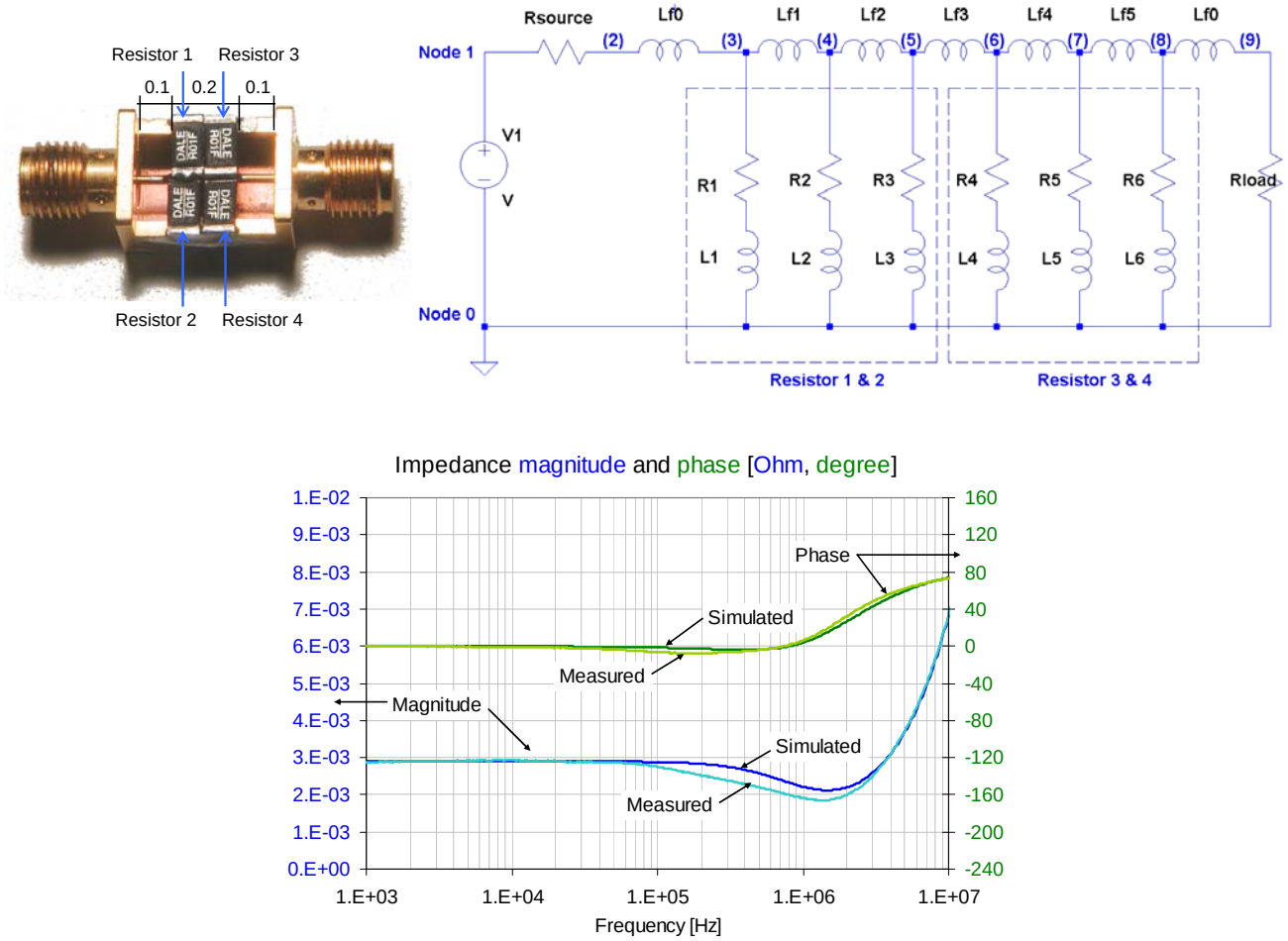


***Figure 9**: Top view of the tile-style reference piece with dimensions shown in inches (on the top left) and equivalent circuit (on the top right). Model correlation is shown on the bottom.*

2.3 Evaluating bypass capacitors with DC voltage bias

Large-capacitance MLCCs are widely used as bypass capacitors due to their small size and good cost/performance ratio. However, their capacitance values may be strongly dependent on the DC voltage, and therefore it is important to evaluate them by applying the appropriate DC voltage bias.

Shunt-thru method with high-impedance inputs

Figure 10 illustrates a proposed new shunt-thru method for DC voltage-biased MLCC measurement. The difference from the conventional shunt-thru method is that the VNA receives the AC signals with the high-impedance inputs. Since the DC current does not

flow into the receivers, we can apply DC bias voltages to the DUT. The AC voltage across the DUT is measured with the receiver VT, and the AC current flowing through the DUT is measured by sensing the AC voltage across the resistor Rc with two receivers VR and VT. This measurement method gives good measurement sensitivity in the small impedance range below Rc. Unlike the conventional shunt-thru method with the 50 ohm system impedance, the 3-term calibration (OPEN/SHORT/LOAD calibration) at the measurement terminal is essential to adjust the measurement system so that we can perform accurate impedance measurements. As we do the 3-term calibration, it is not necessary to accurately know the actual value of Rc, because the LOAD calibration will establish the proper reference values.

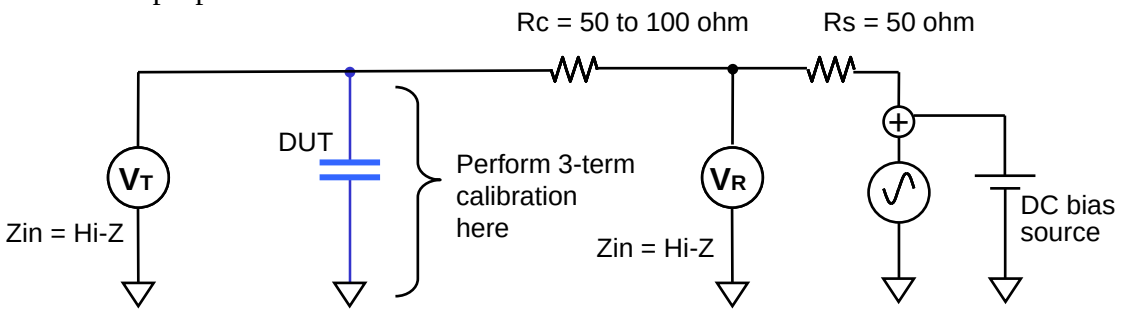


Figure 10: *Modified shunt-thru method for DC voltage biased MLCC measurements.*

Figure 11 shows a configuration example with the E5061B-3L5 LF-RF network analyzer. The DC voltage bias is provided from the analyzer's built-in DC bias source.

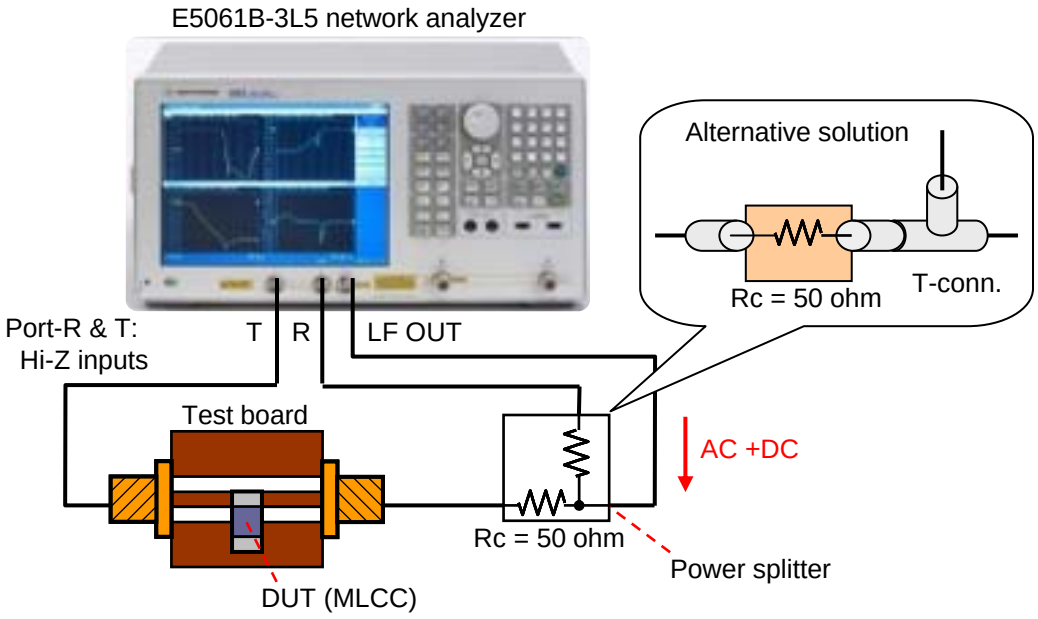


Figure 11: *Configuration example with E5061B-3L5 network analyzer. The same calibration standards can be used as shown in Figure 5.*

The receiver ports R and T are set to the high-impedance input mode. In this example, one of the 50 ohm resistors in the power splitter is utilized as the current sensing resistor Rs. Strictly speaking, the other 50 ohm resistor of the power splitter is not necessary in this configuration. Or, we can substitute this with the combination of a single resistor and a T-connector, as shown in the figure insert. The 3-term calibration in the impedance domain can be performed by setting the analyzer to the reflection-to-impedance conversion mode and performing the 1-port full calibration. The calibration standards in this example are the home-made OPEN, SHORT and 50 ohm LOAD devices, which have the same geometry as the shunt-thru test board for the DUT. To accurately measure up to the DUT's inductive region over the self resonant frequency, it is necessary to define the inductance of the short device in the analyzer's calibration kit definition menu.

Example of MLCC measurement with DC voltage bias

A MLCC with nominal capacitance of 100 uF was measured with the configuration shown in *Figure 11*. The measurement frequency range was 100 Hz to 10 MHz.

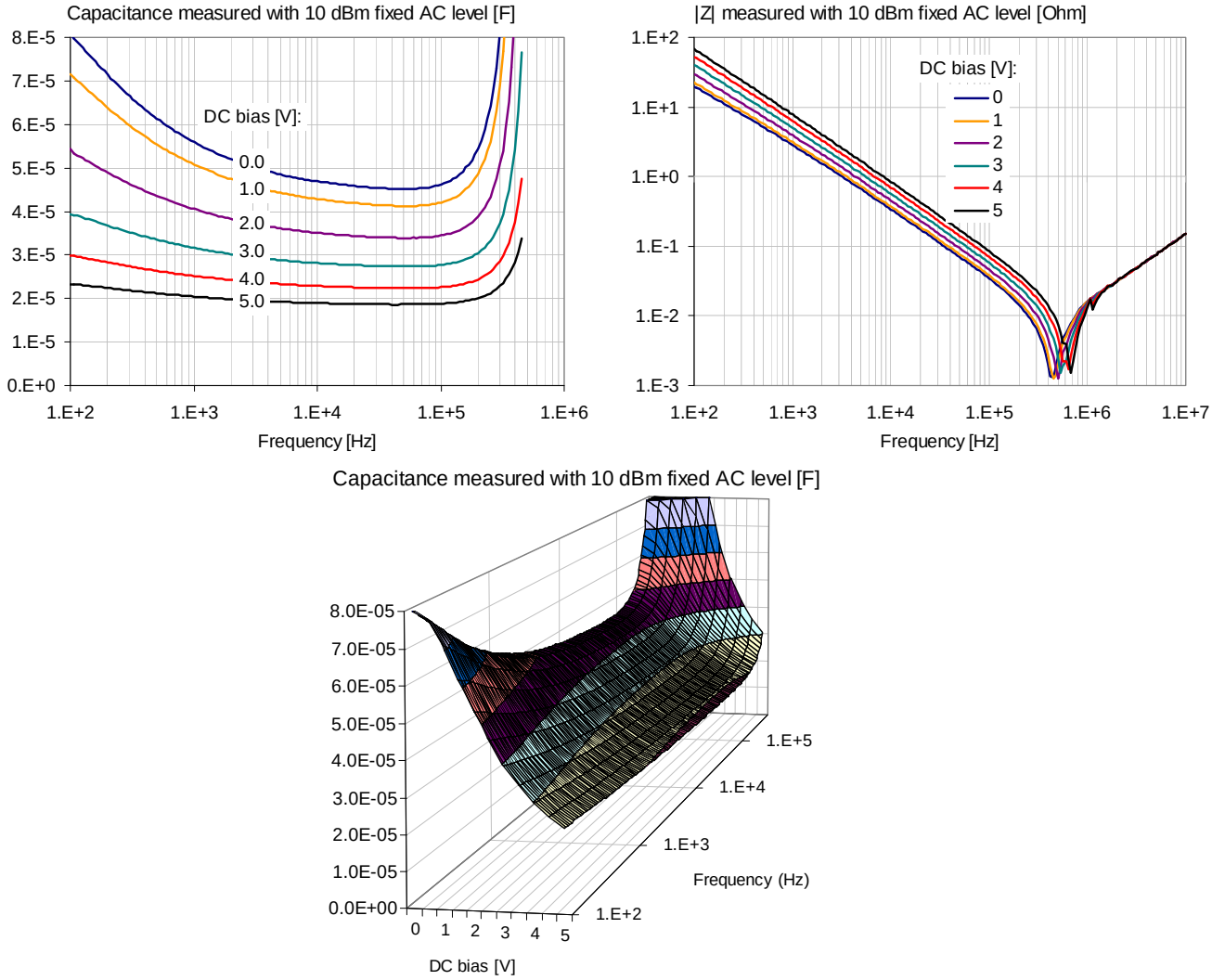


Figure 12: *DC bias dependence of large-capacitance MLCC (DC bias = 0 to 5 Vdc, Source level = 10 dBm).*

The analyzer's source level was 10 dBm. *Figure12* shows the capacitance and |Z| measurement results with the DC bias voltages of 0 to 5 Vdc. As can be seen, the DC voltage bias dependence at the low-frequency capacitive area is successfully measured, while not spoiling the measurement sensitivity in the milliohm impedance range around the self resonant frequency. Note that the nominal value of large-capacitance MLCCs provided from capacitor vendors is traditionally tested at 120 Hz by applying a very high AC level of 0.5Vrms or 1 Vrms across the DUT, without a DC voltage bias. The actual capacitance values at higher frequencies and lower AC levels are much lower than this nominal value, as indicated with the measurement result of *Figure 12*.

2. 4 Evaluating bypass capacitors with constant AC signal level

The highest-density MLCCs also have an AC signal level dependence. In the large-capacitance MLCC measurements described in the previous section, the AC signal level actually applied to the DUT was not constant because the DUT's impedance |Z|=1/(2*PI*f*C) decreases along with increasing frequency toward the self resonant area. The analyzer's fixed source output level is divided by the DUT's impedance and the series impedance of the measurement system (the analyzer's source output impedance: 50 ohm, plus the current sensing resistor Rc). In the measurement examples of *Figure 12*, a relatively high AC voltage of hundreds of millivolts is applied to the DUT around the start frequency, and the AC voltage is decreased down to millivolts or less as the frequency gets closer to the self resonant frequency. In a real application, however, when the capacitor is used to bypass a low-noise supply rail, the AC voltage across the capacitor is in the millivolt order. To evaluate the MLCCs under more realistic AC-level condition, it is desired to uniformly apply the selected level of AC voltage to the DUT as much as possible in the entire test frequency range.

Example solution for applying constant AC signal level

Here we propose a practical solution for applying the constant AC signal level to the DUT in the frequency-swept shunt-impedance measurement. The solution we tried is a straightforward method by using the VNA's segment sweep function. The overview of the measurement procedure is as follows:

Pre-measurement:

1) Connect the DUT in the shunt-thru connection, as shown in *Figure 13*.
2) Set the source power level of each segment to the target power level (Ptgt) to be applied to the DUT.
3) Measure the power level across the DUT with the VNA's absolute measurement function (not the ratio measurement).
4) Re-set the source power level of each segment to
   Original level + (Ptgt – Pdut)
5) Repeat the step-3 and 4 a few times to create the segment sweep table for applying the constant AC voltage across the DUT.

The above procedure can be automated with the VNA's built-in programming function, based on the blocks of tasks shown in *Figure 14*. After this pre-measurement is completed, now we are ready to start the calibration and measurement.

Measurement:
6) Perform the 3-term calibration.
7) Connect the DUT and measure the impedance.

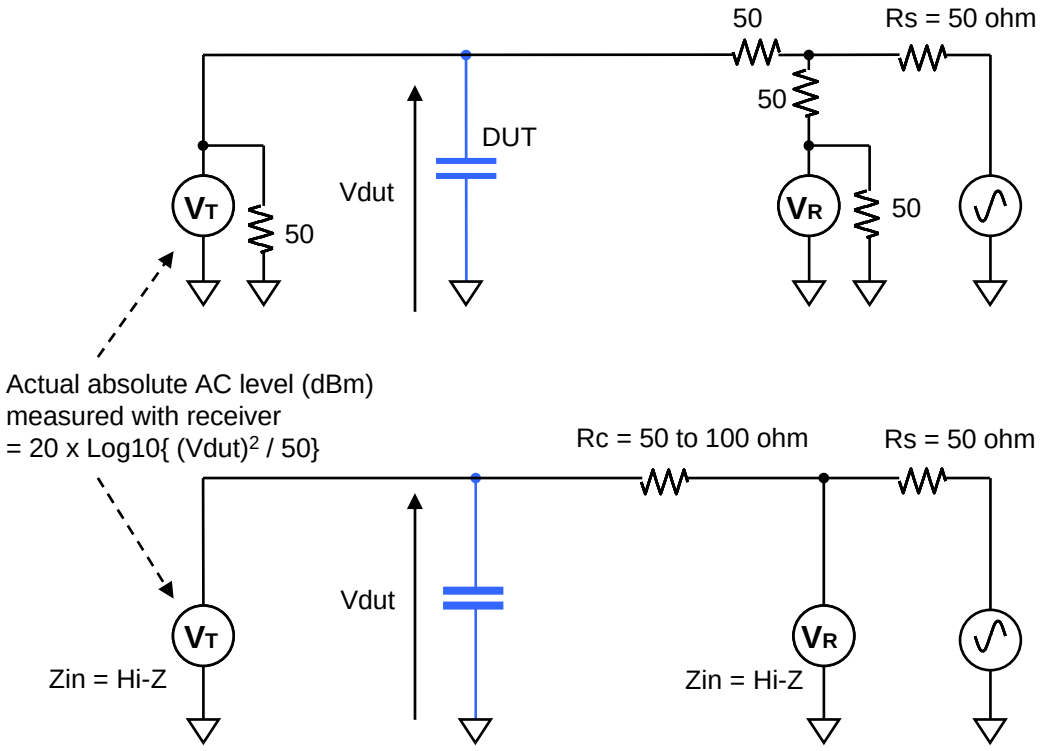


Figure 13: *Monitoring AC level across DUT*
(possible in both 50 ohm shunt-thru method and modified shunt-thru method).

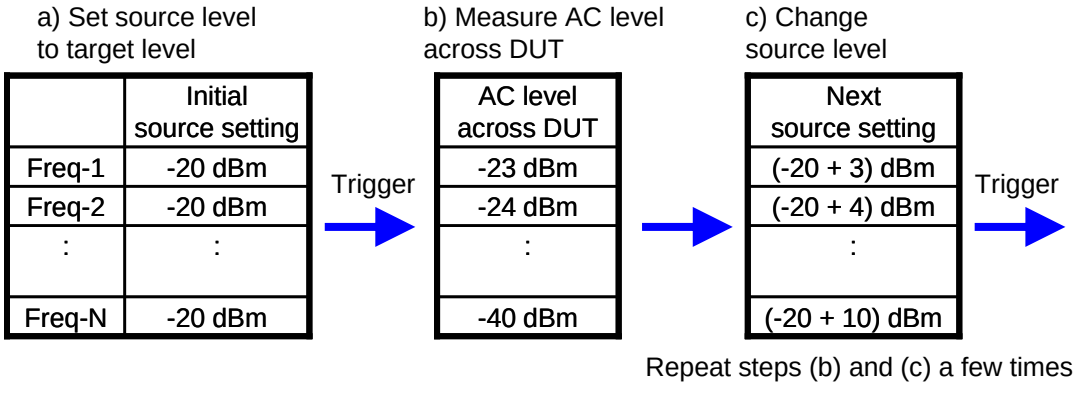
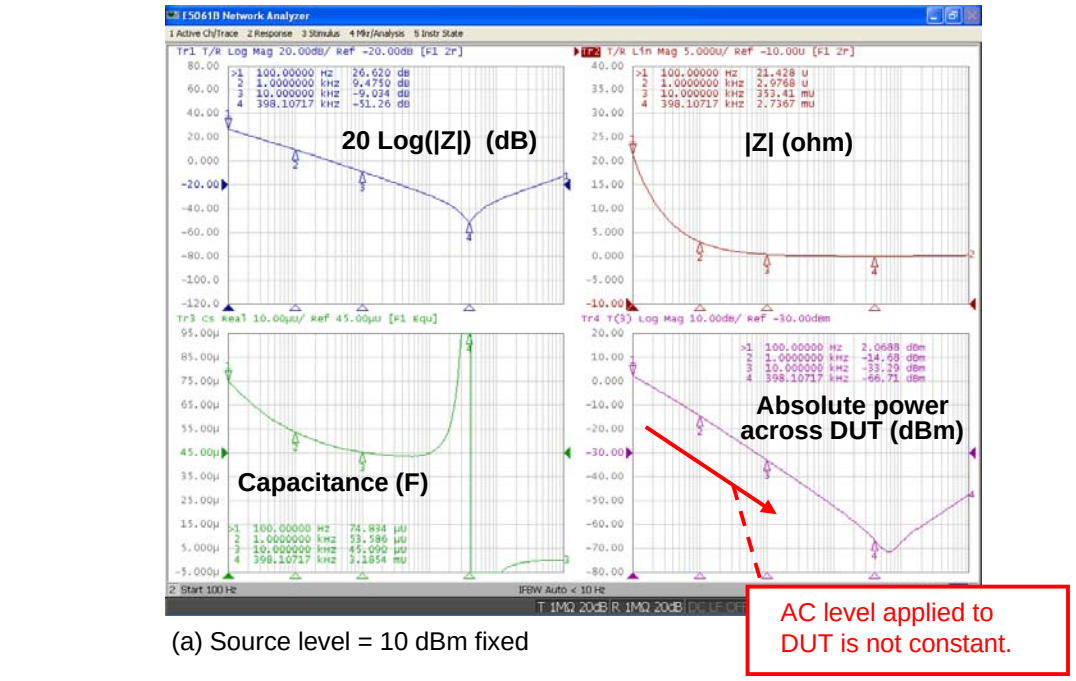


Figure 14: *Making sweep table applying constant AC-level to DUT*
(Example of target level = -20 dBm).

Example of MLCC measurement with constant AC level

The MLCC with the nominal capacitance of 100 uF was measured by applying a constant AC signal level across the DUT with the configuration shown in *Figure 13*. The target AC level to be applied to the DUT is 5 mVrms (= -33 dBm with the VNA's absolute reading referenced to its system impedance 50 ohm).



(a) Source level = 10 dBm fixed

(b) Applying constant AC level (5 mVrms at DUT)

Figure 15: *Screen shots of (a) normal fixed-source measurement method and (b) constant AC-level method.*

The segment sweep table was created by automating the pre-measurement sequence with the E5061B's built-in VBA programming function. *Figure 15* shows screen shots that exhibit the effect of applying the constant AC level. As we can see in the absolute power measurement trace, the AC level of -33 dBm is uniformly applied to the DUT with the constant AC-level solution shown below, in contrast to the normal measurement method with the fixed source level. In the case of this DUT, the constant AC level of 5 mVrms can be applied just up to 10 kHz or so, because of the limitation of the VNA's maximum source output level (up to 10 dBm in the E5061B-3L5). But it sufficiently covers the low-frequency area where the DUT exhibit a strong AC level dependence.

Figure 16 compares the capacitance and |Z| measurement results by using the ordinary measurement method with a fixed source level and the new constant AC-level solution. As can be seen, the capacitance in the low frequency range is more straight when the constant AC voltage of 5 mVrms is applied.

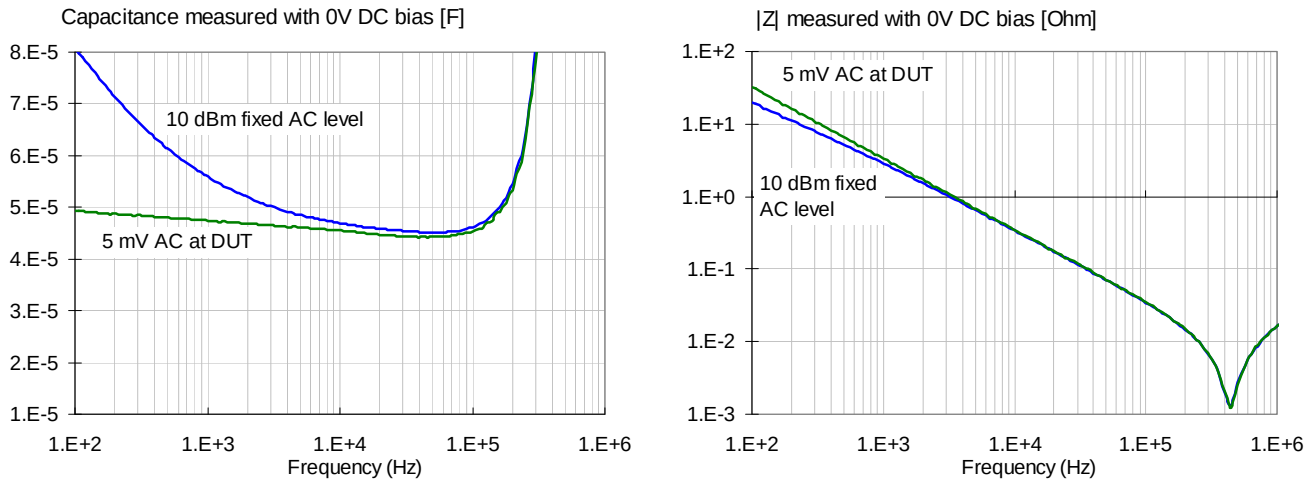


Figure 16: *MLCC measurement results with normal measurement method (10 dBm fixed source at VNA) and constant AC-level method (5 mVrms constant level at DUT).*

2. 5 Example of MLCC measurement with constant AC level and DC bias

Of course, it is also possible to apply a DC voltage bias in the constant AC-level measurement. *Figure 17* shows the measurement results when applying the DC bias of 0 to 5 Vdc in the measurement with the constant AC level of 5 mVrms at the DUT. At each bias level, the capacitance in the low frequency range is more flat than the measurement with the fixed source level that was shown in *Figure 12*.

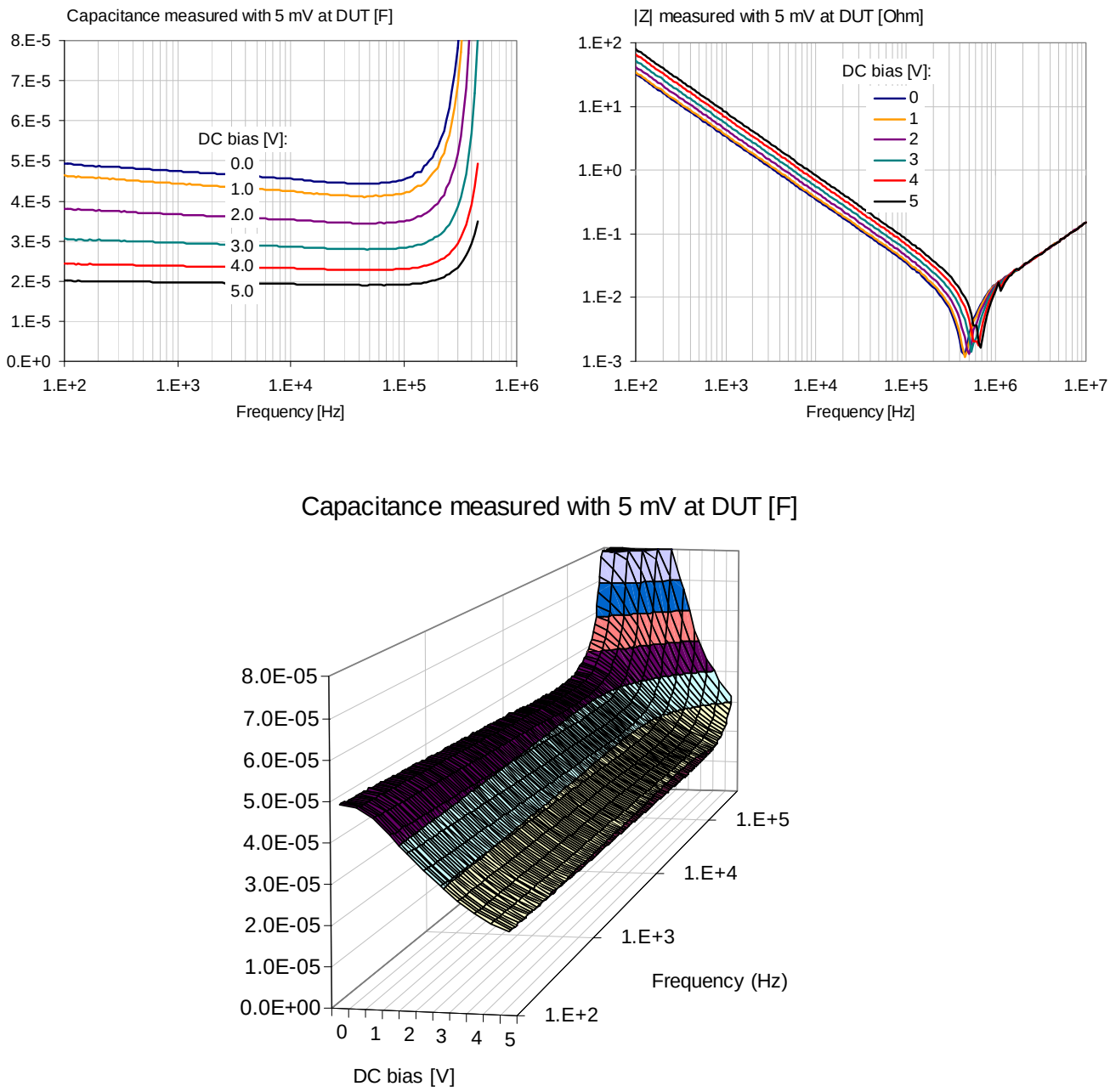


Figure 17: *MLCC measurement results by applying constant AC level and DC bias (AC level at DUT= 5 mV rms, DC bias = 0 to 5 Vdc).*

2. 6 Applying higher constant AC level

If the targeted constant AC level is higher than 5 mVrms, the impedance range where we can apply constant AC level will be narrower due to the limitation of the VNA's maximum source output level. A practical solution for this is to use an external 4-quadrature power amplifier to boost the source level so that the higher AC voltages can be applied to the smaller impedance of the DUT. *Figure 18* shows a configuration

example and a measurement result of applying the constant AC level of 10 mVrms to the MLCC, which is the same one as that of the previous measurement example. As shown in the screen shot, thanks to the source level enhancement with the amplifier, the constant AC level of 10 mVrms is applied to the DUT up to about 26 kHz, which is close to the self resonant area. In this measurement configuration, note that the sweep mode must be switched to the normal logarithmic sweep with a smaller source level only when performing the calibration, not to overload the receiver port T when connecting the open (=thru) device and not to burn the load device in the frequency range where the sweep segment outputs the high source level.

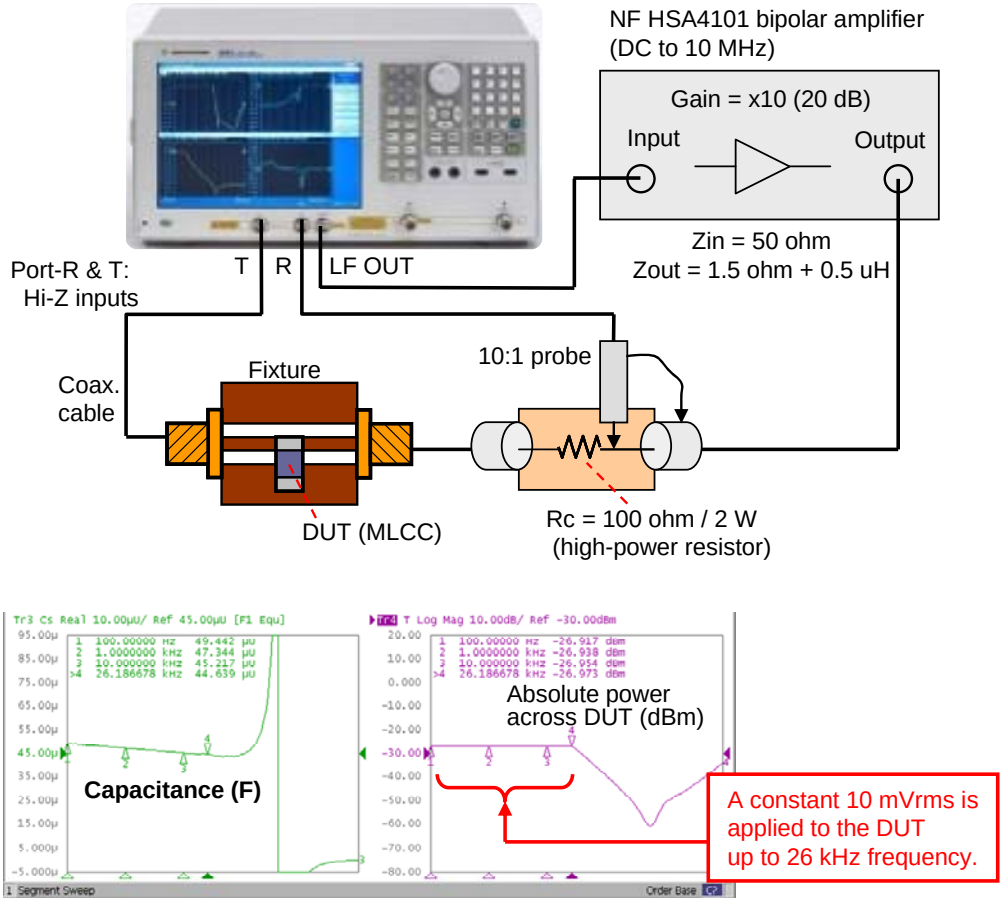


Figure 18: *Applying higher constant-AC level by using external power amplifier.*

2.7 Evaluating inductors with DC current bias

Another key passive component in PDNs is the inductor or ferrite bead. They are used for PDN decoupling, and power inductors are used in the DC-DC converter's output filters together with the bypass capacitors. Since these inductive components have DC current bias dependence, it is preferable to evaluate their impedance parameters by applying a large DC current bias similar to the actual PDN conditions.

1-port measurement method (1 MHz to 1 GHz, up to 5 Adc)
If the DC current bias to be applied is not so high, the 1-port reflection measurement method using the external bias tee is the most practical solution. The 16200B DC bias adapter (1 MHz to 1 GHz, up to 5 Adc) originally designed for 1-port impedance analyzers can also be used with the VNAs. *Figure 19* shows a configuration example and a measurement example of a ferrite bead. We can observe that the impedance of the ferrite bead is significantly decreased by the DC current, which means its decoupling effect will be lower under the large DC current condition.

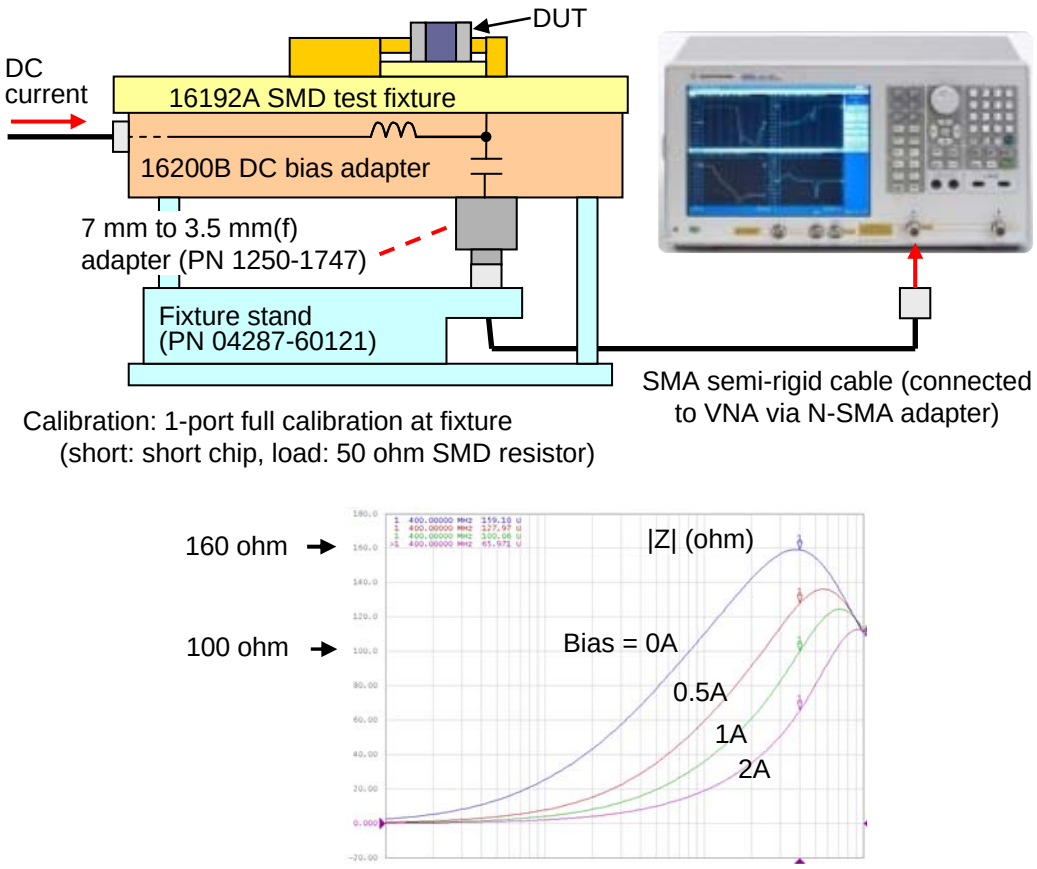


Figure 19: *DC current biased measurement configuration (up to 5 Adc) and measurement example of a ferrite bead.*

PI-network method for high-current power inductors (1 MHz to 100 MHz)
The solution described in *Figure 19* can cover DC-biased measurement needs of most of ferrite beads and low-current power inductors. On the other hand, when designing high-current DC-DC converters, we need to verify that the power inductors are not saturated with higher DC currents, sometimes up to several tens of amperes. However, it is difficult to find an off-the-shelf bias tee that can handle more than 5 Adc in the frequency range below 100 MHz.

Here we consider a quite different approach. In this solution, a PI-network is configured with a DUT and two choke coils as shown in *Figure 20*, and the full S-parameters of the entire PI-network are measured with the VNA by applying the DC bias current from the DC current source. The DUT's impedance Z_{DUT} is extracted from the measured S-parameters with the following formula:

$$Z_{DUT} = \frac{1}{Y_{DUT}} = 50\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \tag{4}$$

Because the VNA measures the entire PI-network that consists of Y1, Y2 and Y_{DUT}, and Y_{DUT} is extracted at each DC current level, the impedance variation of the choke coils due to the DC current basically does not affect on the DUT measurement. Thus, the DUT's impedance can be correctly measured regardless of the impedance variations of the choke coils. Similarly to the series-thru method, the PI-network method gives a good measurement sensitivity if the impedances of the DUT and the choke coils (|Z|=2*pi*f*L) are greater than several ohms. If the DUT satisfies this criterion, we can use the same inductors as the choke coils.

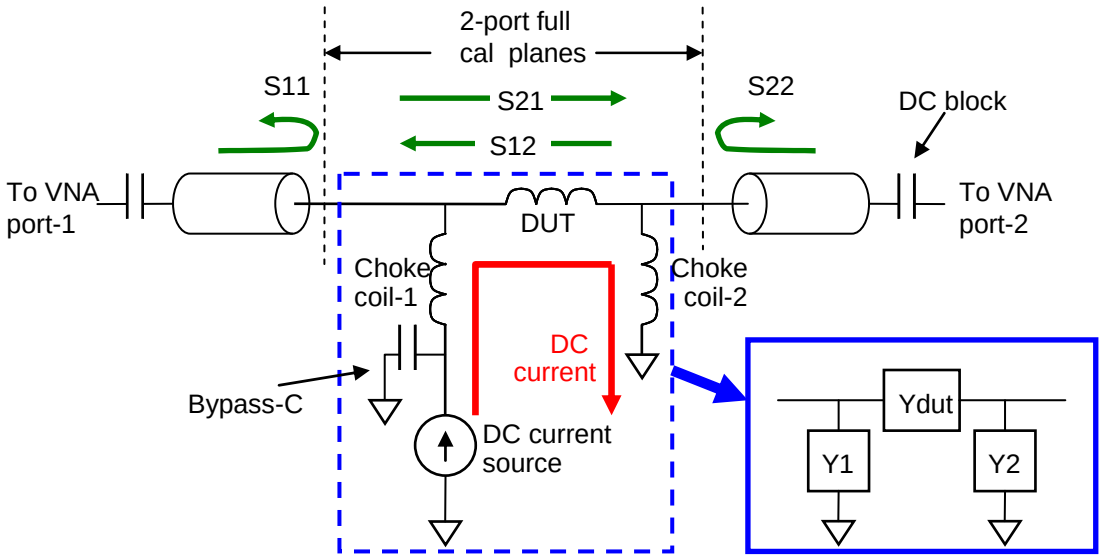


Figure 20: *PI-network method.*

According to our experiments, by comparing the measurement results with the 1-port measurement method (under no DC bias condition), the measurement results of both methods were correlated within 5% for the inductors of hundreds of nH to 1 uH ranges. It is practically good enough for verifying the inductance saturation of high-current power inductors. If the DUT's inductance is lower than 100 nH, the measurement error of the PI-network method would be larger.

Figure 21 shows a configuration example of the fixture for implementing the PI-network method. The DUT is directly soldered to SMA receptacles. The choke coils are connected to the DUT via wire leads. The wire length should not be very short to avoid the mutual

coupling between the DUT and the chokes. One or a few centimeters would be reasonable. To define the calibration plane at the end of the SMA receptacle, the 2-port full calibration should be performed by using home-made open/short/load/thru devices made with the same SMA receptacle.

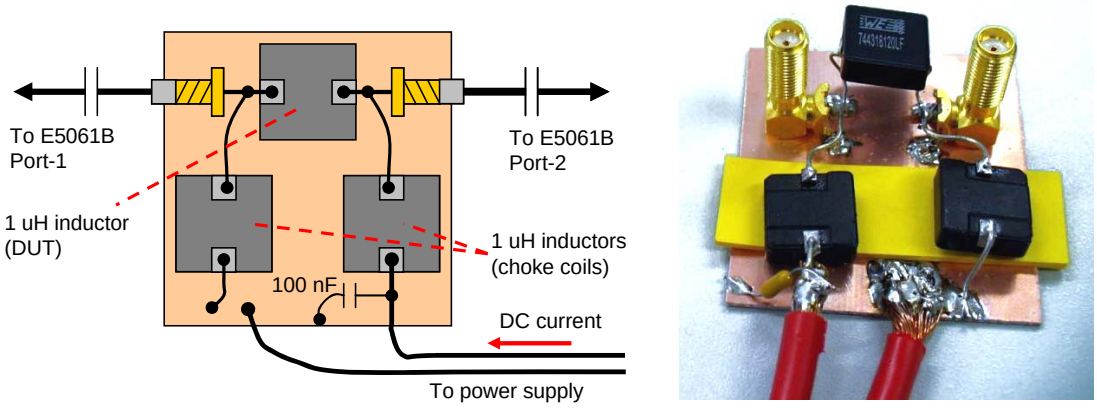


Figure 21: *Fixture configuration example: sketch on the left, photo on the right.*

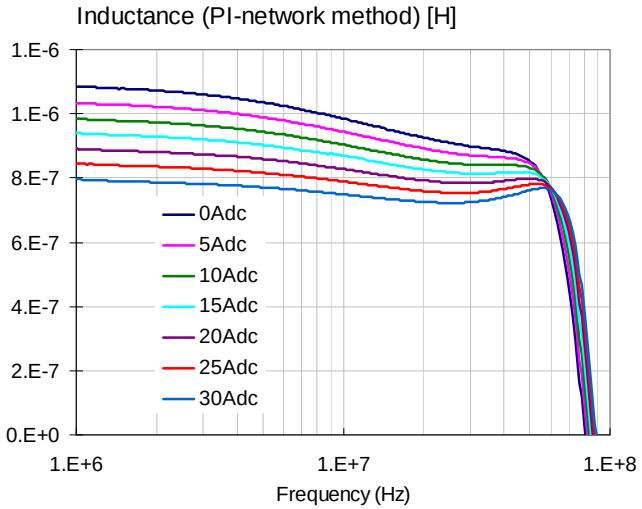


Figure 22: *1 uH power inductor measurement example (Freq. = 1 MHz to 100 MHz, DC bias = 0 to 30 Adc).*

Figure 22 shows a measurement example of the 1 uH power inductor by using this fixture configuration. The test frequency range is 1 MHz to 100 MHz, and the DC bias is up to 30 Adc. The inductance saturation with large DC currents is clearly visible.

2.8 DC-DC converter measurement

Power converters usually require two types of frequency-domain testing: gain-phase stability plots and/or small-signal output impedance plots. These measurements are usually interesting below the fundamental switching frequency of the converter, and

therefore simple Frequency Response Analyzers (FRA) can also be used for this purpose. Directly evaluating the loop phase margin sometimes gives us more insights for improving the transient performance, not just looking at the output impedance peak. *Figure 23* shows the block schematics and connection. We inject the test signal through an isolation transformer in series to the voltage feedback path, where a low-impedance point (converter output) connects to a high-impedance point (error-amplifier input) so that the impact of the series impedance of the injecting circuit on the transfer function can be neglected. *Figure 24* shows the photo of a similar setup with a Venable 3120 FRA (on the left) and the loop gain of a 15A 1V output DC-DC converter evaluation module measured with the 3120 FRA versus the E5061B analyzer. The T1 injection transformer for both cases was a Venable 200-003 injector module.

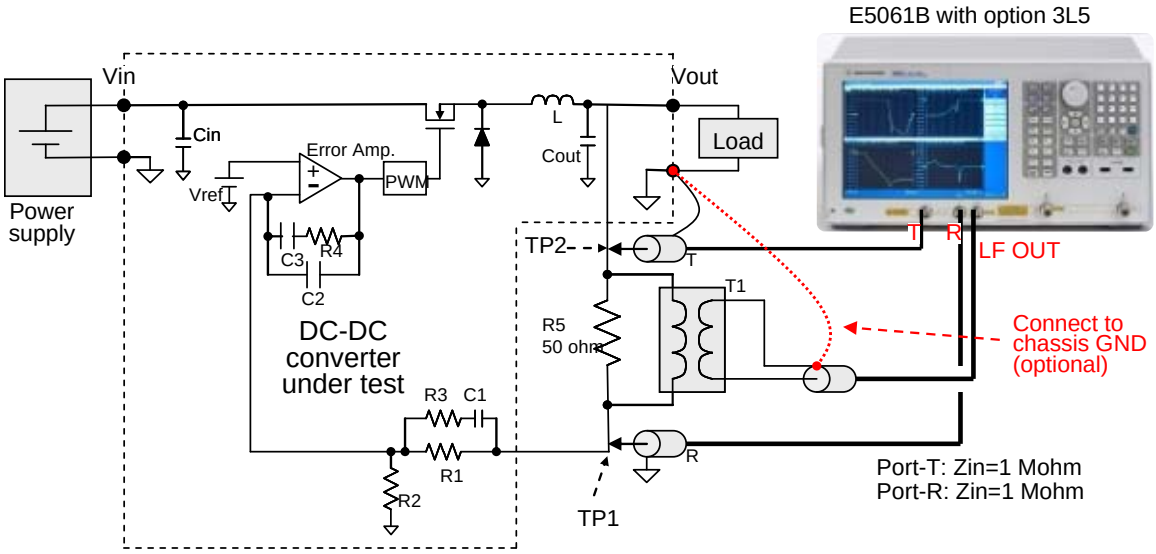


Figure 23: *Setup for measuring the Gain-Phase stability of a DC-DC converter with E5061B.*

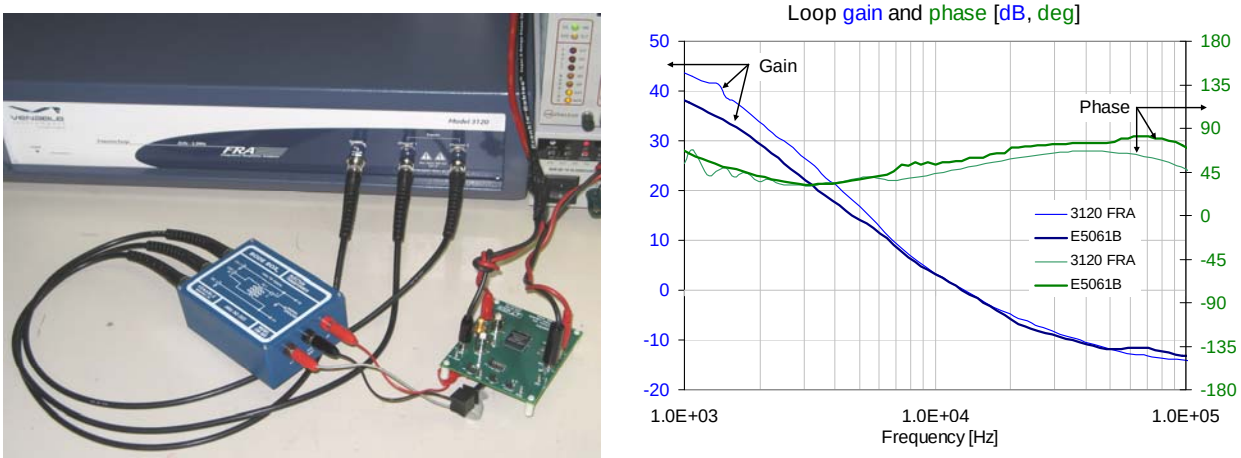


Figure 24*: Gain-phase measurement setup photo with Venable model 3120 FRA on the left, and comparison of gain amplitude and phase measured with E5061B versus 3120 on the right.*

Figure 24 shows the setup photo with the FRA and injector box and the comparison of data obtained with the two instrumentations. There are small differences between the results of the two setups because of the different output impedances and the source levels.

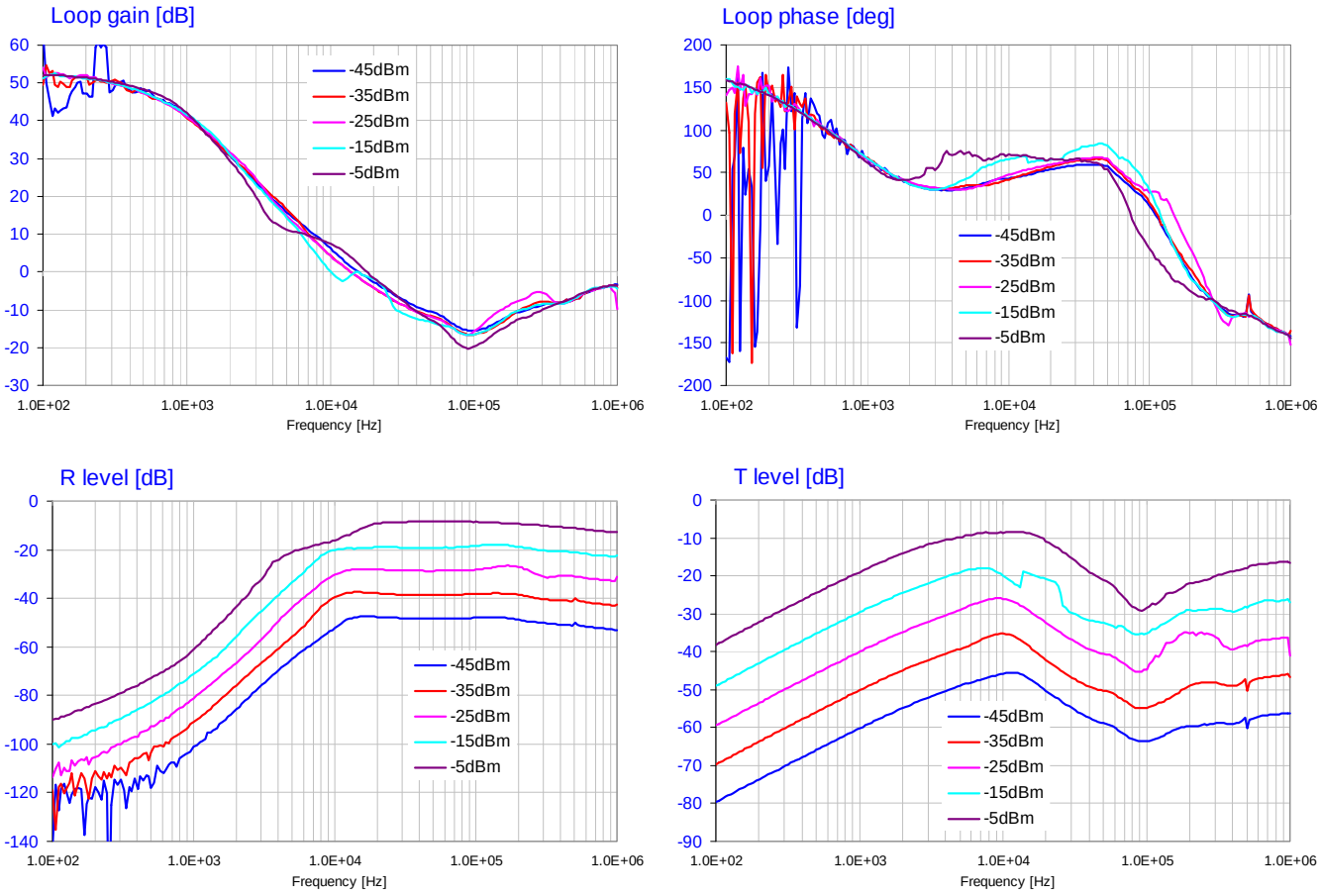


Figure 25: Gain-phase test measurement results with different source levels. The R and T levels refer to levels at TP1 and TP2 in Figure 23.

These differences are further explained in *Figure 25*. First, we can notice on the magnitude and phase plots of the loop gain that with -45dBm and -35dBm source levels there is considerable noise below 1 kHz frequency. The ultimate reason for this is that the measured R level is below the noise floor of the instrument. This happens because at low frequencies the large gain results in very small signal on the input side. Also, the injector transformer's finite bandwidth attenuates the injected level further at low frequencies. However, as we increase the source level, problems show up at higher frequencies: the traces with -15dBm and -5dBm source level get distorted. Most noticeable is the distortion on the measured T signal with -15dBm source level: there is a step-like change between 12 and 25 kHz. This was due to spurious locking of the converter's switching frequency to the harmonic of the injected signal.

When we look at the time-domain signals at the output of the error amplifier (that is where we can expect the largest swing of error voltage), we can follow how the injected test signal varies in magnitude as the frequency varies, eventually driving the error amplifier into saturation in certain frequency ranges when the source level is high. Similar to *Figure 14*, we can apply a sweep table here, too, to avoid the saturation of the error amplifier.

Active sources with very low DC voltage can be measured with the setup that we otherwise would use for low-impedance passive PDN components, for instance the one shown in *Figure 11*. The 1V output of the 15-A DC-DC converter evaluation module from *Figure 24* was measured in a similar setup with input power ON and OFF. *Figure 26* shows the results. Note that the active feedback loop pushes the output impedance to 0.3 milliohm impedance at low frequencies. We know from *Figure 25* that the unity-gain crossover frequency of the control loop is at 15 kHz, and that is the frequency where the unpowered and powered impedance magnitude traces join each other. Even though the active loop modifies the output impedance up to 300 kHz, the effect of the loop is diminishing above the crossover frequency.

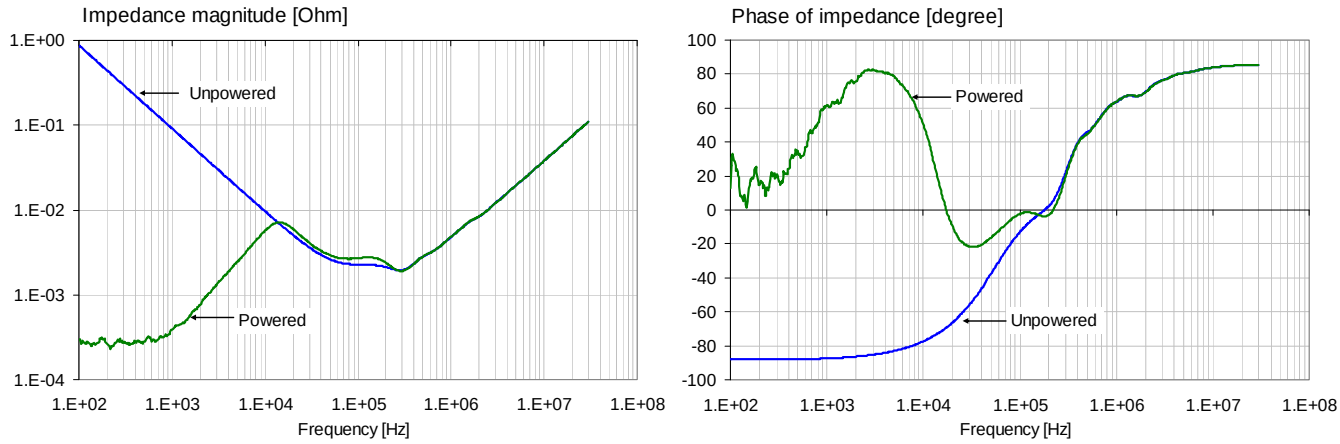


***Figure 26**: Output impedance magnitude (on the left) and phase (on the right) of a 15-A 1V DC-DC converter.*

3 System-level measurements

If we do not need to go below a kHz and can use a ferrite core around one of the connecting cables, we can use the S-parameter side of the E5061B VNA and we can measure the PDN impedance on an unpowered or powered system board with a single connection/setup up to 3 GHz. If we need to measure very low frequency response, the Gain-Phase test port of the instrument can be used in the 5 Hz – 30 MHz frequency range. *Figure 27* shows two such setup photos.

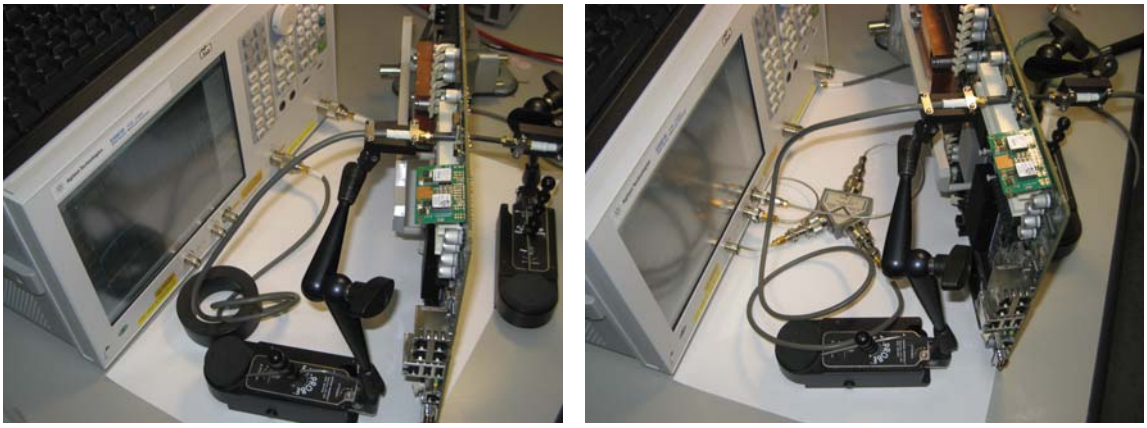


Figure 27: *Measurement setup of a live system board with the S-parameter test port (on the left) and Gain-Phase test port (on the right) of the E5061B VNA.*

Figure 28 shows the impedance magnitude measured on a 1V 100A rail on the system board under four different conditions. All four data sets were collected with the S-parameter test port of the E5061B VNA.

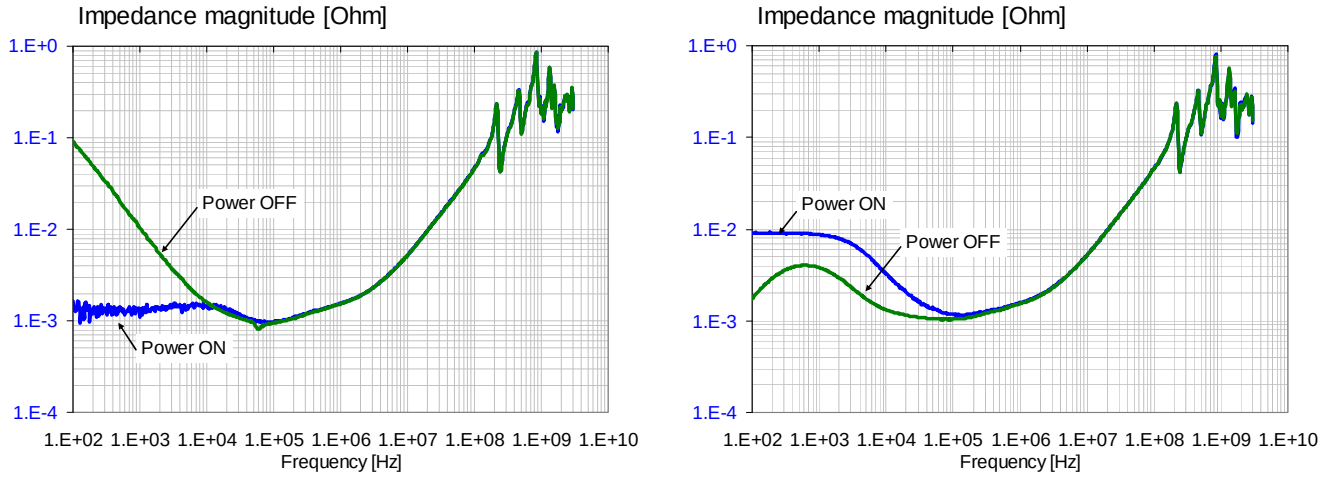


Figure 28: *System-board measurement results in the 100 Hz – 3 GHz frequency range. Left graph: correct data using ferrite core on one of the cables. Right graph: incorrect low-frequency data without ferrite core.*

The left graph uses the ferrite core shown on the left photo in *Figure 27*; the right graph had direct connections with no ferrite core. Both graphs show measured data with the system board unpowered and powered. Note the peculiar error that we get at low frequencies when we measure with the S-parameter test port without using a ferrite core: the large capacitance of the system-board PDN together with the cable-braid inductance creates a realistic-looking impedance profile in the OFF condition. Note also that the low-frequency Power ON value on the left graph is slightly above one milliohm, as

opposed to the fraction of a milliohm we see from a lower-current DC-DC converter in *Figure 26*. This could be a very typical difference between measuring a system board versus a stand-alone DC-DC converter. On a system board application the DC-DC converter's high DC loop gain maintains the very low value of low-frequency impedance across the points where its sense lines are connected. Further away from the sense points the horizontal plane resistance will increase the low-frequency reading. This is not measurement error but the actual characteristics of the system board PDN.

4 Conclusions

In this paper we introduced new measurement possibilities for low-impedance PDN characterization. It was shown that the semi-floating ground reference on the Gain-Phase test port of the E5061B VNA greatly reduces the cable-braid loop error. The S-parameter test port of the VNA makes it possible to measure the entire 100 Hz to 3 GHz frequency range with one cable and probe connection. It was also shown that simple home-made reference pieces can be constructed for milliohm values. Even at low frequencies care must be taken to avoid skin-effect-like phenomena in the reference and calibration pieces. By properly monitoring and regulating the AC bias voltage across the MLCC, the correct capacitance values can be measured. Gain-phase testing and DC-DC converter output impedance measurements as well as full-system PDN measurements can also be made down to the sub-milliohm range.

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