Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range

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AGENDA

- Introduction
- Frequency-Domain PDN Measurement Methods
  - Handling the cable-braid loop error
  - Calibration process and reference pieces
  - Evaluating bypass capacitors with DC voltage bias and constant AC signal
  - Evaluating inductors with DC current bias
  - DC-DC converter measurement
- System-level measurements
- Conclusions, acknowledgement

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INTRODUCTION (1/2)

- Validation of PDN is becoming more critical
  - Tighter budgets
  - More supply rails with more interaction
- Validation can be better done in the frequency domain
- Supply voltages keep dropping
  - Target impedance goes down
- There are multiple challenges in measuring low impedances

INTRODUCTION (2/2)

Challenges in low-impedance measurements

- Except measuring components in fixtures, PDN measurements require cables to reach DUT
- Discontinuities of cable connections to DUT beyond the calibration plane introduce big errors
- Discontinuity error can be reduced by Shunt-through Two-port connection, but it creates a ground loop
- Some PDN components are sensitive to not only DC bias, but also AC bias so that the instrumentation's test signal may alter the result

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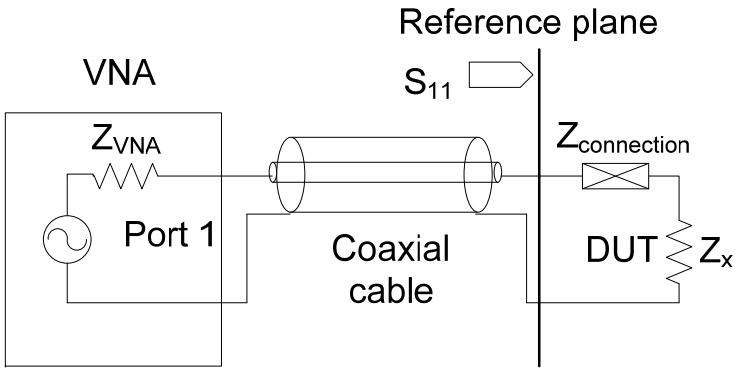
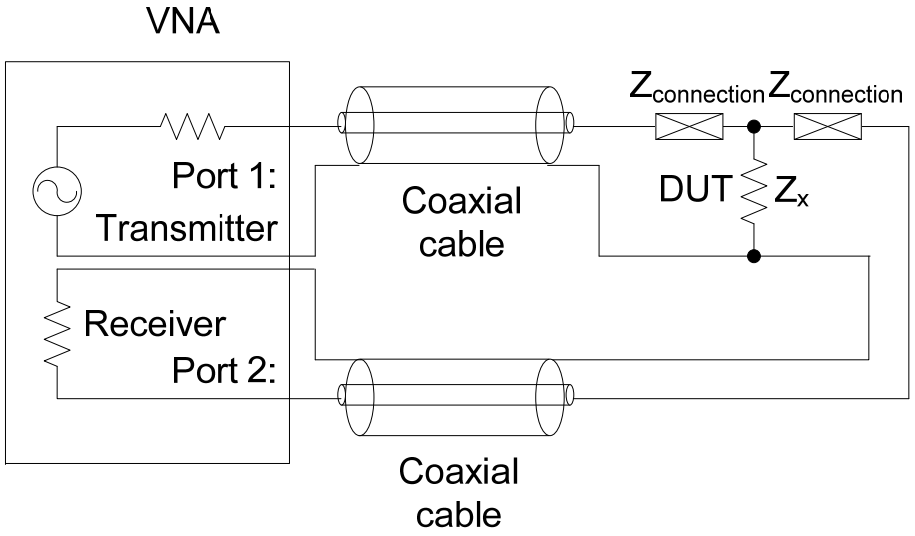
THE CABLE-BRAID LOOP ERROR (1)

The problem:

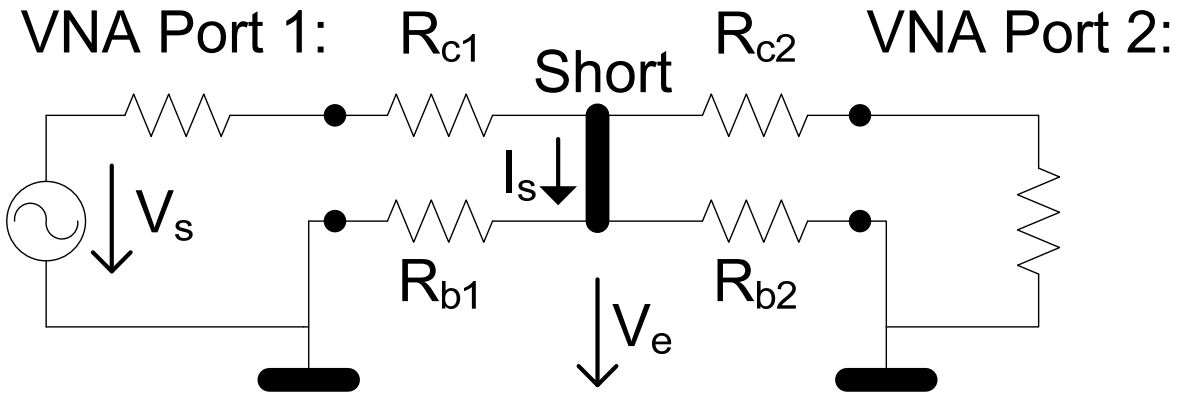


In 1-Port schemes the discontinuity of connection overwhelms the low DUT impedance



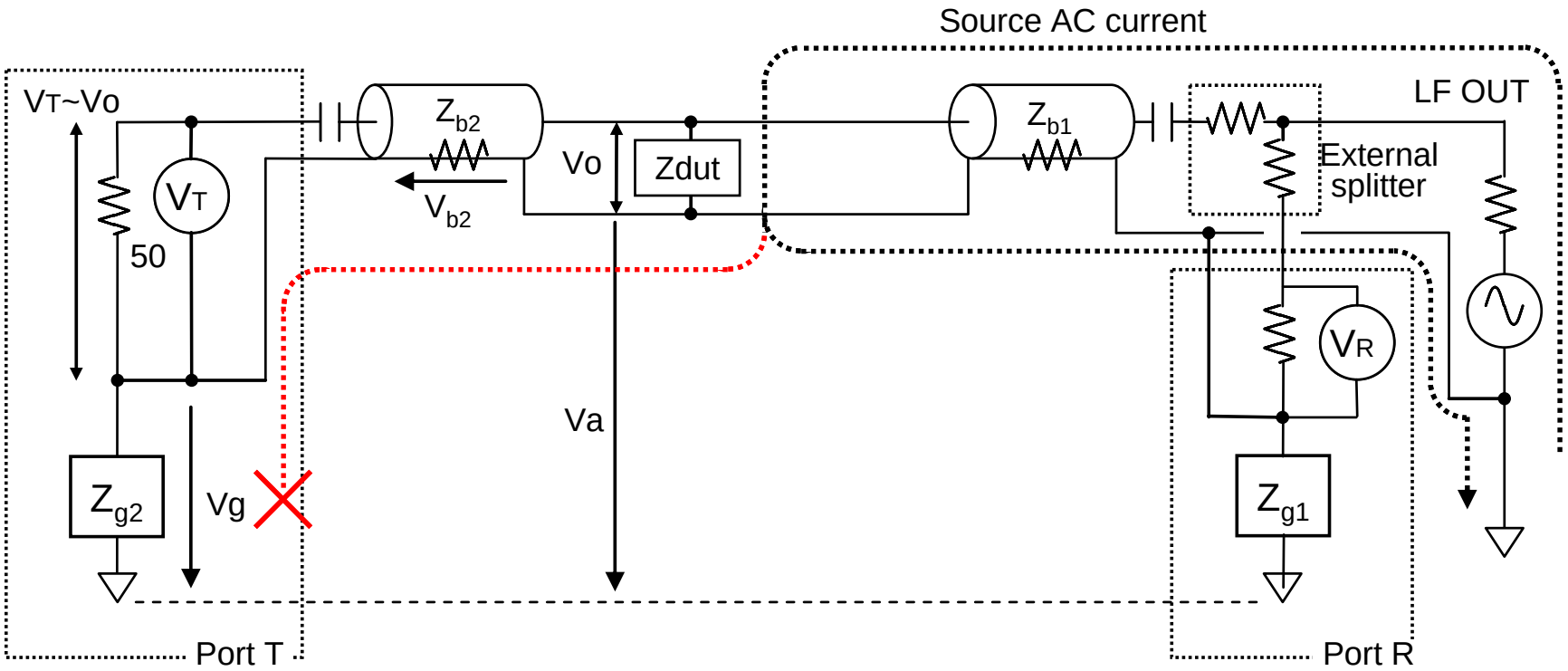
In Two-port Shunt-through schemes the effect of discontinuity is largely removed but the two cable braids create a loop.

THE CABLE-BRAID LOOP ERROR (2)



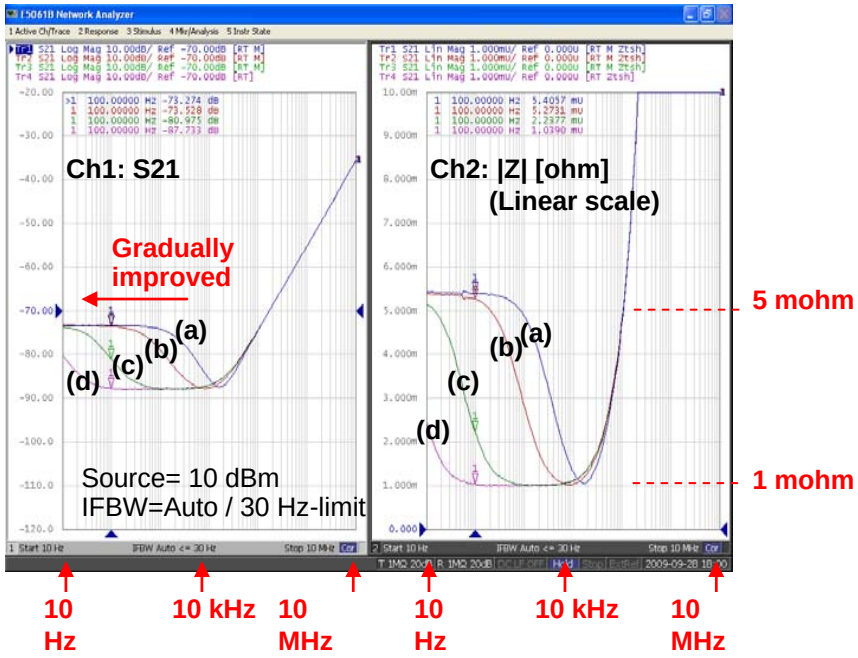
The Is test current returning on the braids lifts the lower side of the DUT. Instead of the DUT, we measure the cable braid resistance.

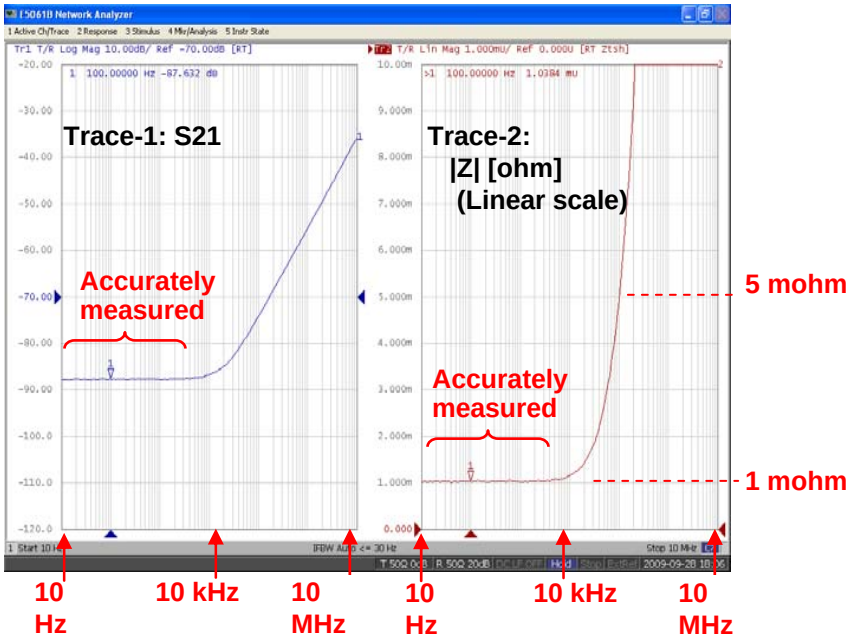
REDUCING THE CABLE-BRAID LOOP ERROR



The receivers are floated on Z_{g1} and Z_{g2}, which attenuates the error by a factor of ~Z_g/Z_b

REDUCING THE CABLE-BRAID LOOP ERROR





S21 and |Z| measurement results with S-parameter test port of E5061B-3L5

(a) Without core
(b) A clamp-on-type core is attached to test cable.
(c) A large toroidal core is attached to test cable.
(d) Test cable is turned three times around a large toroidal core.

S21 and |Z| measurement results with gain-phase test port of E5061B-3L5

Without core or isolation transformer
Source=10 dBm (-5 dBm at thru cal)
Port-T: ATT=0 dB, Zin=50 ohm, Port-R: ATT=20 dB, Zin=50 ohm

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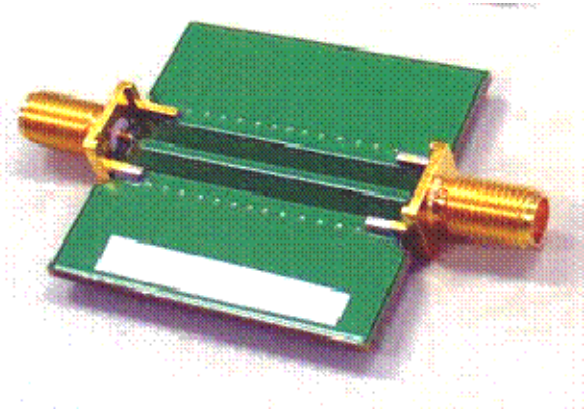
CALIBRATION

Open:



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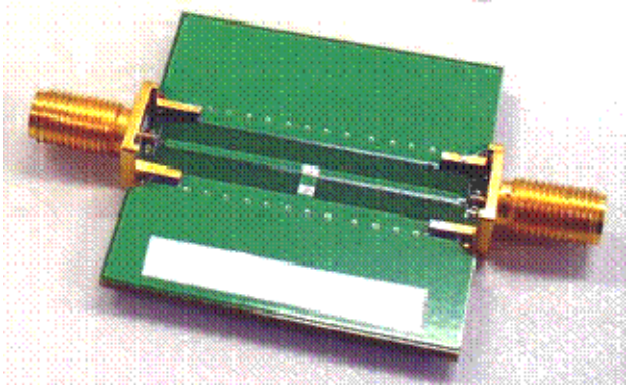
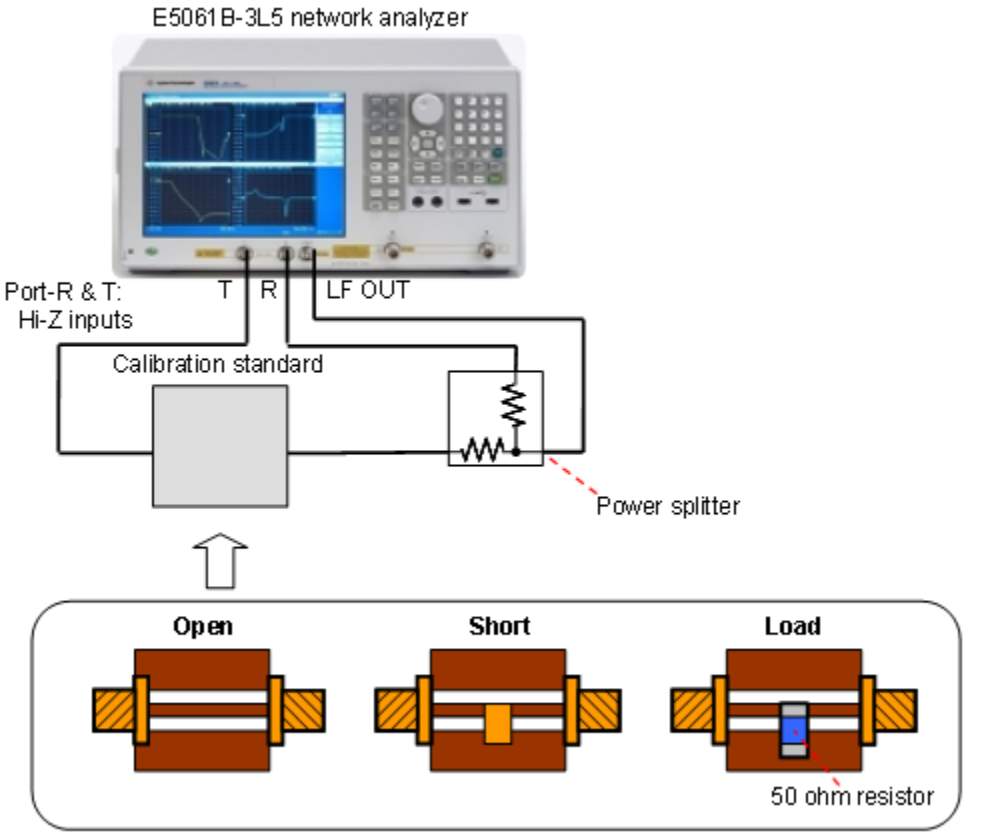
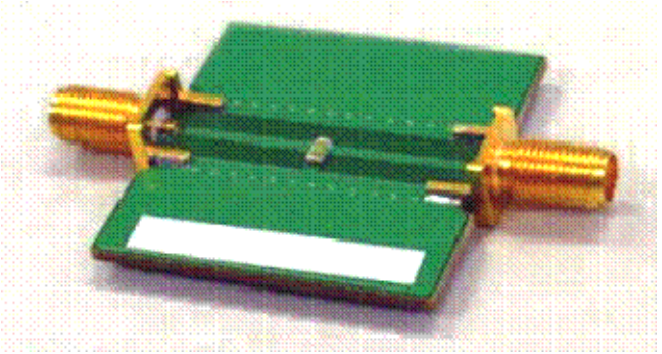


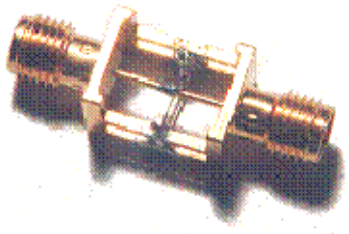


Load:



HOME-MADE CALIBRATION AND REFERENCE PIECES

Open:



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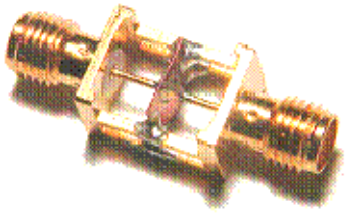

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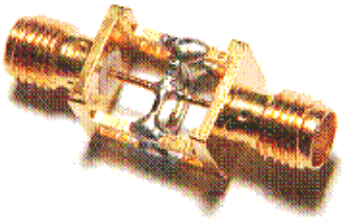
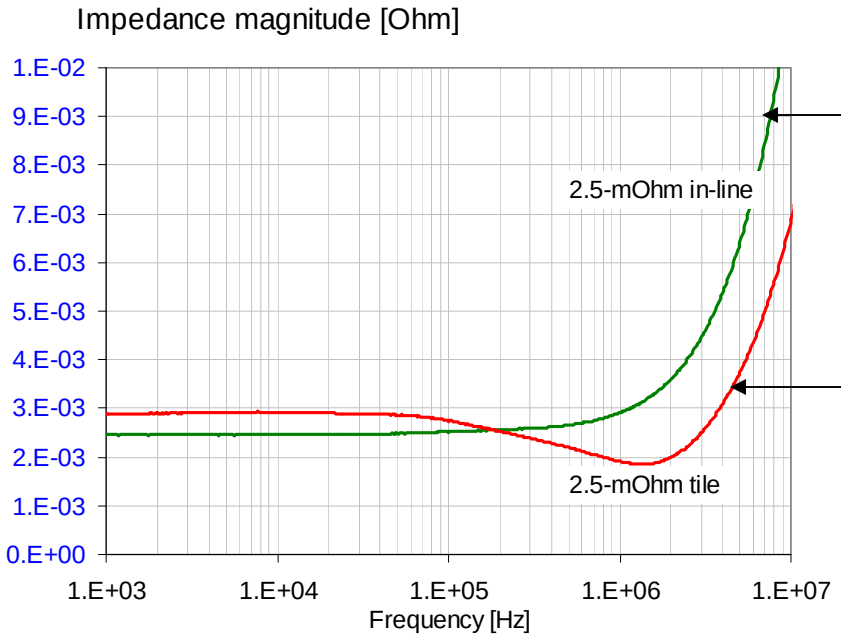
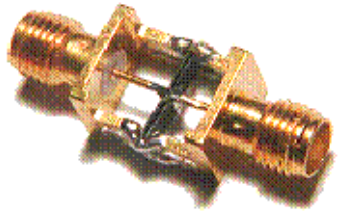
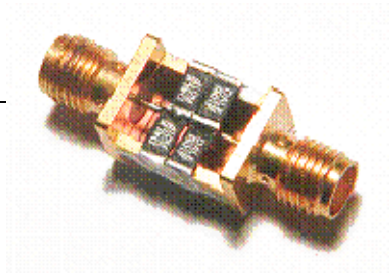




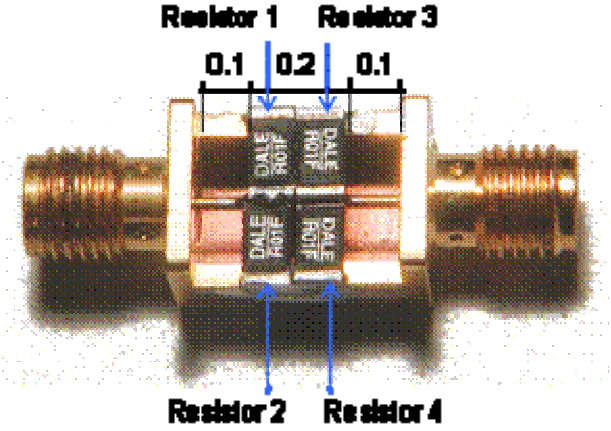


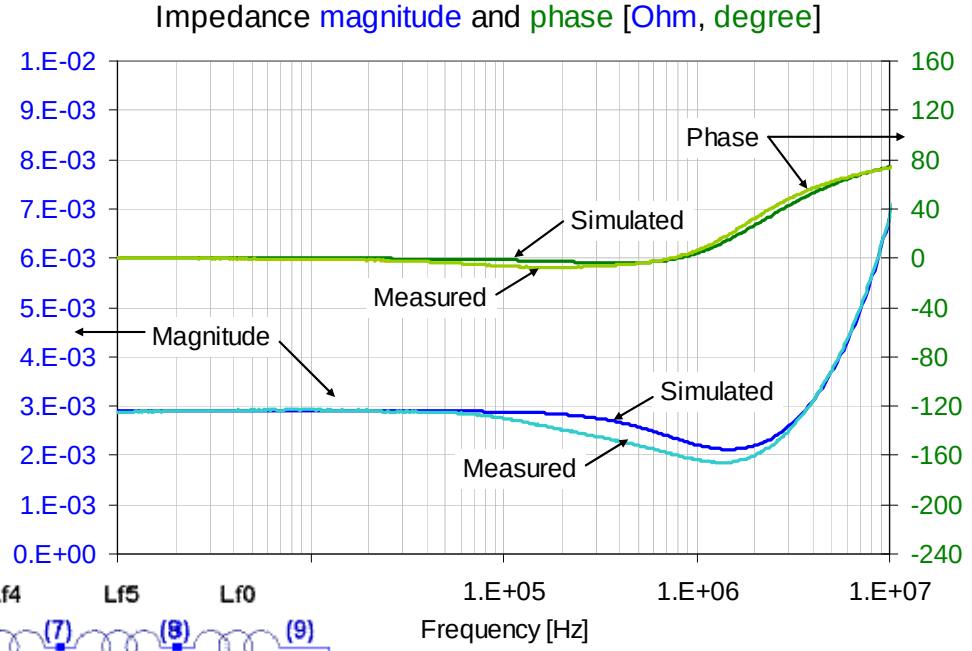
In-line reference:

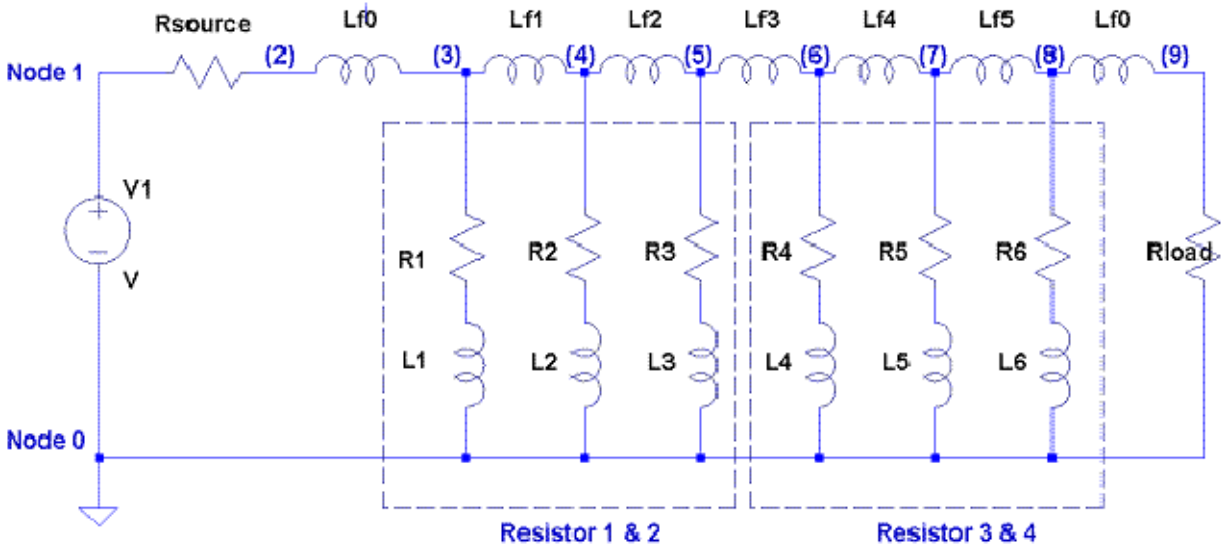


Tile reference:

ERROR IN TILE-STYLE REFERENCE PIECE







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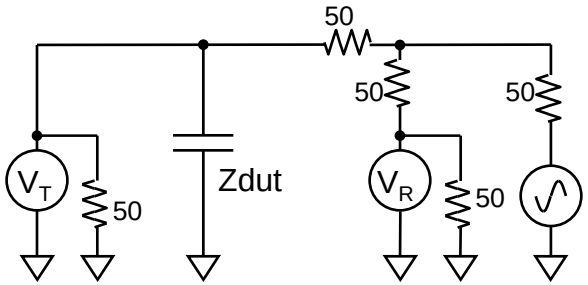
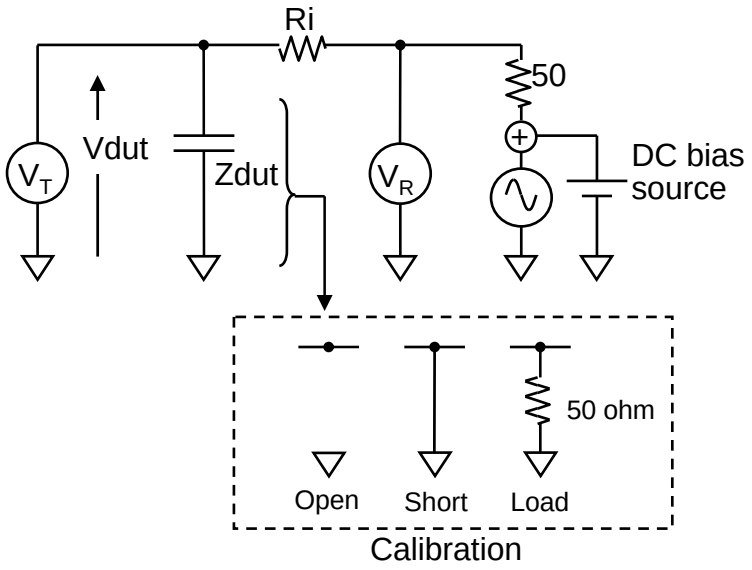
MODIFIED SHUNT-THRU METHOD FOR MEASUREMENT WITH DC BIAS & CONSTANT AC

Conventional shunt-thru method with 50 ohm inputs



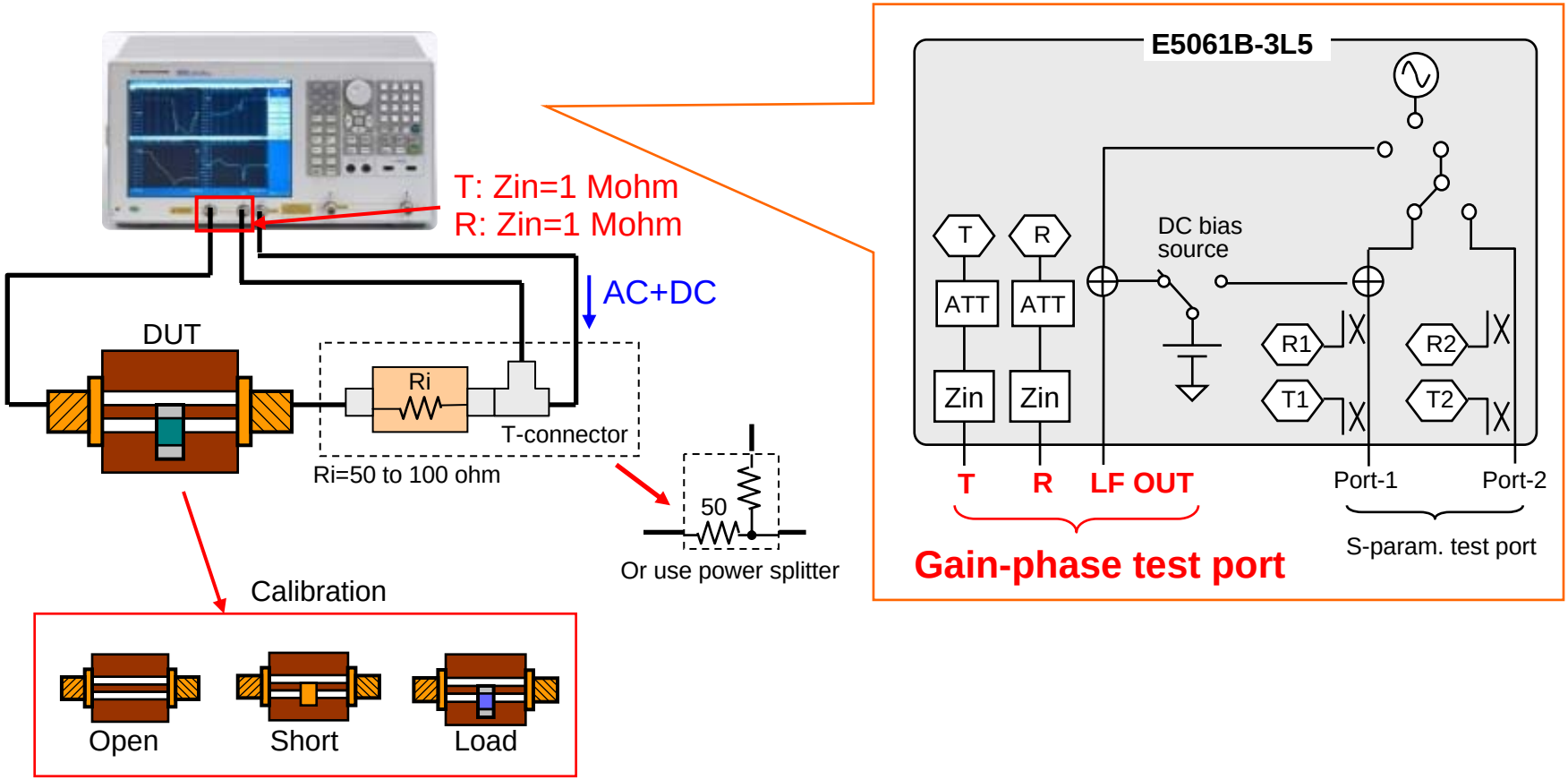
Zdut = 25 x S21 / (1-S21)

Shunt-thru method with High-Z inputs

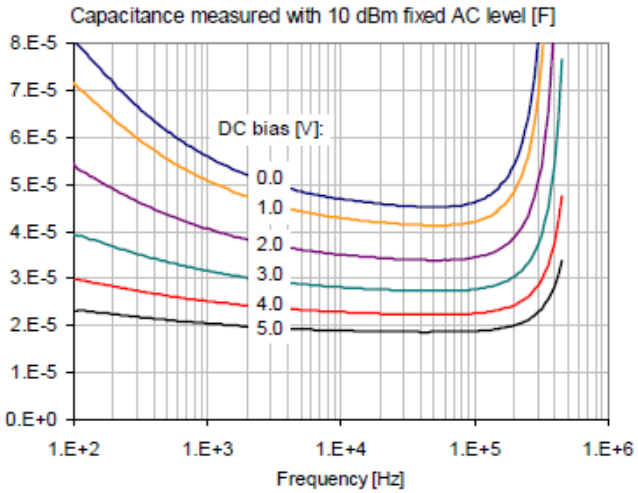


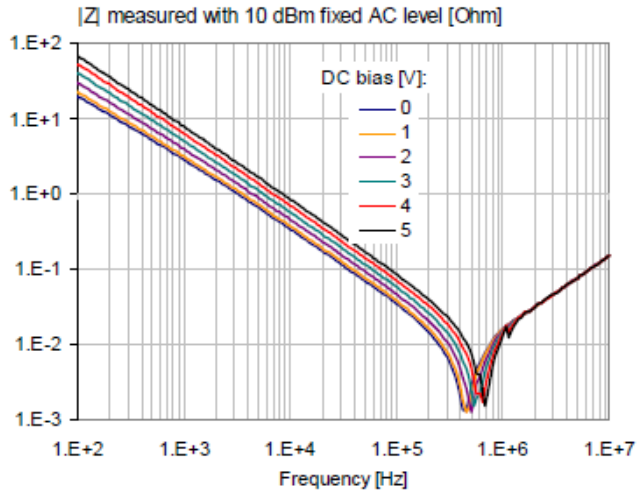
- Hi-Z receivers can receive DC bias up to 40 Vdc.
- V_T monitors AC voltage across DUT (=Vdut).
- Need 3-term cal in Z-domain.

MEASUREMENT CONFIGURATION WITH E5061B GAIN-PHASE TEST PORT



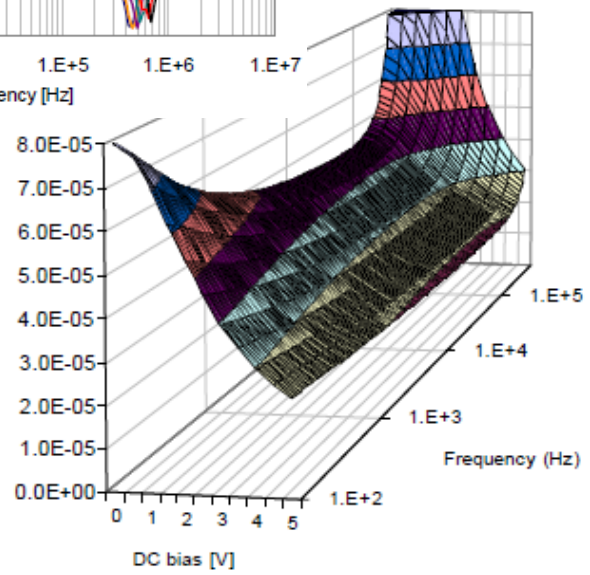
EVALUATING BYPASS CAPACITORS WITH DC VOLTAGE BIAS





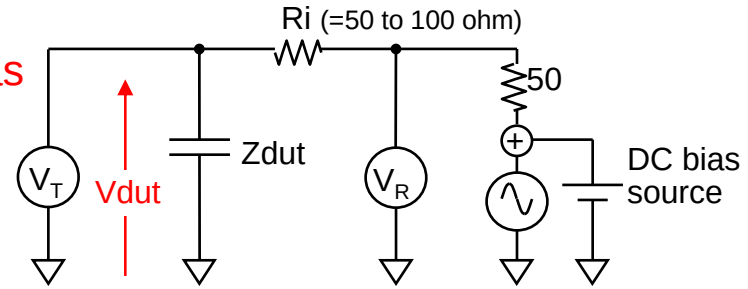
MLCC (Multi-layer Ceramic Capacitor) measurement with DC bias

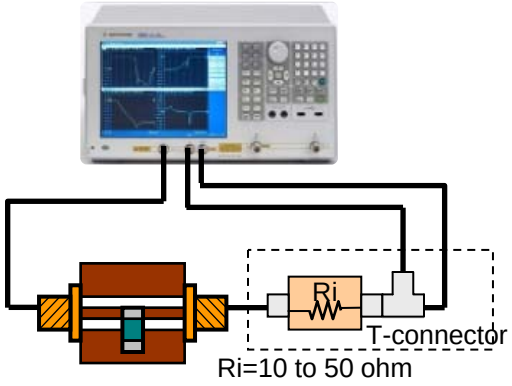
Test freq: 100 Hz to 10 MHz
AC level: 10 dBm fixed source setting
DC bias: 0 to 5 Vdc



EVALUATING BYPASS CAPACITORS WITH CONSTANT AC SIGNAL LEVEL (1)

V_T monitors Vdut as 20*Log(Vdut^2/50)





Pre-measurement for making constant-AC sweep table

	Initial source setting
Freq-1	-20 dBm
Freq-2	-20 dBm
:	:
Freq-N	-20 dBm

Trig →

AC level across DUT
-23 dBm
-24 dBm
:
-40 dBm

→

Next source setting
(-20 + 3) dBm
(-20 + 4) dBm
:
(-20 + 10) dBm

Trig →

Repeat steps b and c a few times. (… And then perform measurement.)

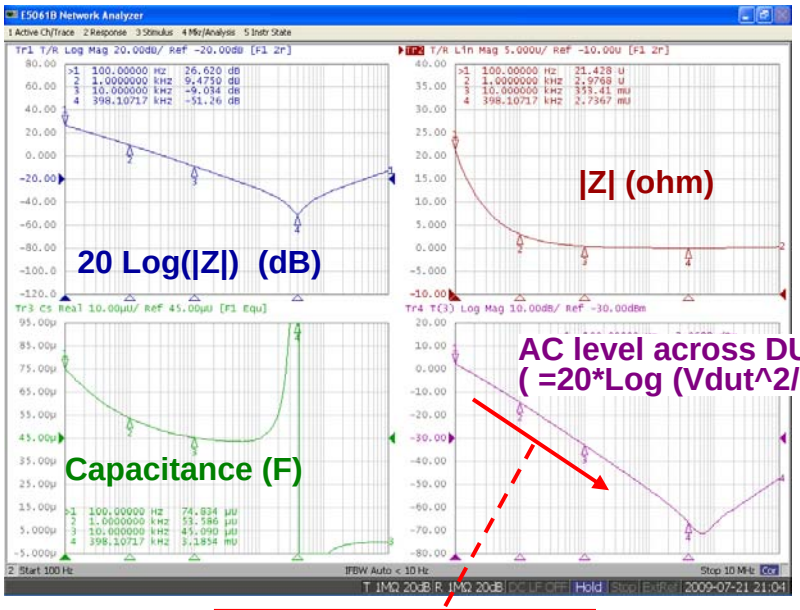
a) Set source level to target level.

b) Measure Vdut.

c) Change source level.

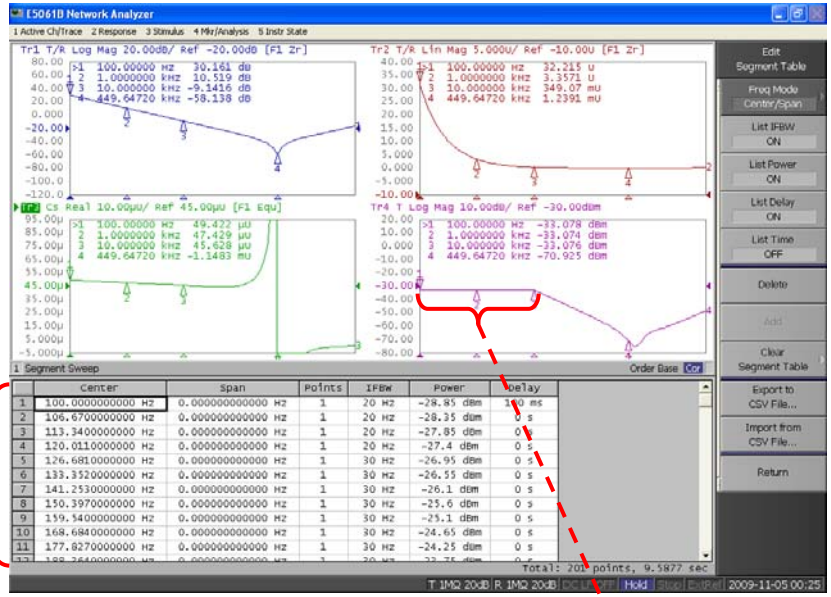
EVALUATING BYPASS CAPACITORS WITH CONSTANT AC SIGNAL LEVEL (2)

(a) Source level = 10 dBm fixed



AC level applied to DUT is not constant.

***(b) Applying constant AC** (5 mVrms at DUT)*

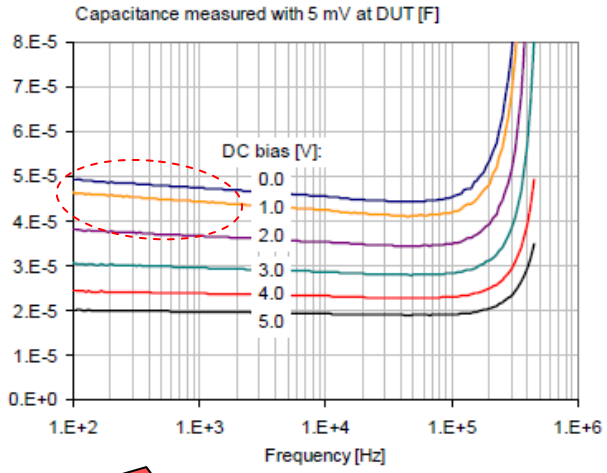


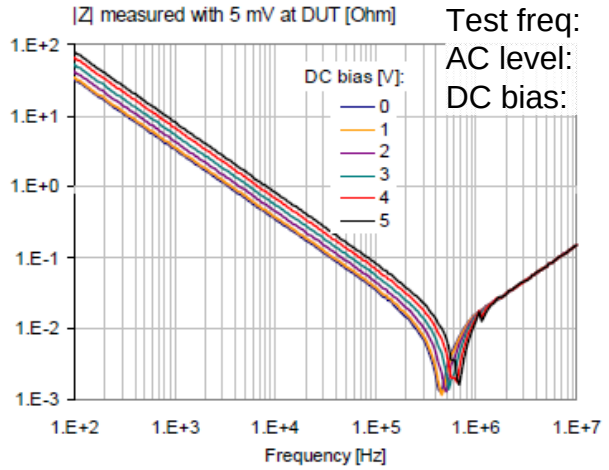
Constant-AC sweep table created by pre-measurement
- 201 segments
- 100 Hz to 10 MHz.

5 mVrms is constantly applied to DUT in this freq range.

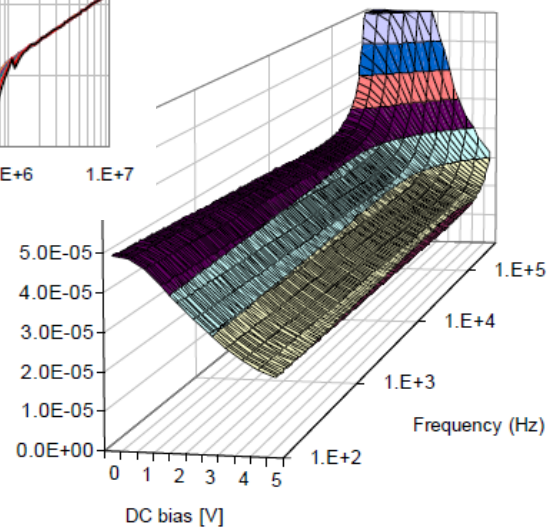
EVALUATING BYPASS CAPACITORS WITH CONSTANT AC LEVEL AND DC BIAS

MLCC measurement with constant AC level and DC bias

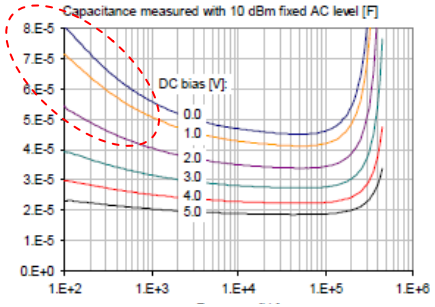




Test freq: 100 Hz to 10 MHz
AC level: 5 mVrms constant at DUT
DC bias: 0 to 5 Vdc

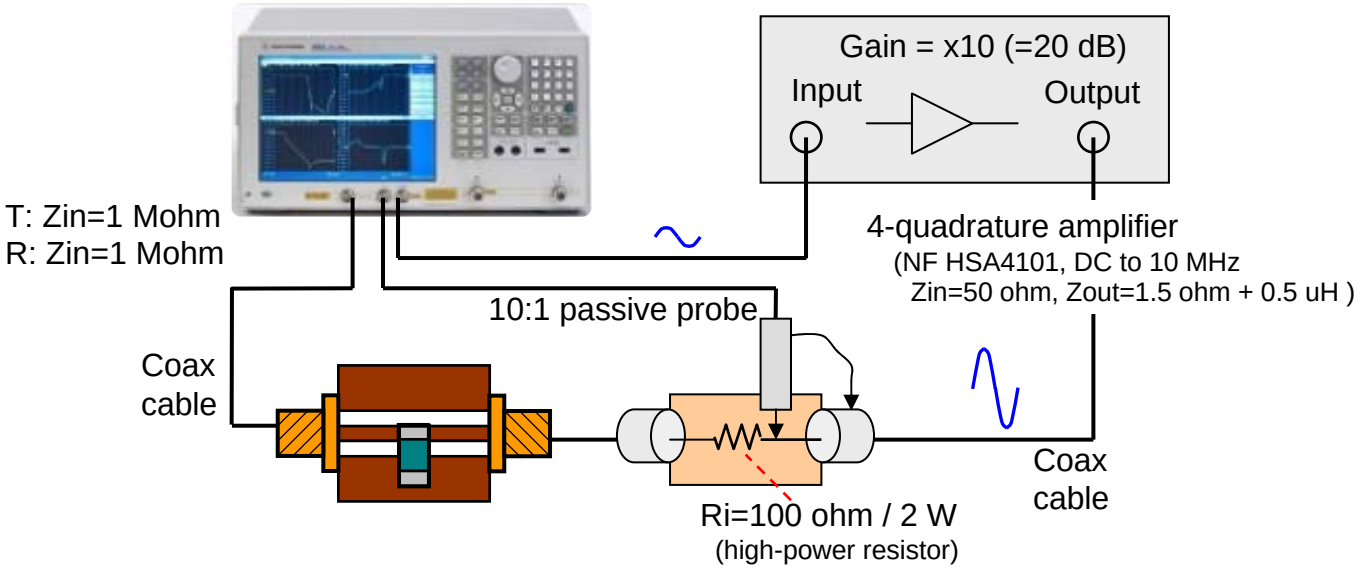


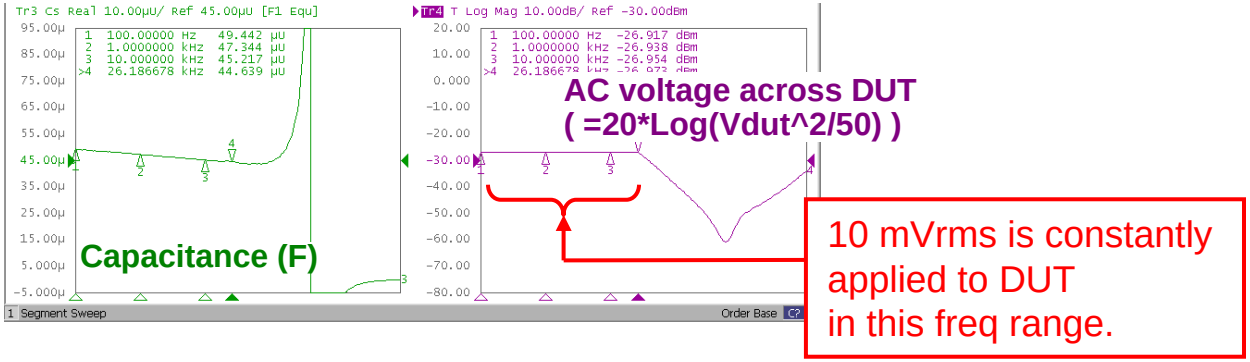
Improvement with constant AC



With fixed source setting…

APPLYING HIGHER CONSTANT AC LEVEL





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  - Example of MLCC measurement with constant AC level and DC bias
  - Applying higher constant AC level
  - Evaluating inductors with DC current bias
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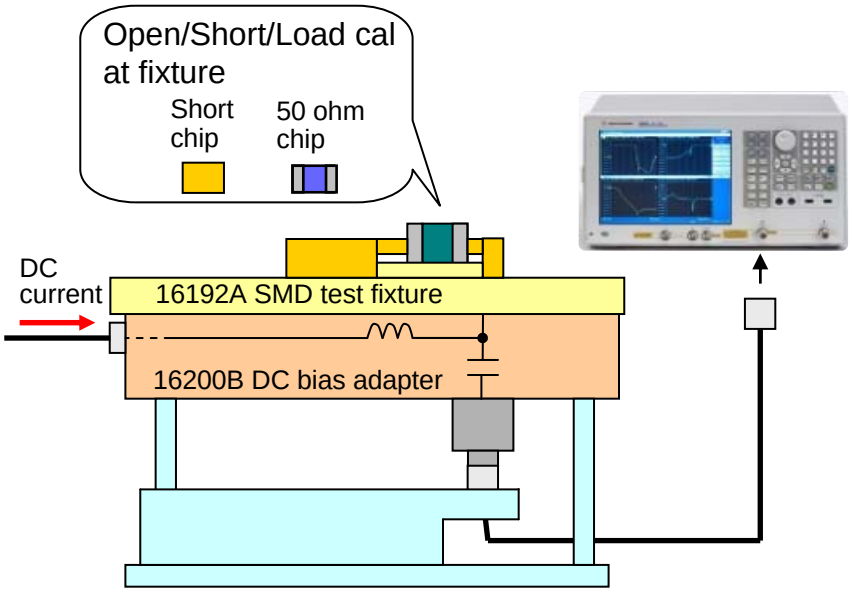
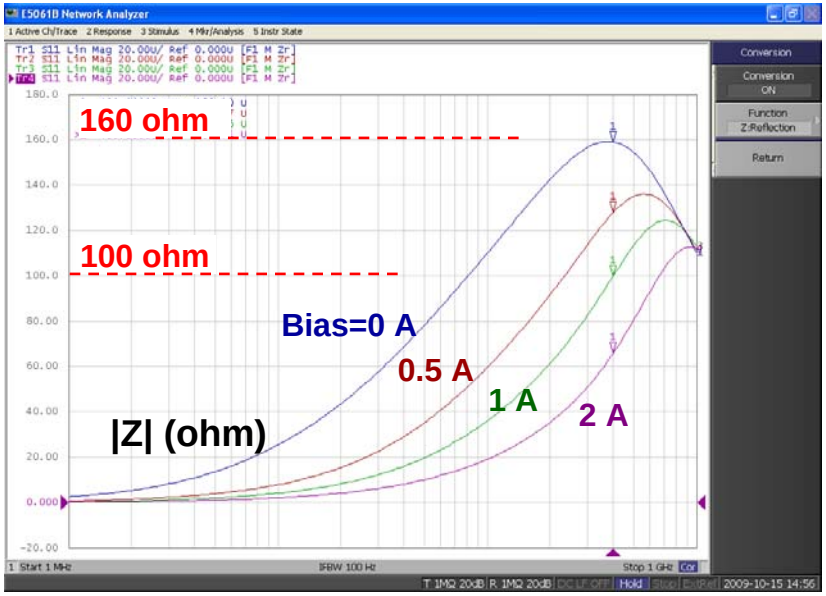
EVALUATING INDUCTORS WITH DC BIAS CURRENT (1)

***1-port reflection method with bias tee** (Test freq: 1 MHz to 1 GHz, DC bias: up to 5 Adc)*



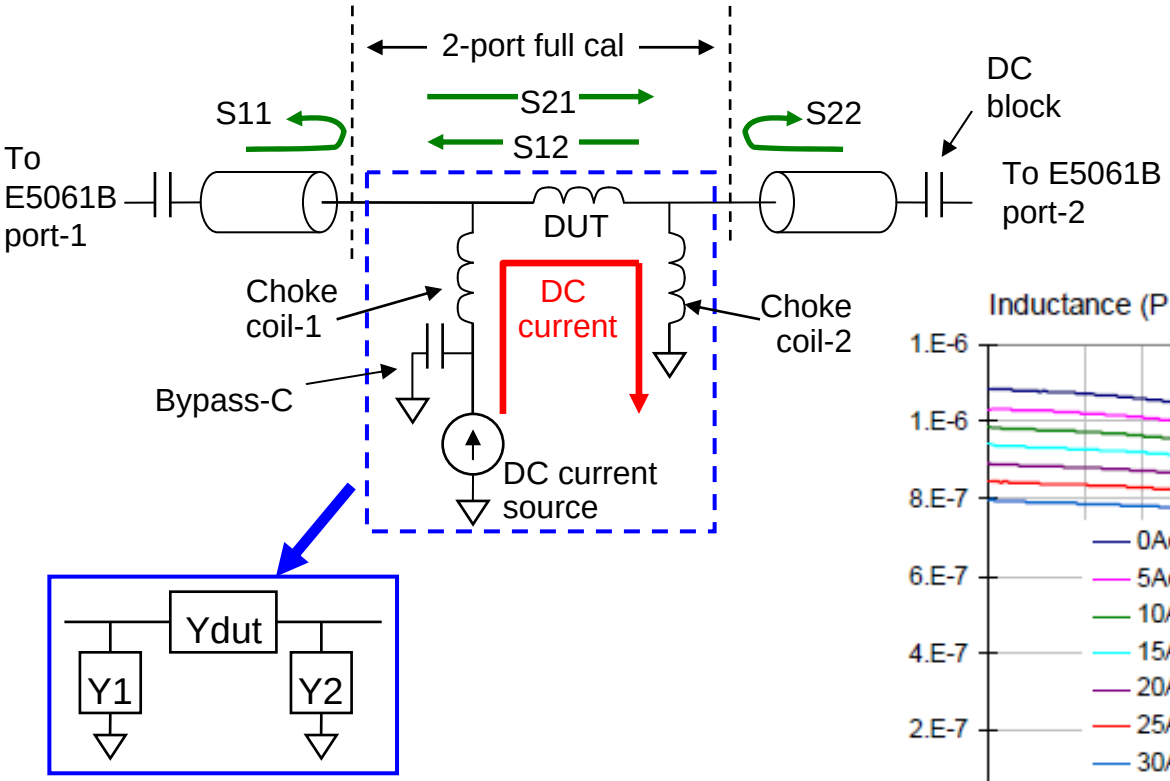


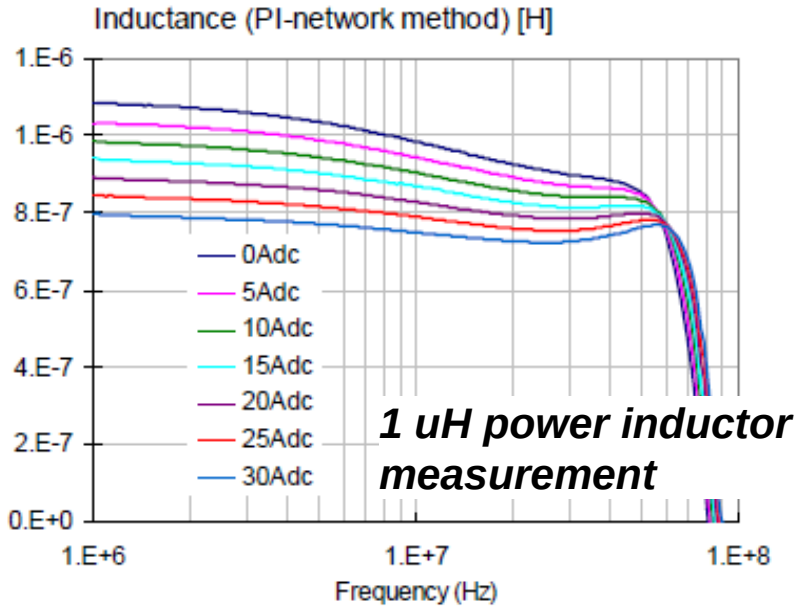
Ferrite bead measurement

Test freq: 1 MHz to 1 GHz
DC bias: 0 to 2 Adc

EVALUATING INDUCTORS WITH DC BIAS CURRENT (2)

***PI-network method** (Test freq: 1 MHz to 100 MHz, DC bias: up to >30 Adc)*





1 uH power inductor measurement

$Zdut=1/Ydut=50((1+S_{11})(1+S_{22})-S_{12}S_{21})/(2S_{21})$

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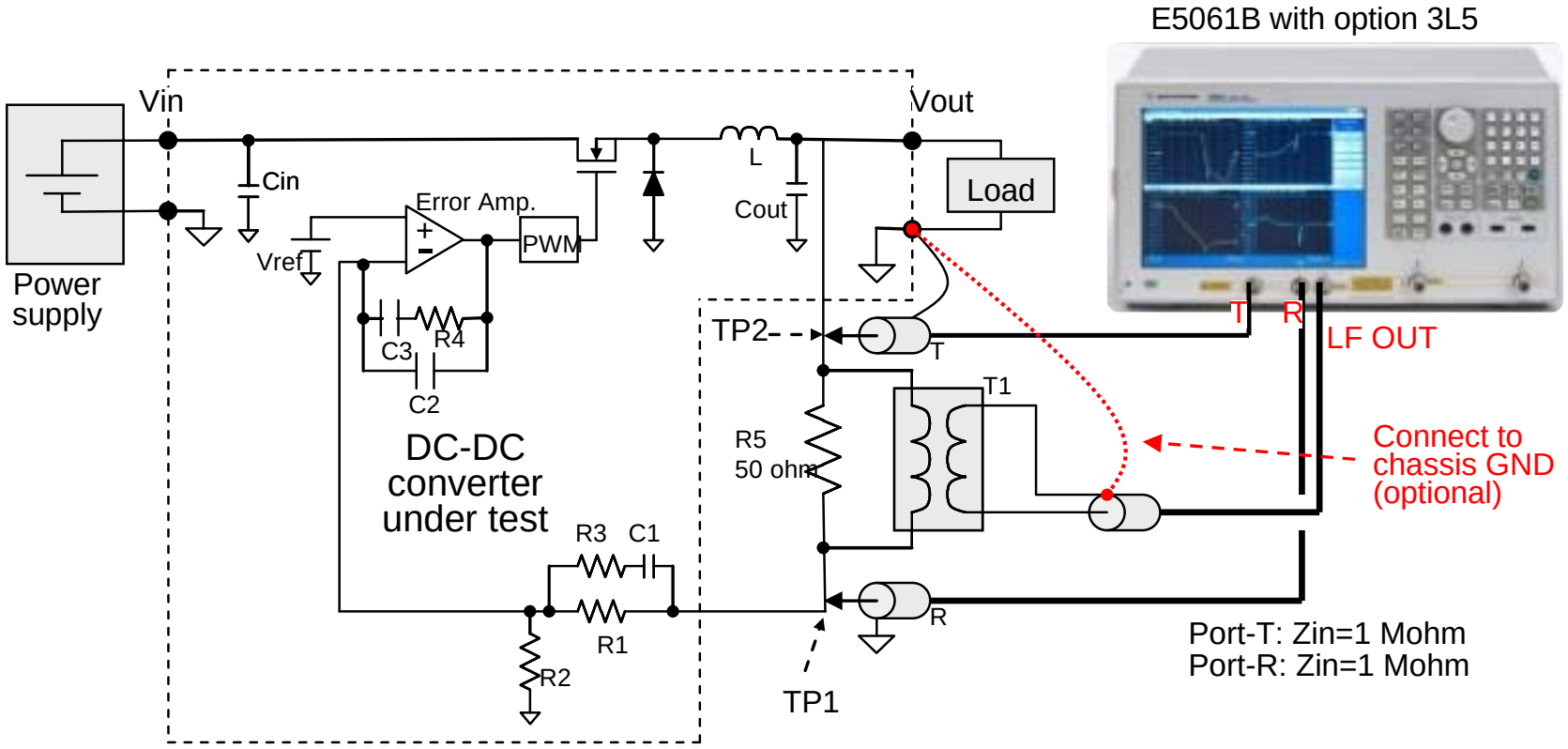
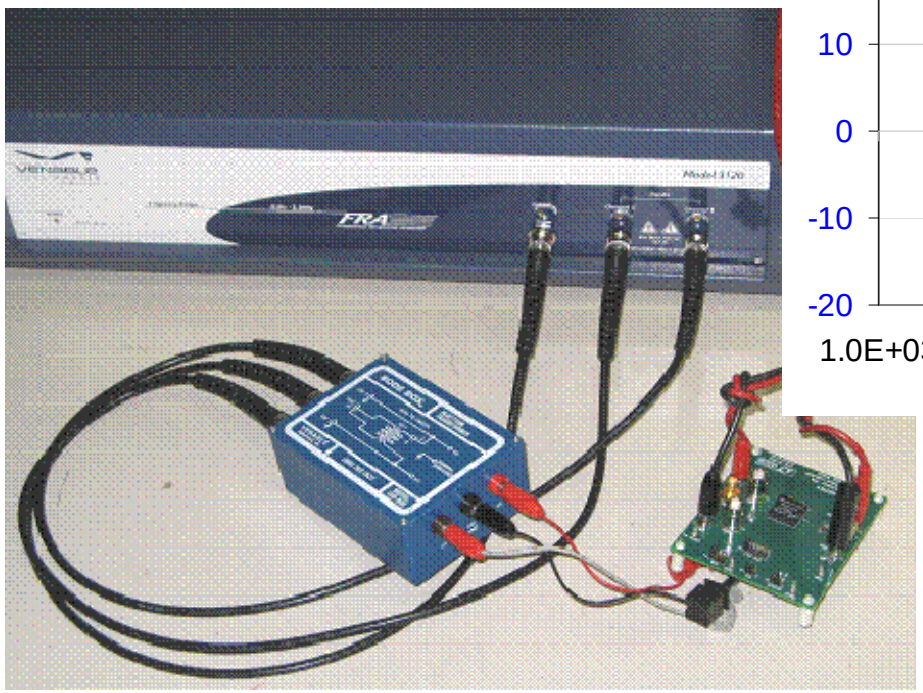
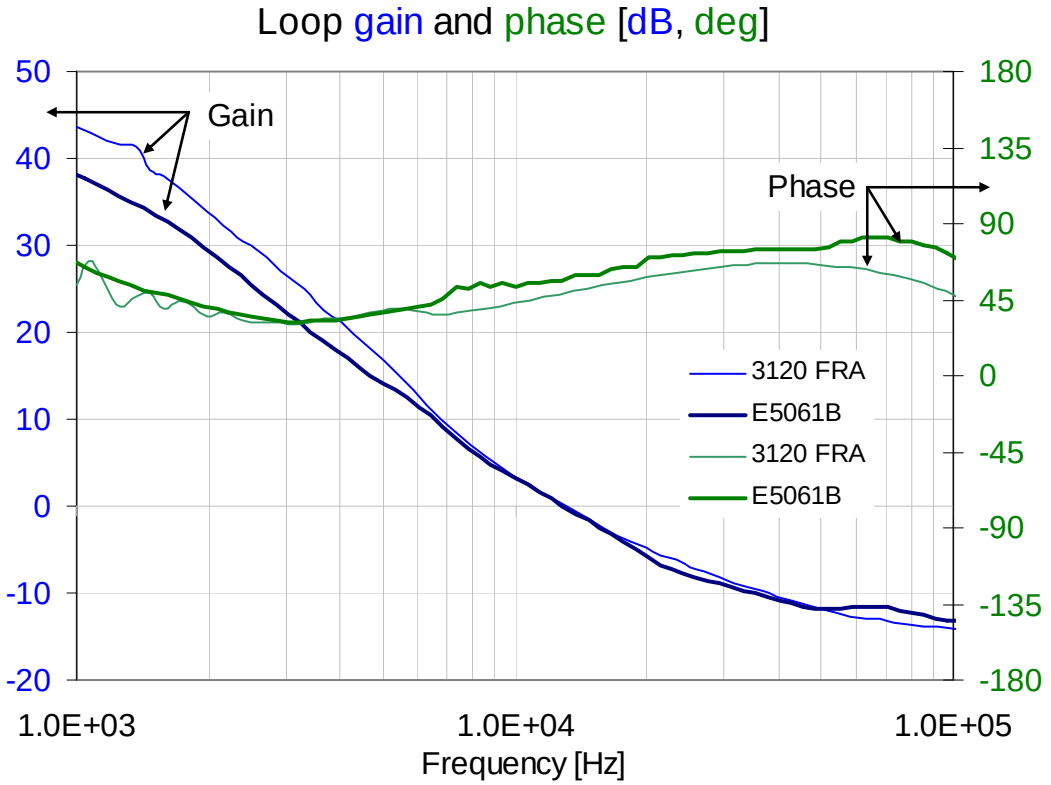
DC-DC CONVERTER MEASUREMENTS (1)



DC-DC CONVERTER MEASUREMENTS (2)

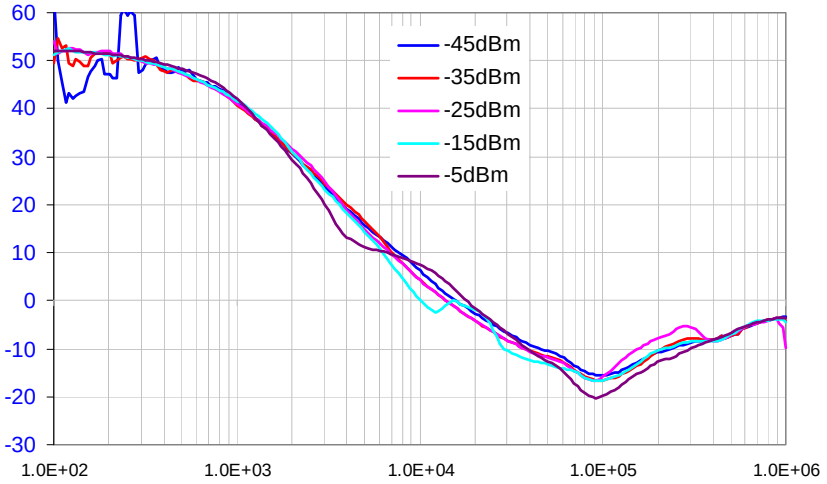
Loop stability measurement of a Linear Technology LTM4617 evaluation module



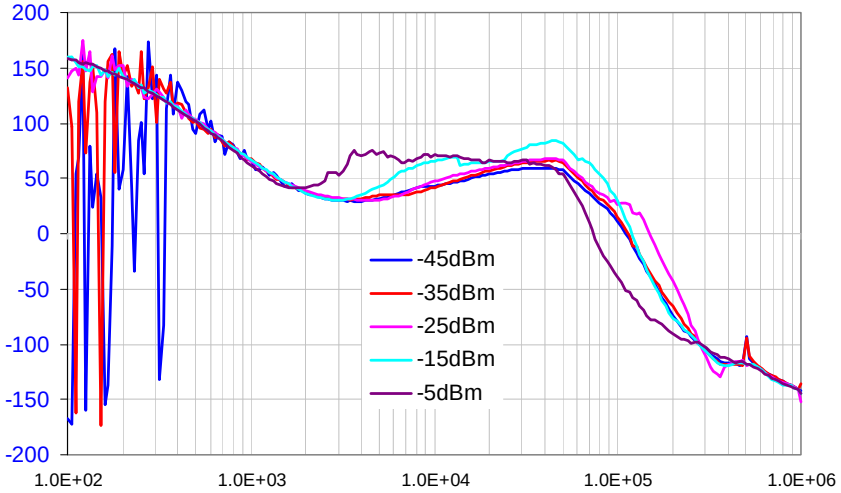


DC-DC CONVERTER MEASUREMENTS (3)

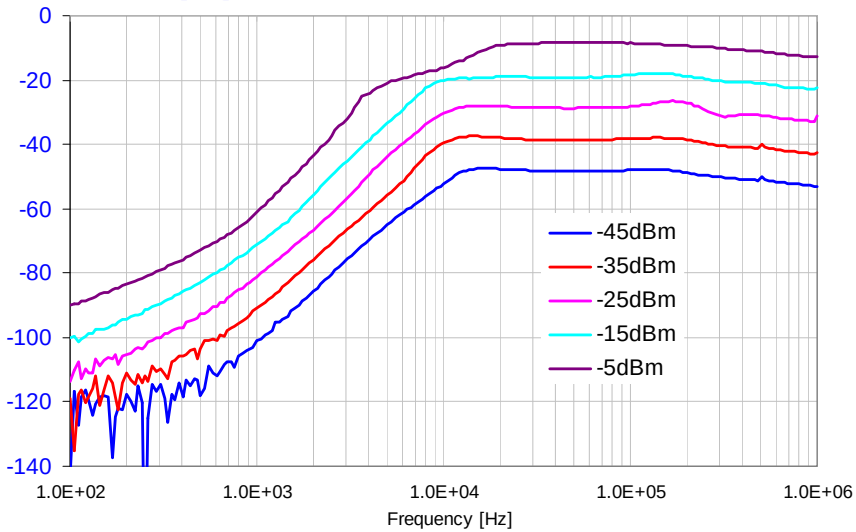
Loop gain [dB]



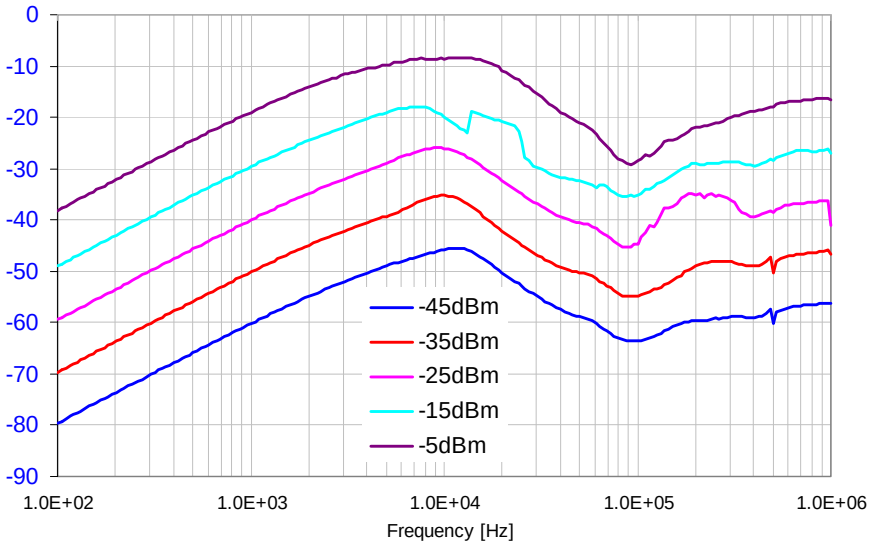
Loop phase [deg]



R level [dB]

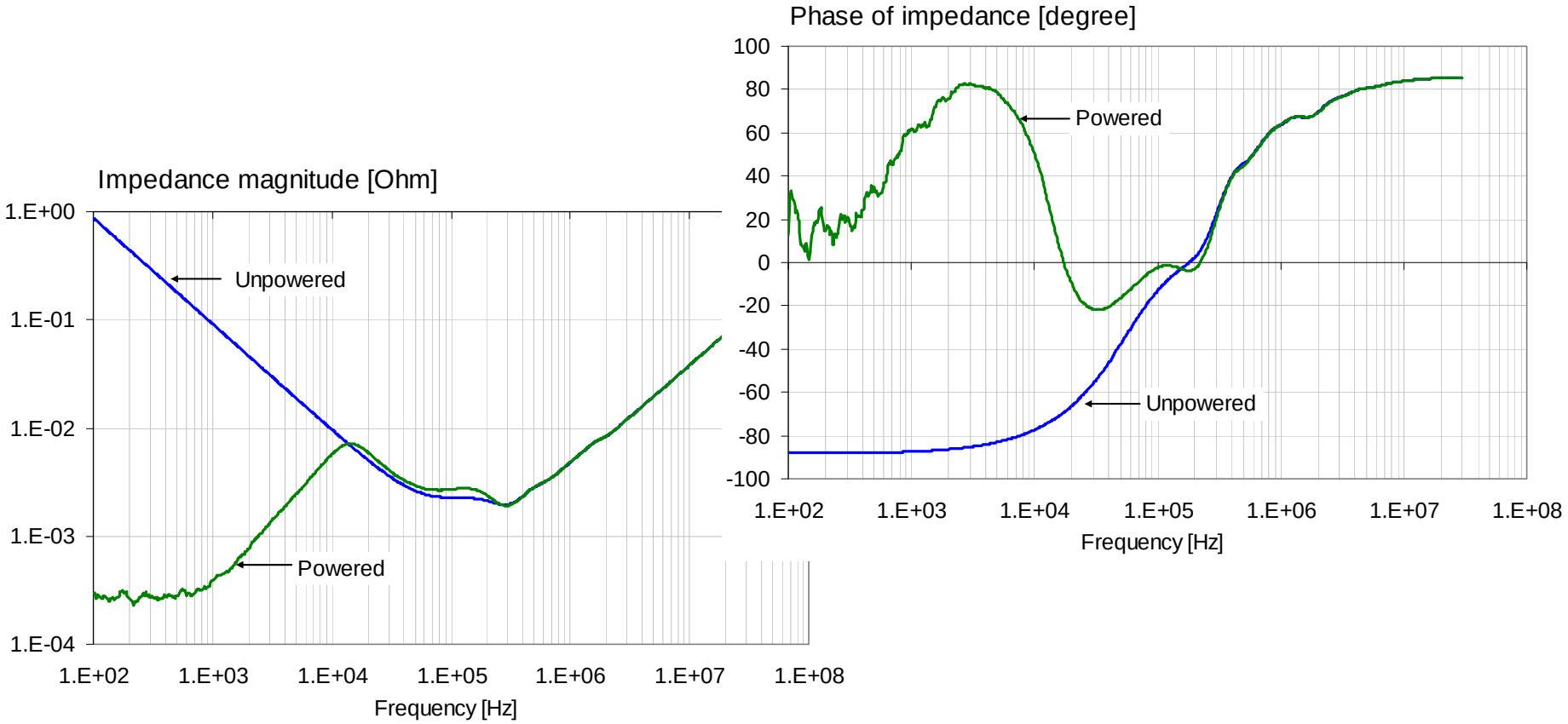


T level [dB]



DC-DC CONVERTER MEASUREMENTS (4)

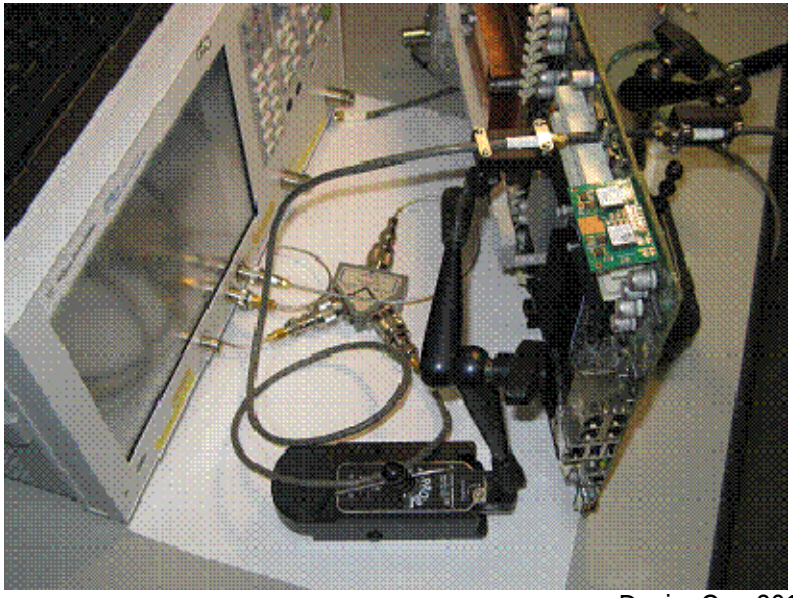
Output impedance magnitude (on the left) and phase (on the right) of a 15-A 1V DC-DC converter

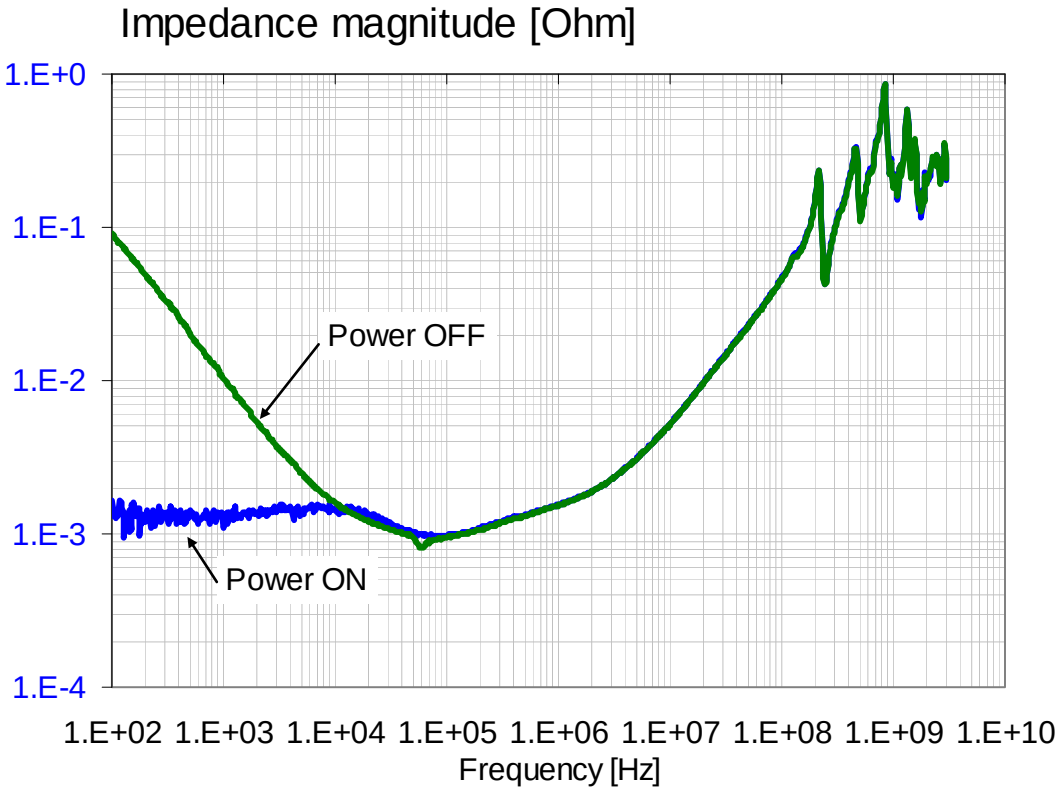


AGENDA

- Introduction
- Frequency-Domain PDN Measurement Methods
  - Handling the cable-braid loop error
  - Calibration process and reference pieces
  - Evaluating bypass capacitors with DC voltage bias
  - Evaluating bypass capacitors with constant AC signal level
  - Example of MLCC measurement with constant AC level and DC bias
  - Applying higher constant AC level
  - Evaluating inductors with DC current bias
  - DC-DC converter measurement
- System-level measurements
- Conclusions, acknowledgement

SYSTEM-LEVEL MEASUREMENTS





SUMMARY

- Semi-floating ground reference greatly reduces cable-braid error
- MLCCs may exhibit dependence on AC bias as well
- Scripts can help to keep AC level across DUT at user-defined levels
- Gain-phase test port can measure both loop margin and output impedance of DC-DC converters

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THANK YOU