DesignCon 2011

Technical panel TP-M3:

Capacitor Modeling Requirements in the 21st Century

Panelists:

John Prymak	Kemet
Steve Pytel	Ansys
Bruce Archambeault	IBM
Istvan Novak*	Oracle

* panel organizer

Abstract

Many capacitors are used in today's electronics. Some of the critical applications include DC-blocking in high-speed SerDes signaling and bypass capacitors of power distribution networks. To simulate the electrical performance and to specify parts, we use models to describe the parts behavior. A simple equivalent circuit uses series lumped C-R-L elements, sometimes including frequency, temperature and bias-voltage dependence. Capacitors can also be described by impedance, admittance or scattering-parameter listing as a function of frequency. The necessary frequency range and the included parameters depend on the applications and type of capacitors. For instance, large bulk capacitors for bypass applications need to focus on capacitance and ESR at relatively low frequencies, whereas DC-blocking capacitors for multi-Gbps SerDes signals need a lot of high-frequency details. This panel brings together capacitor vendors, CAD tool vendors and OEMs to discuss the various data formats for the different capacitor types and applications.

Panelist biographies

John Prymak, Kemet
John is the Director of Advanced Applications in the Advanced Technology Group at KEMET Electronics Corp. John worked for AVX, at the Advanced Products Group in Olean, NY, for 15 years and was involved in the early introductions of the stacked ceramic capacitors, reverse geometry low inductance capacitors, multiple capacitor EMI/RFI filters, high voltage products, and multilayer varistors, leaving as a Development Engineer in 1990. He has been working at KEMET for the past 20 years. In his 35 year history with both manufacturers, he has been involved with ceramic, film, wet and dry tantalum, aluminum-polymer, and aluminum electrolytic capacitors. John has authored or co-authored close to one hundred technical papers presented at technical symposiums. Topics include SPICE modeling, failure analysis, flex, power, ripple current capabilities, surge, EMI/RFI, high voltage, and improved electrical performance through improvements in ESL and ESR. Several papers have been presented in technical publications and he has also been contributing author for a couple of text books dealing with dielectric studies and circuit packaging. John has been granted fifteen patents, to date.
John is the author of the KEMET Spice software that was started in early 1997, and has also written programs for SSST (Surge Step Stress Testing) analysis, Flex testing and analysis, Reverse-Voltage analysis on polar capacitors, and Weibull Life testing and data analysis.

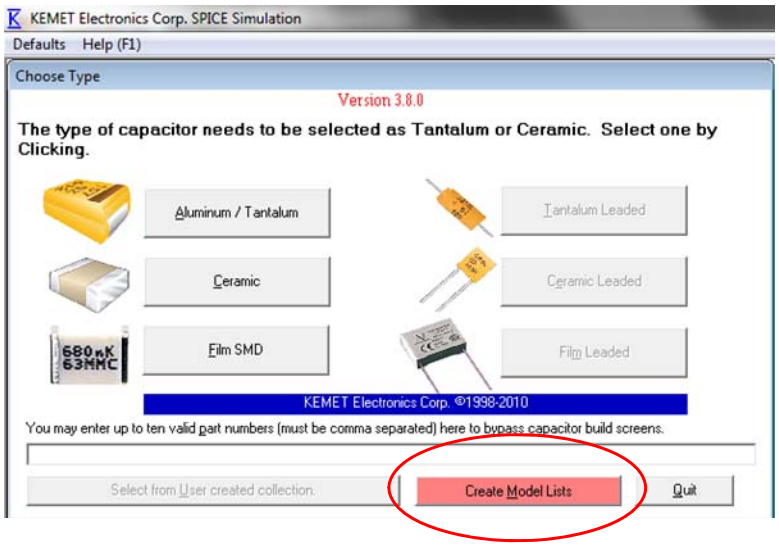
Steve Pytel, Ansys-Ansoft
Dr. Steven Gary Pytel Jr. is currently employed with ANSYS, INC., as the Signal Integrity Product Manager. He received a Doctor of Philosophy specializing in Signal Integrity from the University of South Carolina, a Masters of Engineering from the University of South Carolina, and a Bachelors of Science from Northern Illinois University. Steve previously worked at Intel Corporation as a Senior Signal Integrity and Hardware Design Engineer where he helped design Blade, Telecom, and Enterprise servers. He focused on research which incorporated frequency dependent dielectric losses and copper surface roughness losses into transmission line models. His current research interests include high speed serial signaling and statistical analysis of digital circuits. He has over 20 publications along with several invited papers and presentations. He has written an invited chapter on signal integrity simulation for John Wiley, IEEE-Interscience entitled, Maxwellâ€™s Equations: The Foundations of Signal Integrity authored by Paul G. Huray.

Bruce Archambeault, IBM
Bruce is a Distinguished Engineer at IBM in Research Triangle Park, NC. He received his B.S.E.E degree from the University of New Hampshire in 1977 and his M.S.E.E degree from Northeastern University in 1981. He received his Ph.D. from the University of New Hampshire in 1997. Dr. Archambeault has authored or co-authored a number of papers in computational electromagnetics, mostly applied to real-world EMC applications. He is currently a member of the Board of Directors for the IEEE EMC Society and a past Board of Directors member for the Applied Computational Electromagnetics Society (ACES). He has served as a past IEEE/EMCS Distinguished Lecturer and Associate Editor for the IEEE Transactions on Electromagnetic Compatibility.

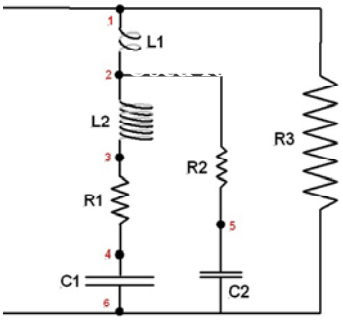
Istvan Novak, Oracle-America
Dr. Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high speed serial and parallel buses, he is engaged in the design and characterization of power distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

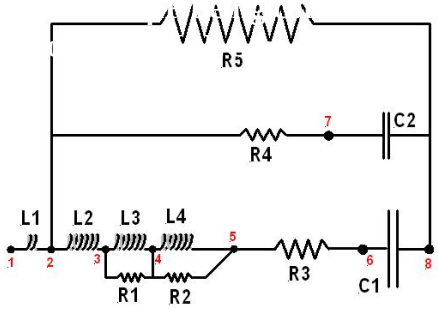
Creating Application Specific EDA Models

KEMET Spice Software

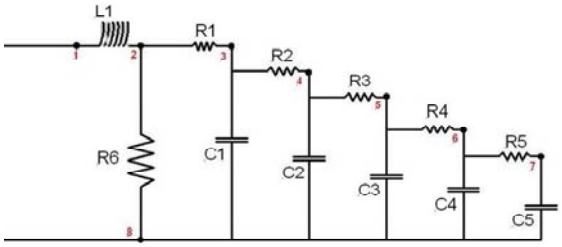


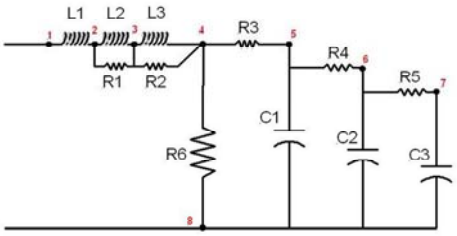
NetList Type Models used for Film and MLCC



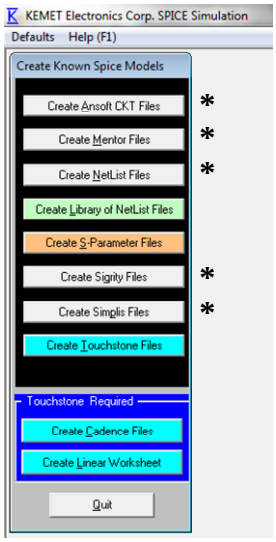


NetList RC-Ladder Models for Electrolytic Capacitors





Multiple EDA Model Selections



*** Very similar**

Time to Create Ceramic Files

	Ceramic SMD Capacitors					
	Commercial SMD		Military SMD		All Ceramic	
	PNs	Seconds	PNs	Seconds	PNs	Seconds
Ansoft	2930	16	458	3	3388	19
Cadence	2930	6	458	2	3388	8
Mentor	2930	16	458	2	3388	18
NetList (.Ckt/.END)	2930	16	458	3	3388	19
NetList (.Ckt/.ENDS)	2930	15	458	2	3388	17
NetList (.Cir/.ENDS)	2930	15	458	2	3388	17
NetList Library	2930	18	458	3	3388	21
S-Param (Shunt)	2996	30	483	6	3479	36
S-Param (Series)	2996	30	483	6	3479	36
Sigrity	2930	15	458	2	3388	17
Simplis	2930	19	458	4	3388	23
Touchstone Z	2930	32	458	5	3388	37

Time to Create Al/Tant Files

	Aluminum/Tantalum SMD Capacitors					
	Commercial SMD		Military SMD		All Al/Tant	
	PNs	Seconds	PNs	Seconds	PNs	Seconds
Ansoft	2125	13	833	5	2958	18
Cadence						
Mentor	2125	13	833	6	2958	19
NetList (.Ckt/.END)	2125	13	833	6	2958	19
NetList (.Ckt/.ENDS)	2125	13	833	5	2958	18
NetList (.Cir/.ENDS)	2125	12	833	5	2958	17
NetList Library	2125	13	833	9	2958	22
S-Param (Shunt)	2125	31	837	11	2958	42
S-Param (Series)	2125	31	837	11	2958	42
Sigrity	2125	15	833	6	2958	21
Simplis	2125	22	833	8	2958	30
Touchstone Z	2125	27	833	10	2958	37

Time to Create Film Files

	Film SMD Capacitors	
	Commercial SMD	
	PNs	Seconds
Ansoft	2172	11
Cadence	2172	6
Mentor	2172	12
NetList (.Ckt/.END)	2172	11
NetList (.Ckt/.ENDS)	2172	11
NetList (.Cir/.ENDS)	2172	11
NetList Library	2172	14
S-Param (Shunt)	2172	28
S-Param (Series)	2172	28
Sigrity	2172	13
Simplis	2172	21
Touchstone Z	2172	23

For All Files

	All Types			.txt	.dcl (103)	.dml (103)
	PNs	Seconds	File Size (bytes)	File Size (bytes)	File Size (bytes)	File Size (bytes)
Ansoft	8518	48	340			
Cadence	5560	14		320	38 to 5.4k	8.7k to 245k
Mentor	8518	49	340			
NetList (.Ckt/.END)	8518	49	340			
NetList (.Ckt/.ENDS)	8518	46	340			
NetList (.Cir/.ENDS)	8518	45	340			
NetList Library	8518	57	5.4k to 200k (32 library files)			
S-Param (Shunt)	8518	106	**33k**			
S-Param (Series)	8518	106	**33k**			
Sigrity	8518	51	340			
Simplis	8518	74	400			
Touchstone Z	8518	97	**11k**			

Reducing File Counts

- Previous file generations used all possible Part Numbers available in KEMET Spice program.\
- Using “PartList.XLS” loaded with only those Part Numbers available though your company’s purchasing reduces the time to convert.
  - The PartList.XLS is initially loaded with 545 randomly selected Part Numbers.
  - Includes Aluminum, Ceramic, Film, and Tantalum part types.

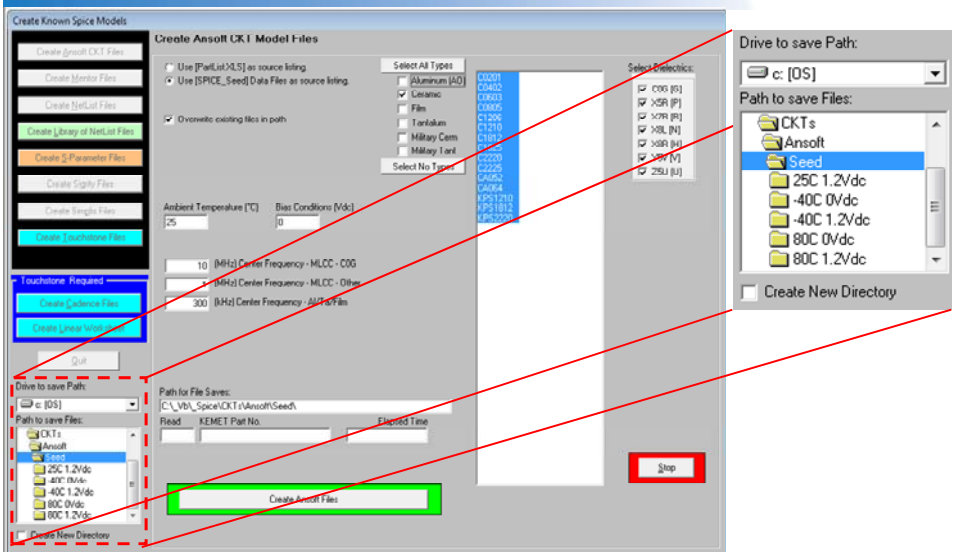
545 Part Numbers in PartList.XLS

	All Types			.txt	.dcl	.dml
	PNs	Seconds	File Size (bytes)	File Size (bytes)	File Size (bytes)	File Size (bytes)
Ansoft	545	7	340			
Cadence	123	2		310	22 to 156	822 to 17.6k
Mentor	545	8	340			
NetList (.Ckt/.END)	545	8	340			
NetList (.Ckt/.ENDS)	545	7	340			
NetList (.Cir/.ENDS)	545	7	340			
NetList Library	545	12	3k to 70k	(54 Library Files)		
S-Param (Shunt)	545	13	33k			
S-Param (Series)	545	12	33k			
Sigrity	545	8	340			
Simplis	545	8	400			
Touchstone Z	545	11	11k			

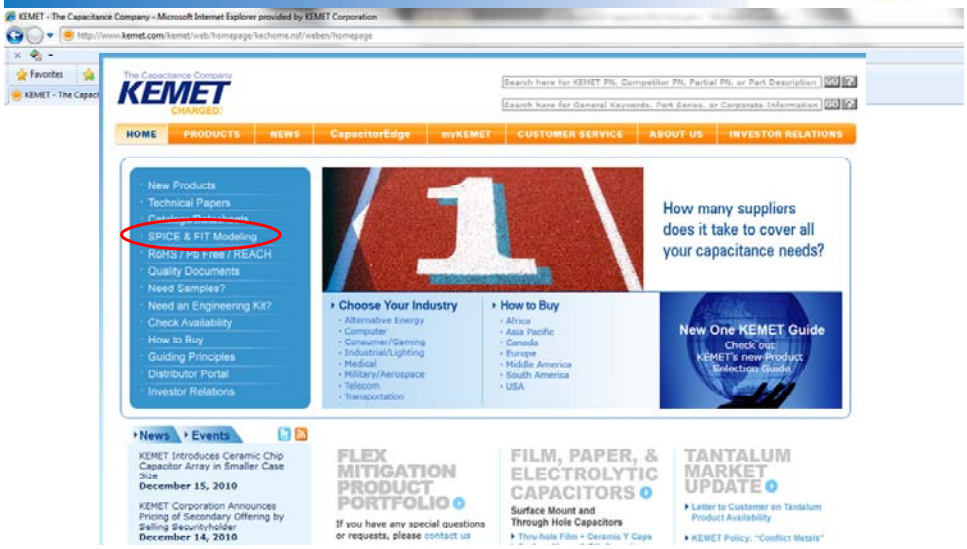
Files are Condition Specific

- Temperature is selectable (25Ð Default)
- DC Bias is selectable (0 Vdc Default)
- NetList types are frequency selectable
  - 100 kHz Alum, Film, Tant, and Ceramic >= 10 uF
  - 1 MHz Ceramic (100 pF < Cap < 10 uF)
  - 10 MHz Ceramic equal or below 100 pF
- Cadence, Linear are at self-resonance
- Frequency range is 6 decades with stop frequency selectable
  - 100 MHz Alum, Film, Tant
  - 1 GHz Ceramic
  - 10 GHz Ceramic equal or below 100 pF

Creating Models for Multiple Conditions



Files are accessed from Spice web page



Models in WEB

KEMET Net List Files

Models

The EDA model files as well as frequency listing of S-Parameter and Touchstone Impedance files follow.

Click here for Ansoft
Click here for Cadence
Click here for Mentor
Click here for NetList
Click here for S_Parameters
Click here for Sigrity
Click here for SIMPLIS
Click here for Touchstone

- **Models created using default conditions (0 Vdc and 25℃)**
- **Use "KEMET Spice" software to create using specific conditions**

Responding to Customer Requests

- The model formats are those requested by our customers.
- The formats created by the EDA vendors are not readily available.
  - Some vendors are extremely cooperative in assisting us to conform to their requirements.
  - Some vendors are reluctant to share, adopt, or verify the accuracy and acceptance of these models.

Capacitor Modeling Requirements in the 21st Century

TP – MP3

Steve Pytel, Ph.D.
Signal Integrity Product Manager,
ANSYS, INC.

Why Does It Matter to Simulation?

- Accurate prediction of plane impedances, board/package resonances, EMI/EMC, and effects on signal integrity
  - Capacitor values vary depending on temperature, biasing, manufacturing…
  - Parasitics of capacitors play a key role when trying to get the correct resonance
  - Layout can be key to obtain impedances in the micro-ohms

Important Considerations from Simulation Software

- **Modeling of the capacitor is key** whether a **Measured** model, **Equivalent Circuit** model, or **Field Solver** model
  - Was it measured in Series or Shunt mode?
    - Is there a preference (series?)?
  - What was considered in the model during the measurement?
    - Substrate loading effects?
    - Any additional interconnect (vias, traces, connectors, …)
  - What temperature was the model made at?
  - What biasing condition was the model made at?

Important Considerations from Simulation Software

- **Modeling of the capacitor is key** whether a **Measured** model, **Equivalent Circuit** model, or **Field Solver** model
  - Causality
    - A non-causal capacitor model used in a simulation will provide non-causal models for the board and package
      - Need to maintain Hilbert consistency between RL and CG
    - Can be the source for error when performing SPICE simulations accounting for PDN effects
    - Can be the source for non-convergence in the simulator whether field solver or SPICE

Important Considerations from Simulation Software

- **Modeling of the capacitor is key** whether a **Measured** model, **Equivalent Circuit** model, or **Field Solver** model
  - Capacitor arrays
    - Should this be modeled as an N-port device or a series of two port capacitors?
  - Low inductance caps
    - How to include layout effects in simulation software properly accounting for the capacitor model?

Moving Forward

1. Causal models
   - Parametric equivalent circuit models could be the answer for many questions
     - Enforcing causality/passivity
     - Accounting for temperature and voltage biasing
   - Could this be an IBIS like standard?
2. Part numbering specification that includes versioning
3. Standardization on measurement techniques
4. Standardization on a binary format for Touchstone models

Capacitor Modeling Requirements in the 21st Century

Panel Discussion

Bruce Archambeault, PhD
IBM Distinguished Engineer
IEEE Fellow

Capacitors have Many Applications

- Bulk Storage of charge
- Power/GND plane decoupling
  - Usually limited to ~400 MHz on PCB
- Filtering
- Series DC blocking for Gbit/sec links

Series DC Blocking for Gbit/sec Links

- Well known that PCB mounting has major impact at high frequencies
- ESL provided by vendors is a contributor
  - Usually an ideal value that is not achievable in real world PCBs
  - Measurement set up at vendor has a huge impact
  - Tolerances not well understood
    - Can have major impact of link performance
  - Variation with frequency?

High Speed Link Analysis

- Many long links do not have much margin for performance
  - Gets even worse as speeds increase
- Dependable models for inductance especially important
  - Frequency dependance
  - Tolerance

Inductance Models for Capacitors

- Standardize
  - Distance above return plane
  - Via separation
  - Frequency range
- Standardize data file format would be helpful
  - S/W tool vendors can easily read
  - More efficient/faster modeling

Thanks for your attention

ORACLE

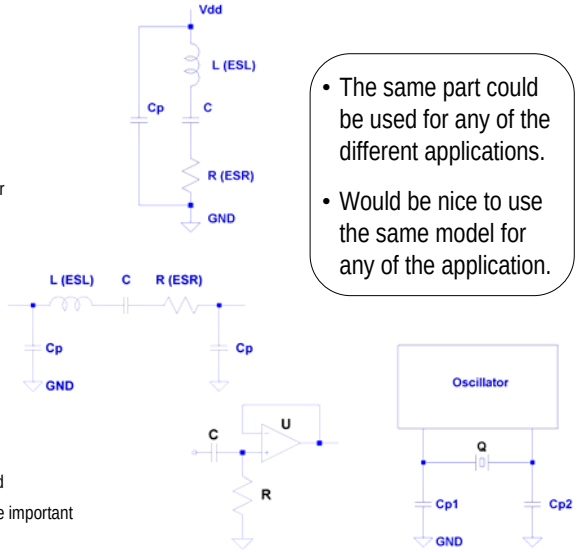
Capacitor Modeling – a User's Perspective

Istvan Novak

DesignCon 2011 TP-M3, January 31, 2011

Distinct Applications

1) Bypassing
   - part is between supply rails
   - parallel equivalent circuit
   - one port model
   - frequency range tends to be lower
   - body parasitic to GND does not matter
   - causality of model matters less
2) High-speed DC blocking
   - part is floating wrt GND
   - series equivalent circuit
   - two port model
   - body parasitic to GND is important
   - causality of model is important
3) Analog
   - part can be either floating or grounded
   - non-linear and second-order effect are important



- The same part could be used for any of the different applications.
- Would be nice to use the same model for any of the application.

The Challenges

The format (black-box: S, Z, or equivalent circuit)

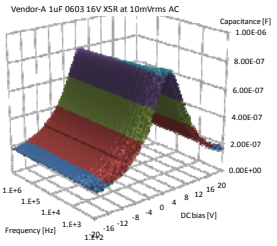
The frequency range (zero to infinite?)

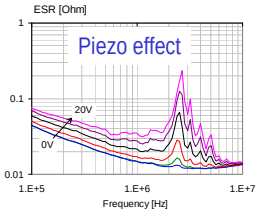
How to handle multi-terminal capacitors

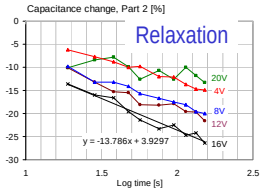
What variables/effects to include?

- tolerances
- user mounting geometry
- secondary resonances
- temperature
- DC-AC bias
- relaxation
- piezoelectric effect
- aging

DC bias







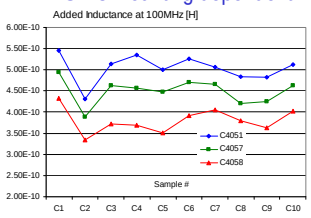
For details, see "DC and AC Bias Dependence of Capacitors", 13-TH2, DesignCon 2011
At www.electrical-integrity.com

The Problems

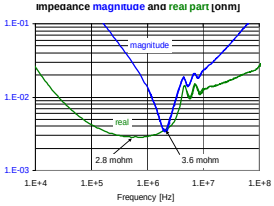
Some parameters are user-geometry dependent (ESL, also ESR), parallel shunt C

Unknown frequency range requirement

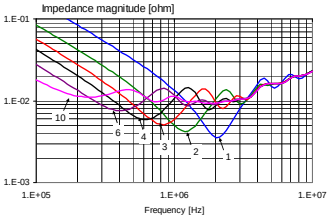
ESL is mounting dependent



Secondary resonances



ESR is mounting dependent



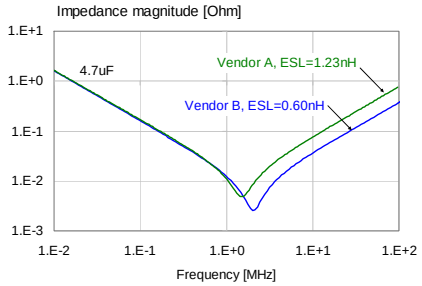
For more details, see
"Slow-Wave Causal Model for Multi Layer Ceramic Capacitors," DesignCon 2006
"Inductance of Bypass Capacitor," TF7 DesignCon West 2005
"A Black-Box Frequency Dependent Model of Capacitors for Frequency Domain Simulations," DesignCon East 2005
"Inductance of Bypass Capacitors," TF-MP2 DesignCon East 2005
"Frequency-Dependent Characterization of Bulk and Ceramic Bypass Capacitors," 12th Topical Meeting on Electrical Performance of Electronic Packaging, October 2003, Princeton, NJ
At www.electrical-integrity.com

The End-User's Wish List

- Flexible, user-defined ('infinite') frequency range
  - Automatically satisfied with equivalent circuits
- Causal model (for SerDes use)
- Same assumption for user geometry
- Optional secondary parameters
  - TC
  - aging
  - bias
  - nonlinear effects

For details, see "Inductance of Bypass Capacitors, Part 1", QuietPower columns At www.electrical-integrity.com

0805-size X5R 6.3V 4.7uF from two different vendors



The Way Out

Need standardization of models and characterization processes

ORACLE

THANK YOU

Istvan Novak,
istvan.novak@oracle.com