Determining PCB Trace Impedance by TDR: Challenges and Possible Solutions

Session 6-TA4
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Outline

• Introduction and Background
• Performance of Uniform Transmission Lines
• Manufacturing Variability
• Modeling and Potential Compensation
• Conclusions
• Introduction and Background

• Performance of Uniform Transmission Lines

• Manufacturing Variability

• Modeling and Potential Compensation

• Conclusions
Time Domain Reflectometry (TDR)

- High-speed interconnects must be designed for specified impedances
- Validation requires measuring the impedance
- Popular option to measure impedance is TDR
TDR Response of Uniform Loss-less Line

\[ \Gamma = \frac{Z_0 - Z_{\text{ref}}}{Z_0 + Z_{\text{ref}}} \]

\[ Z_0 = \sqrt{\frac{L_u}{C_u}} = \sqrt{\frac{L}{C}} \]

\[ t_{pd_u} = \sqrt{L_u C_u} \]

\[ t_{pd} = \sqrt{LC} \]
PCB Trace Validation

Is this trace OK?

Specification: 45 ohms +/- 10%
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Uniform Lossy Line

Conductor:

\[ Z_0 = \frac{R(f) + j\omega L(f)}{\sqrt{G(f) + j\omega C(f)}}; \quad \gamma(f) = \sqrt{(R(f) + j\omega L(f))(G(f) + j\omega C(f))} = \alpha(f) + j\beta(f) = \alpha + j\omega t_{pd} \]
Wide-band DeBye model used

With increasing frequency:
- Capacitance and inductance drop
- Resistance and conductance grow
Impedance and Delay of Uniform Lossy Line

- Wide-band DeBye model used
- As a function of frequency $Z_0$ has a shallow bath-tub shape
- With increasing frequency delay drops
Simulating a Uniform Lossy Line

W Element RLG C Model

All TDR responses should settle at \( Z_{\text{ref}} + R_{\text{DC}} \)

Wtest1 in2 0 out22 0 N=1 RLGCMODEL=W1 L=20
+ INCLUDEGDIMAG=YES
+ INCLUDERSIMAG=YES
* W-line model, values are per inch
.param Charimp1=50
.param Delayperinch1=160p
.param Lunit1='Delayperinch1*Charimp1'
.param Cunit1='Delayperinch1/Charimp1'
.param Rdcunit1=0.2
.param tandelta1=0.01
.MODEL W1 W MODELTYPE=RLGC, N=1
+ Lo = Lunit1
+ Co = Cunit1
+ Ro = Rdcunit1
+ Go = 0
+ Rs = 'Rdcunit1/10000'
+ Gd = 'Cunit1*tandelta1'
Uniform Lossy Line, Resistance Sweep

20-inch 50-ohm line
Ideal dielectric, Df = 0

20-inch 50-ohm line
Medium dielectric loss, Df = 1%

Resistance creates upslope.
AC resistance produces overshoot.
Dielectric loss reduces impedance!
AC resistance increases apparent impedance and creates a changing slope. With no AC resistance, TDR response climbs linearly to $Z_{\text{ref}} + R_{\text{DC}}$. 
Dielectric loss lowers apparent impedance.
After a fast initial drop, impedance drops slowly.
Uniform Lossy Line, Bandwidth

20-inch 50-ohm line  
Typical parameters

0.5-inch 40-ohm line  
Typical parameters

Lower bandwidth reduces horizontal resolution and slows response edge.
50-ohm line
Typical parameters

Envelope response can be used for any length of DUT
Uniform Lossy Line, Impedance

20-inch line
Typical parameters

Response shape is independent of DUT characteristic impedance as long as loss parameters stay the same
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Device Under Test, Connections

- Semirigid probe
- Ground vias
- Signal vias
- Precision 0402 50-ohm resistor
- Solder braid
- Differential wafer probe
- Signal vias

Total length: 17"
Same board, same trace measured multiple times.
- Same day with same calibration.
- Next day with old calibration.
- Next day with new calibration.
Very little variation was seen.
Six boards from two vendors
The same trace pair is measured
Same calibration, same probe
All traces follow the simulated signatures

N leg of diff pair is measured from left

P leg of diff pair is measured from left
P-N, Left-Right Variation

Two boards from the same vendor

TDR Impedance, Board1, Vendor A [Ohm]

P and N measured from left
Response has lower slope

Board 1
P and N measured from right
Response has higher slope

TDR Impedance, Board2, Vendor A [Ohm]

P and N measured from right
Response has lower slope

Board 2
P and N measured from LEFT
Response has higher slope
P-N, Left-Right Trends

Two boards from the same vendor
Different slopes from left-to-right vs. right-to-left!!!

TDR Impedance, Board1 [Ohm]

TDR Impedance, Board2 [Ohm]
VNA Measurements, Ports

Total length: 17”
Single Ended Reflections

Port 1
Port 2
Left
Right
Port 3
Port 4
N
N

S11 S33 magnitude [dB]

S22 S44 magnitude [dB]

Up to 10 GHz only small differences

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Differential Reflections

5-10dB difference in the 1-10 GHz range

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Transfer, Mode Conversion

Up to 10 GHz only small differences
Propagagation delay [s]

1. Propagation delay (left axis) and skew (right axis) [s]

- Delay:
  - Frequency [Hz]: 1.0E+07 to 1.0E+11
  - Propagation delay [s]: 2.75E-09 to 3.15E-09
- Skew:
  - Frequency [Hz]: 8.0E-12 to 1.6E-11
  - Skew values: 1.0E-11 to 2.0E-11

- Graphs show data for different frequencies and propagation delays.
Cross Sections, Dimensions

![Diagram of cross sections with labels a to l]

**Percent deviation from average:**

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<th>Location</th>
<th>b</th>
<th>d</th>
<th>c</th>
<th>f</th>
<th>g</th>
<th>k</th>
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<td>4.89</td>
<td>1.16</td>
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**Random!**
Cross Sections, Glass Weave

Same differential pair at two different locations. Glass-weave effect changes local Dk.
Estimated Deviation

TDR impedance and estimated deviation [Ohm, %]

Little correlation!
Even at DC, surface roughness matters.
Current will not (fully) penetrate the peaks.
For DC resistance purposes, copper thickness must be measured between lines across minima.

Measurement lines must be placed across minima.
Reasonable correlation is achieved only with copper thickness measured between lines across minima.
Each cascaded section follows its own trend.
The only interaction among sections is due to edge slow-down.
Even if specified as a uniform trace, its characteristic impedance could change or vary within the specified limits.
Simulations with ten cascaded uniform lines.
The characteristic impedance values step up or step down.
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• If the interconnect is uniform and its parameters are known, we know the TDR response.
• In long resistive traces the response has a positive tilt.
• The positive tilt can be approximated and subtracted from the measured response.
A linear estimate ignores the impedance increase due to AC resistance.

A linear estimate of the actual response still has large errors close to the excitation edge.

\[ y = 1.00E+09x + 4.53E+01 \]
A sixth-order polynomial captures the time-dependent impedance with sufficient accuracy. Lines are undistinguishable.

Subtracting the estimated response from the measured TDR curve. Trace is within +1.5 -0.5% of nominal.

TDR impedance [ohm]
Conclusions

- Long and/or resistive traces have significant difference between actual and apparent impedance.
- Apparent impedance is increased with increasing DC and AC resistances.
- AC resistance creates overshoot beyond the DC resistance value.
- Apparent impedance is decreased by dielectric loss.
- DC resistance is increased by surface roughness.
- Thin 20-40” traces may have apparent impedances go outside the tolerance window.
- In PCB manufacturing, resistive panel coupons need compensation.
- In full-board validations, TDR results need compensation.
- A sixth-order polynomial is suggested to compensate for losses.
• TDR has been used for decades to check trace impedance.

• Why was this not a problem earlier?

Because we used lossier dielectrics, wider and heavier traces and maybe shorter etches…
THANK YOU!

Any Questions?

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