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Does skew really degrade SERDES performance?

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Abstract

As the speeds of multi-gigabit interconnects continually increase, concerns have been growing about passive channel skew. Many publications have explained the sources of skew and its consequences, but does skew really matter when it comes to performance of practical SERDES channels? Can we mitigate performance degradation due to skew by adapting transmitter/receiver equalization settings? In this paper we look at the impact of skew on SERDES performance using measurements where we introduce controlled skew in fine increments at multiple bit rates. We show correlation between these measurements and end-to-end simulations.

Authors Biographies

Shirin Farrahi is a Hardware Engineer at Oracle. She is engaged in the design and characterization of high-speed signal interconnects for high-performance server systems. She received her Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

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Ying Li is a Senior Hardware Engineer at Oracle Corporation where she works on signal and power integrity of ASIC packaging interconnects simulation and measurement validation. In previous graduate studies, her research work focused on computational electromagnetics, sensitivity analysis and optimization. She received her Masters degree in electrical engineering from McMaster University. She is pursuing her Ph.D. degree at University of Washington.

Xun Zhang is a Principle Hardware Engineer at Oracle. Her work focuses on high-speed SerDes architecture development, link modeling and circuit design specifications. Before joining Oracle, she had been working at LSI Corporation as a system architect for 8 years, where she was responsible for servo IP development for high density magnetic recording channels. She got her PhD from Carnegie Mellon University in 2006, and master's degree from Shanghai Jiaotong University in 2001, both specializing in communications and signal processing areas.

Gustavo J. Blando is a Principle Hardware Engineer with over twenty years of experience in the industry. Currently at Oracle Corporation, he is leading the SI/PI team and responsible for the development of new processes and methodologies in the areas of broadband measurement, high speed modeling and system simulations. He received his M.S. from Northeastern University.

Istvan Novak is a Senior Principle Engineer at Oracle. Besides signal integrity design of high-speed serial and parallel buses, he is engaged in the design and characterization of power-distribution networks and packages for mid-range servers. He creates simulation models, and develops measurement techniques for power distribution. Istvan has twenty plus years of experience with high-speed digital, RF, and analog circuit and system design. He is a Fellow of IEEE for his contributions to signal-integrity and RF measurement and simulation methodologies.

I. Introduction and Background

Passive skew has been one of the most discussed issues for high speed serial signaling and to a lesser extent for parallel signaling. Skew is primarily caused by asymmetries in the differential signal routing [1 -6], fiberglass weave effect [7], [9 - 11], periodic loading [8] and PCB manufacturing limitations. Reducing skew is very important for reducing signal degradation, mode conversion, EMC problems, and link failures. Skew can be mitigated using many different strategies. It is possible to reduce skew by reducing asymmetries in the design. Length differences can be compensated by opposite turns [1] or with a rectangular bulge on one leg [1], [12], [13]. Via asymmetries can be compensated by tight control of via stub lengths [1] or by reducing asymmetric GND via configurations [5]. Fiberglass weave effect on skew can be minimized by using multi-ply materials, angled routing, or using tighter pitch and thinner glass weaves [1], [7], [14].

Even though there are a number of ways to counter skew, it cannot be eliminated completely. As data rates for multi-gigabit interconnects are increasing at a very fast pace, bit times continue to drop significantly. In these situations, PCB skew could almost be equal to the bit time. The consequences of such high skew can be very alarming, causing the received eye at the input to be completely closed. Even for relatively low speed operation, it is possible that skew can introduce a half wave resonant frequency which is close to the operating frequency. How do we handle this skew? What is the maximum skew that a design can tolerate? How capable are SerDes devices of minimizing the impact of skew? At the end of the day, how important is to control passive skew on boards to the overall high speed SerDes / channel operation? Also, the techniques mentioned above in controlling the PCB routing and materials for reducing skew might be expensive. Do we really need to adopt all those techniques to achieve tolerable skew and Serdes performance?

In this paper, we devise a test plan to show how skew impacts SerDes performance. A test board that has a SerDes controller is connected to a compliance card that has variable etch lengths. The driver and the receiver are on the same controller and the channel is connected in a loopback mode. To induce controlled skew between the legs of the differential pair, we use adjustable delay lines. These delay lines have the capability to delay the signal by specific increments using mechanical turns on the device. The driver and receiver have equalization capabilities and the settings are adaptive to achieve best performance. We will see how the SerDes performance changes as the skew is increased. We will also show the simulations for the same channel and the correlation between our simulation and measurement.

Simulations at a higher speed of 25.6 Gbps, in addition to the measurements of 12.8 and 19.2 Gbps, are shown to understand the trend of how the performance is impacted as skew increases.

II. Anatomy of passive skew

To analytically describe the effect of skew, we can look at an expression for differential insertion loss

$$S_{dd12} = \frac{S_{13} - S_{14} - S_{23} + S_{24}}{2}$$

where we define the single ended ports as shown below on the left and S_{dd12} is the differential insertion loss with the ports defined on the right

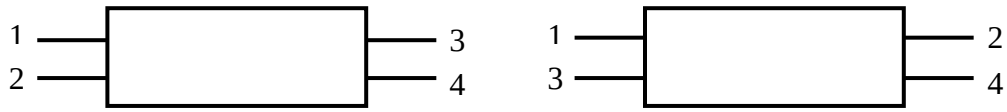


Figure 1*: Port ordering for single-ended (left) and differential (right) s-parameters*

Let's assume that $|S_{13}| \cong |S_{24}| = |IL(f)|$ and $|S_{14}| \cong |S_{23}| = |X(f)|$ where IL is the insertion loss and X is the cross-coupling of the channel. We know that $S_{xy} = |S_{xy}|e^{j\theta_{xy}}$. Therefore we can rewrite the above expression as

$$S_{dd12} = \frac{|S_{13}|e^{j\theta_{13}} + |S_{24}|e^{j\theta_{24}} - |S_{14}|e^{j\theta_{14}} - |S_{23}|e^{j\theta_{23}}}{2}$$

$$S_{dd12} = \frac{|IL|}{2}\left(e^{j\theta_{13}} + e^{j\theta_{24}}\right) - \frac{|X|}{2}\left(e^{j\theta_{14}} + e^{j\theta_{23}}\right)$$

Assuming that the cross-coupling in the channel is significantly smaller than the insertion loss ($|X| \ll |IL|$), we can simplify the above expression to

$$S_{dd12} = \frac{|IL|}{2}\left(e^{j\theta_{13}} + e^{j\theta_{24}}\right)$$

To represent channel skew, let us define $\theta_{13} = \theta + \frac{\Delta\theta}{2}$ and $\theta_{24} = \theta - \frac{\Delta\theta}{2}$. Using Euler's equation and trigonometric identities, we can simplify our expression to

$$S_{dd12} = |IL|\cos\left(\frac{\Delta\theta}{2}\right)e^{j\theta} \quad (1)$$

which shows that the skew of the angle, $\Delta\theta$, modulates the insertion loss amplitude. The frequencies at which we will see notches in the differential insertion loss correspond to values of $\cos\left(\frac{\Delta\theta}{2}\right) = 0$. For integer values of n these will correspond to

$$\left(\frac{\Delta\theta}{2}\right) = \frac{(2\mathrm{n} - 1)\pi}{2}$$

Since frequency $f = \frac{\Delta\theta}{\Delta t}$, $\frac{\Delta\theta}{2} = 2\pi f \Delta t$, where Δt corresponds to the amount of skew. Therefore the frequencies at which we will see resonant notches are given by the following expression:

$$f = \frac{2n-1}{2\Delta t}$$

This result is shown in the insertion loss plot in *Figure 2* for two models with and without skew.

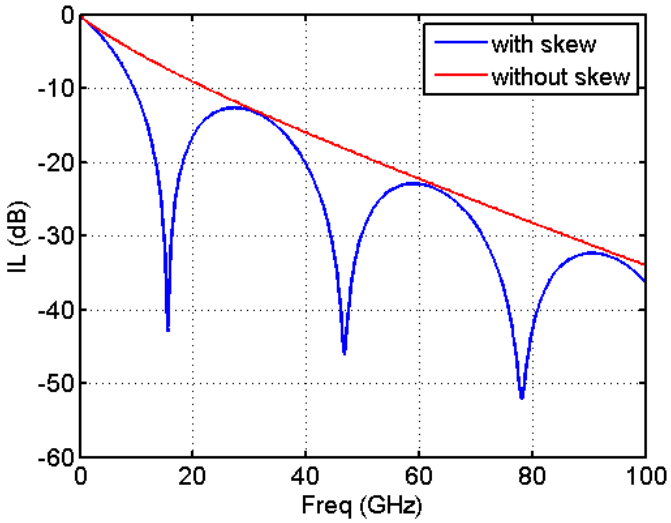


***Figure 2**: Differential insertion loss for transmission lines with and without skew (Δt = 30 ps)*

III. Description of test setup

Measurements

In the previous two sections we talked about the sources of skew, how to minimize skew and how to calculate skew from equations. Now we will look at the impact of the skew on the performance of SerDes channel. To understand this, we created a test setup to introduce controlled skew in the channel, measure the signal at the receiver, and look at the equalization settings as skew varies. *Figure 3* shows the setup used in the measurements. The channel is a loop-back from the transmitter to the receiver of the same test board. A compliance card with varied etch lengths is connected to control the channel length. The adjustable delay lines shown in the channel are used to induce skew between the positive and negative legs of one differential channel in a controlled manner.

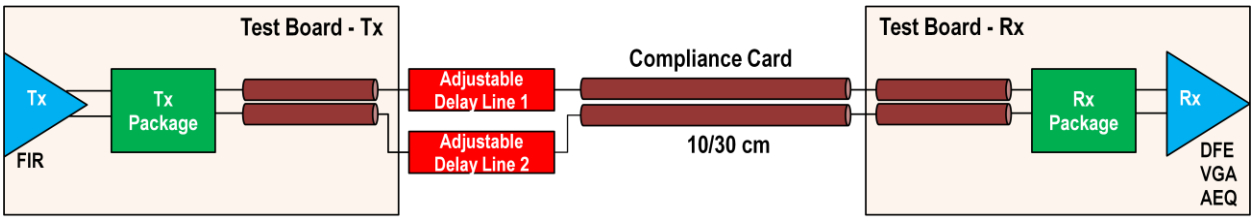


***Figure 3**: Block diagram of the SERDES channel that includes the test board, adjustable delay lines and the compliance card*

The adjustable delay lines have a multi-turn mechanism to manually adjust the delay with very low insertion loss over a wide range of frequencies [10]. Using two of the delay lines, one for each leg of the differential channel as shown, we can induce controlled amounts of known skew in the differential signal. The delay line on the P-side is fixed while the N-side delay line is varied with 1 turn increments to increase the skew. When both the delay lines are set to the same number of turns the skew is approximately zero. As we increase the number of turns on N leg, the skew increases around 5.5 ps per turn. In *Figure 4*, we can see how the skew varies for each turn. When the number of relative turns is 6, the skew is around 34 ps. The differential insertion loss is shown in *Figure 5* where we see that at low frequencies the adjustable delay lines have very low insertion loss. Using the equation of calculated resonant frequency versus skew in section II, the resonance frequency moves lower as skew increases.

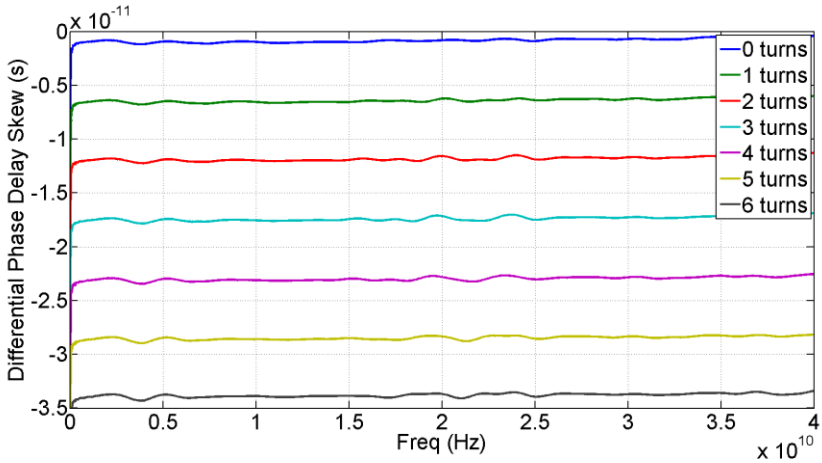


***Figure 4**: Differential skew Vs Frequency as the relative turns of delay lines vary*

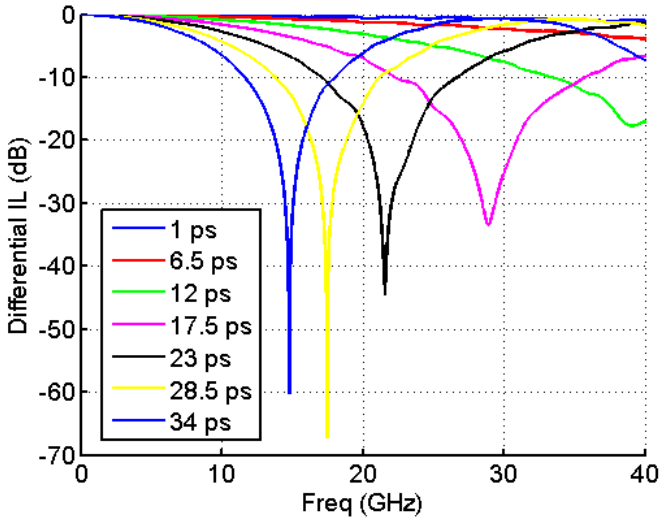


***Figure 5**: Differential insertion loss for varying amounts of skew*

To understand the impact of skew, we looked at different cases with different combinations of Serdes speeds and channel etch lengths. The compliance card has etch lengths of 10 cm (4") and 30 cm (12"), and the speeds of operation are 12.8 and 19.2 Gbps. For each combination of length and speed, the skew is varied from 1 ps to 34 ps. The driver uses a 3-tap FIR filter for transmitter

equalization and the receiver implements 10-tap decision feedback equalizer (DFE) along with analog equalizer (AEQ) and variable gain amplifier (VGA).

The transmitter FIR taps are chosen such that the received eye has good margins when there is no introduced skew from the adjustable delay lines. As the skew changes, the receiver adapts and optimizes all the equalization parameters to get the best resulting eye. *Table 1* gives a quick overview of how the parameters change with skew for two extreme cases of speeds and lengths.

Parameters	12.8 gbps, 10 cm, 1 ps skew	19.2 gbps, 30 cm, 34 ps skew
VGA	7	12
AEQ	6	15
DFE - H0	24	24
DFE - H1	4	20
FIR – CO	315 mV	315 mV
FIR – C-1	15 mV	15 mV
FIR – C+1	0 mV	0 mV
Eye Height (mV)	193	44.1
Eye Width (UI)	0.623	0.287

***Table 1**: Equalization parameters as skew, speed and length vary. Eye width and height also shown*

The passive channel was measured end to end including the package on either side. To facilitate the measurement at the package bump, the chip is milled down to the package so that all the bumps of the package were visible and clear to probe. The channel was setup on the probe station using 150 µm single ended wafer probes. The frequency response of the channel with varying skew is measured using a 50GHz Vector Network Analyzer [12]. *Figure 6* shows the differential insertion loss for 10 cm and 30 cm channels with variable skew. You can clearly see how the half wavelength resonance moves toward lower frequency as the skew increases.

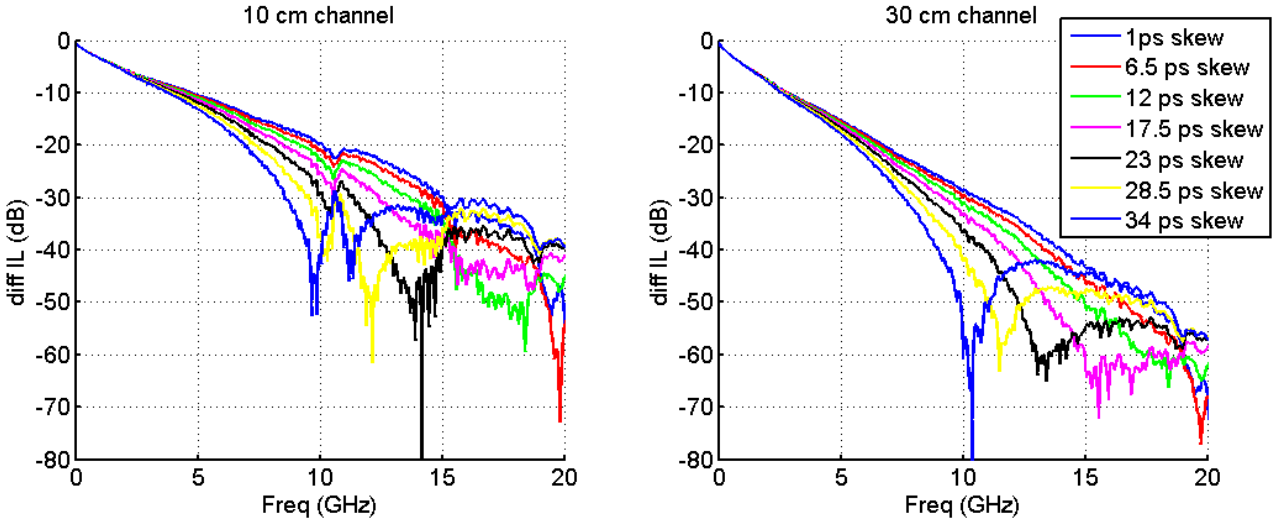


***Figure 6**: Differential insertion loss vs frequency for varying amounts of skew*

TDR plots of the impedance measurement show that the impedance variation for skew variance is very minimal. See *Figure 7* for impedance plots of the short channel. The part of the channel where

adjustable delay lines are located is circled in the plot. From the zoomed version of the impedance plot at the location of delay lines, we see the change in TDR due to skew.

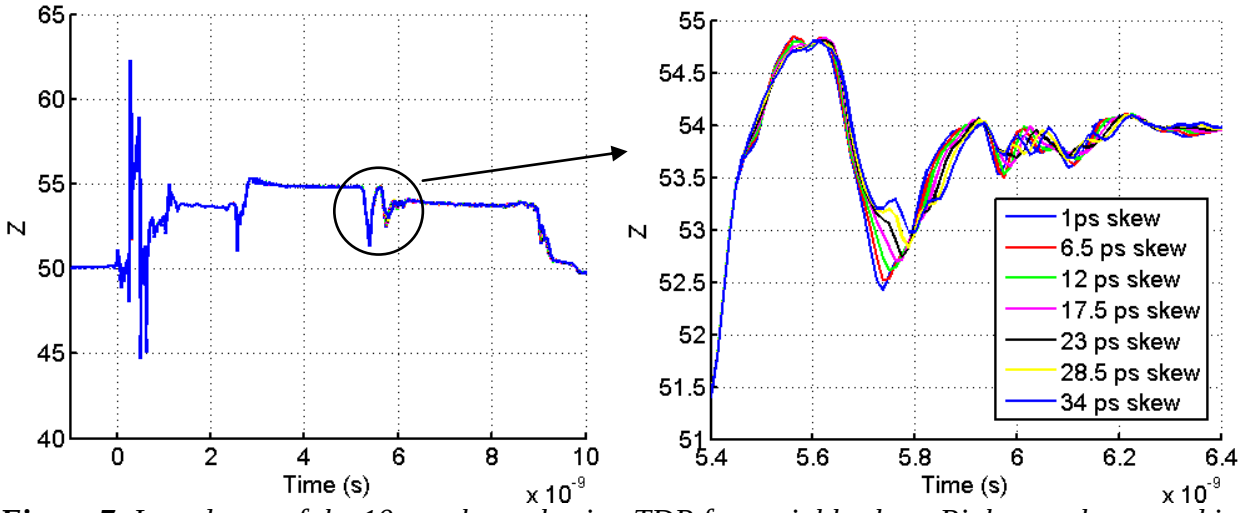


***Figure 7**: Impedance of the 10 cm channel using TDR for variable skew. Right panel: zoomed in at the point where the impedance varies with skew*

Simulations

We performed simulations of our test setup using IBIS-AMI models of the driver and receiver provided by the manufacturer and measured models of the channel (as described above). We performed our simulations using a Matlab-based IBIS-AMI simulator created in-house. Before proceeding with all simulations, we verified our simulation results against an industry-approved standard IBIS-AMI simulator [11]. As shown in *Figure 8*, the results from our in-house simulation tool agree with those obtained from this tool.

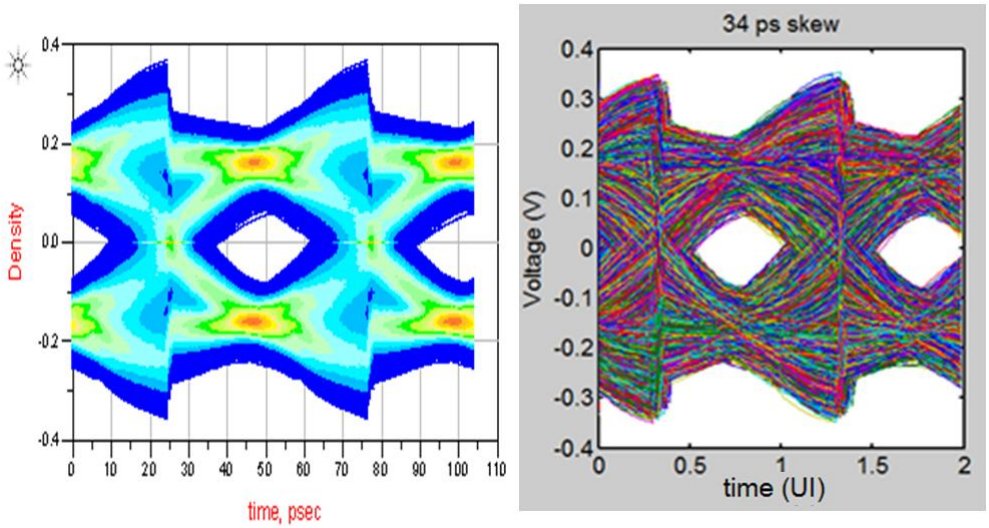


***Figure 8**: Eye diagrams from simulations in an industry standard simulator (left) and our Matlab-based IBIS-AMI simulator (right) using the 10 cm channel length at 19.2 Gbps with 34 ps skew*

The simulations were performed using a 2 million bit PRBS 31 pattern. The driver FIR settings were selected to match those from our measurement results (C_0 = 315mV, C_{-1} = 15mV, and C_{+1} = 0mV). The receiver process, temperature and voltage were set to typical. The remaining receiver settings were adapted by the IBIS-AMI model as shown in *Figure 9*. The size of the data block used in these simulations was 20,000 samples. We can see from *Figure 9* that the model parameters settled to their final values within roughly 500 data blocks. The tap settings reported in the remainder of this paper were taken after the tap values had settled.

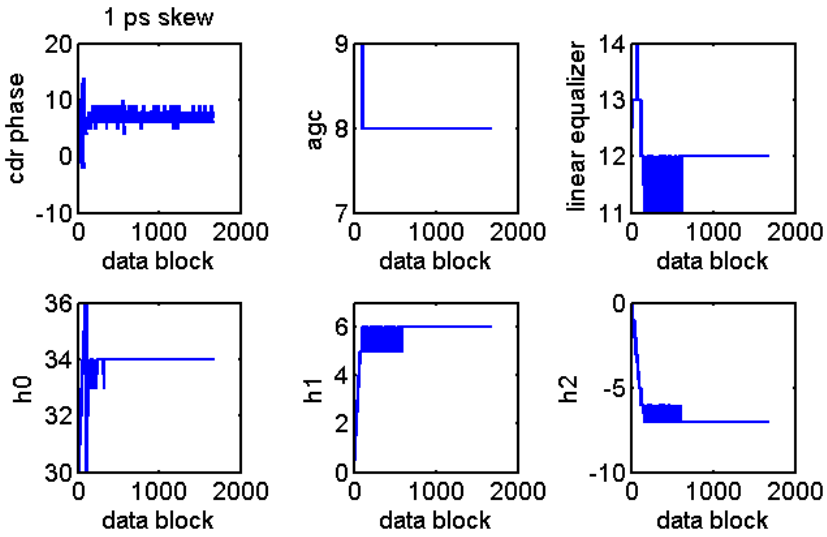


***Figure 9**: Example showing IBIS-AMI receiver model parameters adapting to the input signal*

The output waveform was used to plot eye diagrams. To determine the bit error rate (BER), the output waveform was sampled at various vertical and horizontal points, and the resulting bit streams were correlated with the input bit pattern. By seeing which sampling points are closest to a bit error rate of 10-8, we estimated the eye height and width for this target BER. Since we used two million bits for our simulations, we extrapolated our BER estimates using a 3rd order polynomial.

IV. Results

The eye measurements at the receiver show that the eye is degraded as skew increases. Since the receiver is capable of adapting to the received signal, the signal quality is improved by the automatic adjustment of the equalizers' parameters. *Figure 10* shows the eye contours as skew varies from 1ps to 34 ps for a 30 cm channel operating at 19.2 Gbps. You can see the eye envelope shrinking as the skew increases. The eye envelopes for different skews are overlaid in *Figure 11* to visualize the eye degradation at a BER of 1e-8. We can see that the eye is not closed even when the skew is so high (34 ps is more than 60% of the UI at 19.2 Gbps). This shows that the receiver is capable of improving the input signal by adapting towards the optimal equalization parameter values.

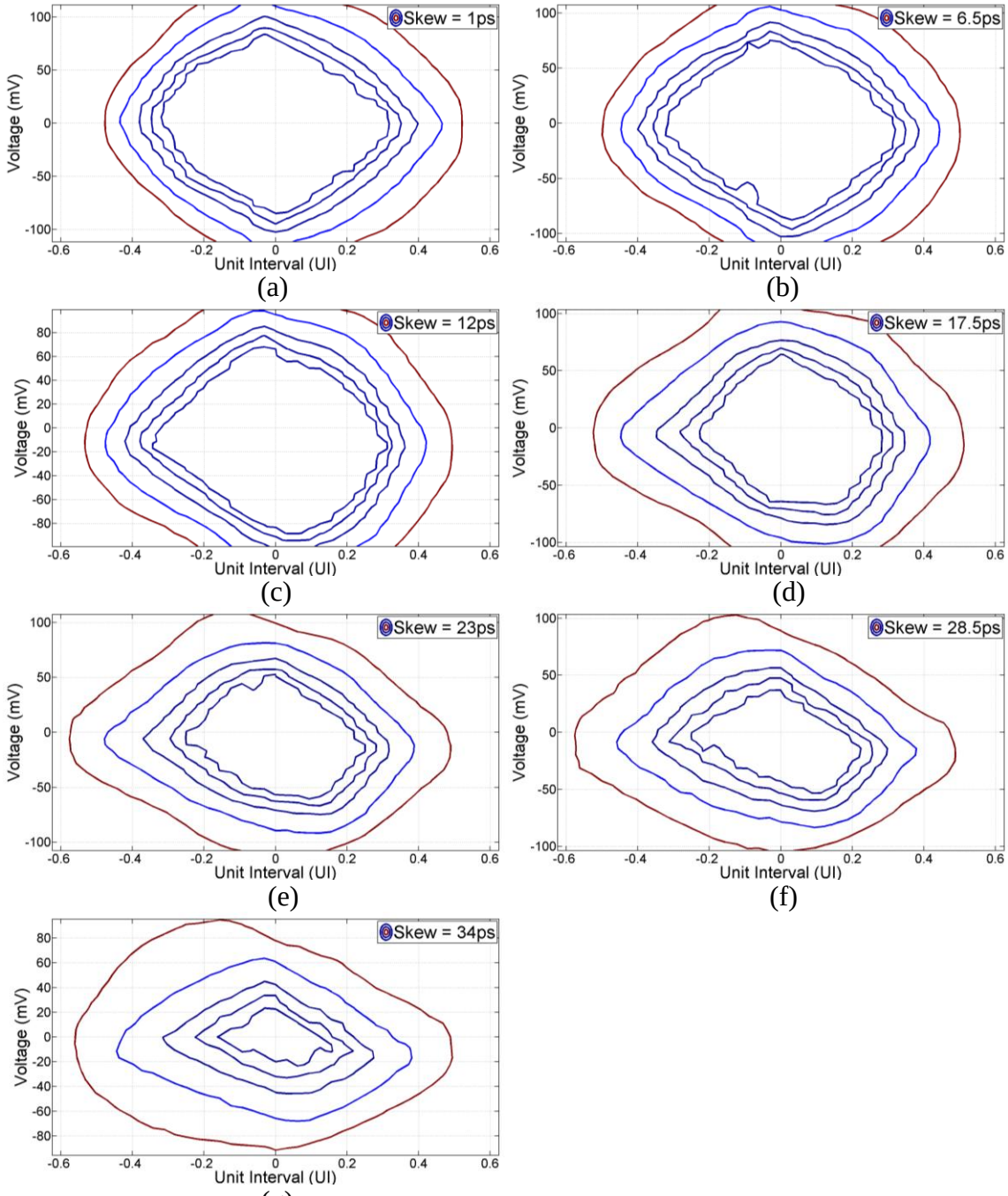


***Figure 10**: Eye contours for the input signal at the receiver for different amounts of skew. The speed of operation is 19.2 Gbps for the 30 cm channel (a) 1 ps (b) 6.5 ps (c) 12 ps (d) 17.5 ps (e) 23 ps (f) 28.5 ps (g) 34 ps*

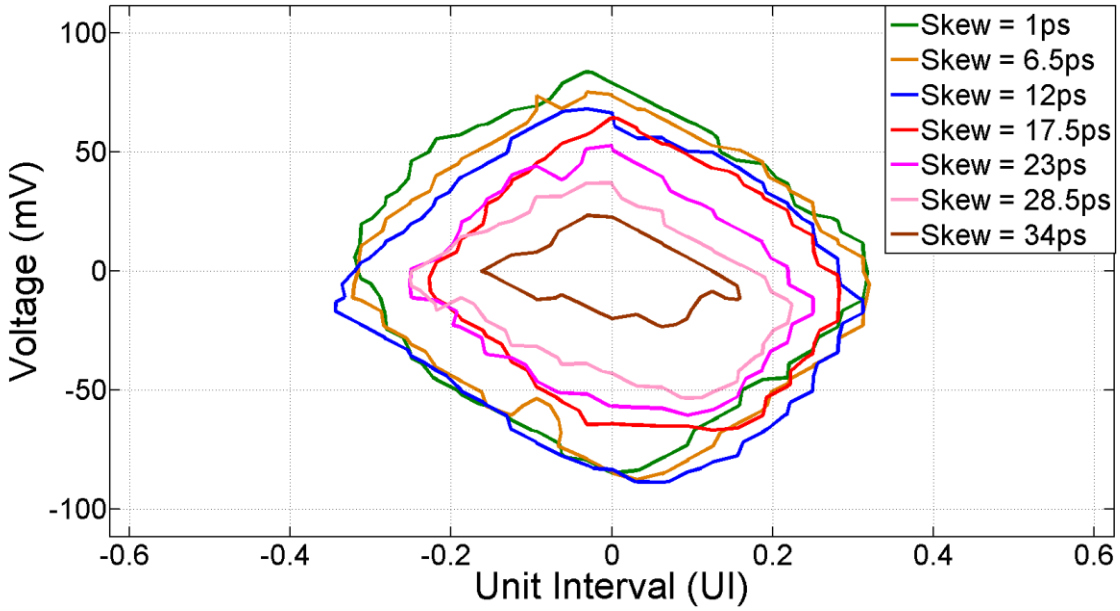


***Figure 11**: Inner eye envelope for the signal at the receiver output for different amounts of skew. The speed of operation is 19.2 Gbps for the 30cm channel @ BER 1e-8*

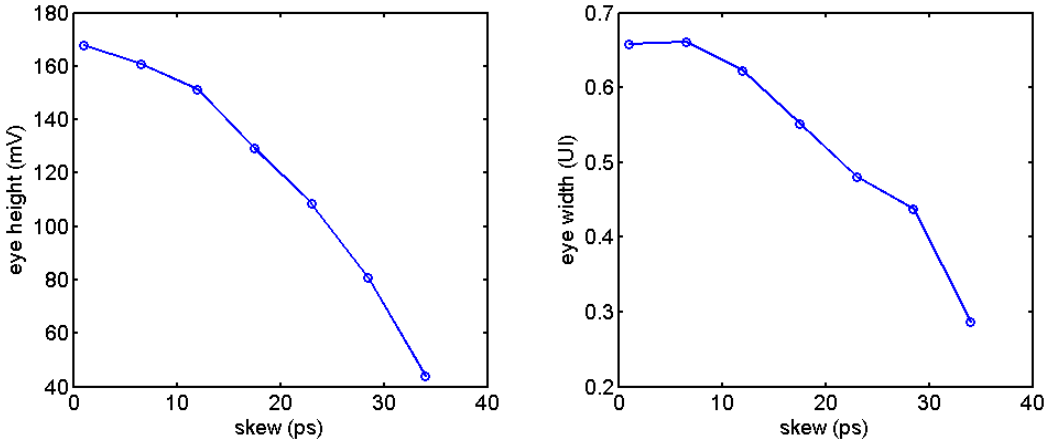


***Figure 12**: Eye dimensions for various amounts of skew. The speed of operation is 19.2 Gbps for the 30cm channel*

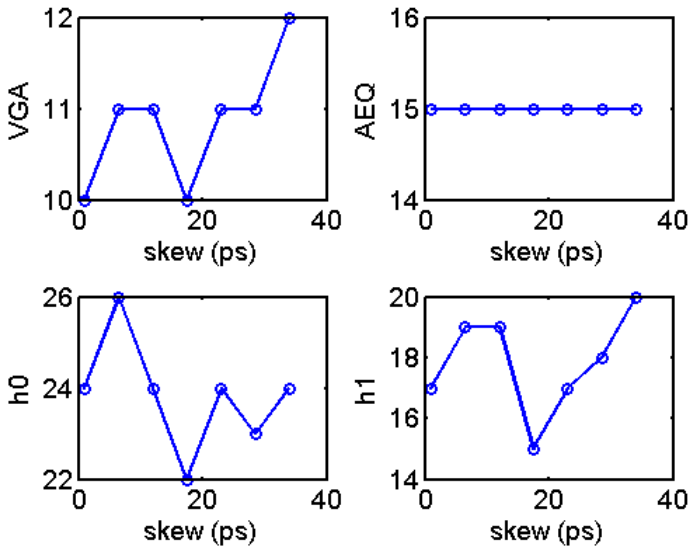


Figure 13*: Measured receiver tap settings for various amounts of skew. The speed of operation is 19.2 Gbps with the 30cm channel*

Measurement and Simulation Correlation

In *Figure 14*, we are showing plots for of eye height and width for our measurements and simulations at two data rates (12.8 and 19.2 Gbps) and two compliance card lengths (10 and 30 cm). We see that although the absolute value of simulated eye widths and heights are in some cases different from the measured values, the trends with increased skew are in general the same. The absolute eye dimension differences could be due to differences between the IBIS-AMI model compared to the actual performance of the SerDes, and the differences in the BER estimation algorithm that we use for obtaining eye dimensions at a target BER. It could also come from measurement inaccuracy of the passive channel VNA measurements, the process corner of the chip and temperature and voltage variations. Our goal in this study was not to obtain perfect correlation between simulation and measurement but to confirm both indicate the same general trends of Serdes performance vesus skew. With this level of correlations, we validated our simulation model, and it allows us to study the effect of skew in a wider variety of cases which may not be available or feasible for measurements.

We monitored the receiver's tap settings as they adapted to our measured and simulated signals with increasing skew. As can be seen from *Figure 15*, the ratio h1/h0 and adapted AEQ value increases with skew. Both indicate that skew causes more insertion loss. Compared with the eye dimensions shown in *Figure 14*, it is clear that performance starts to deteriorate when AEQ gets close to saturation.

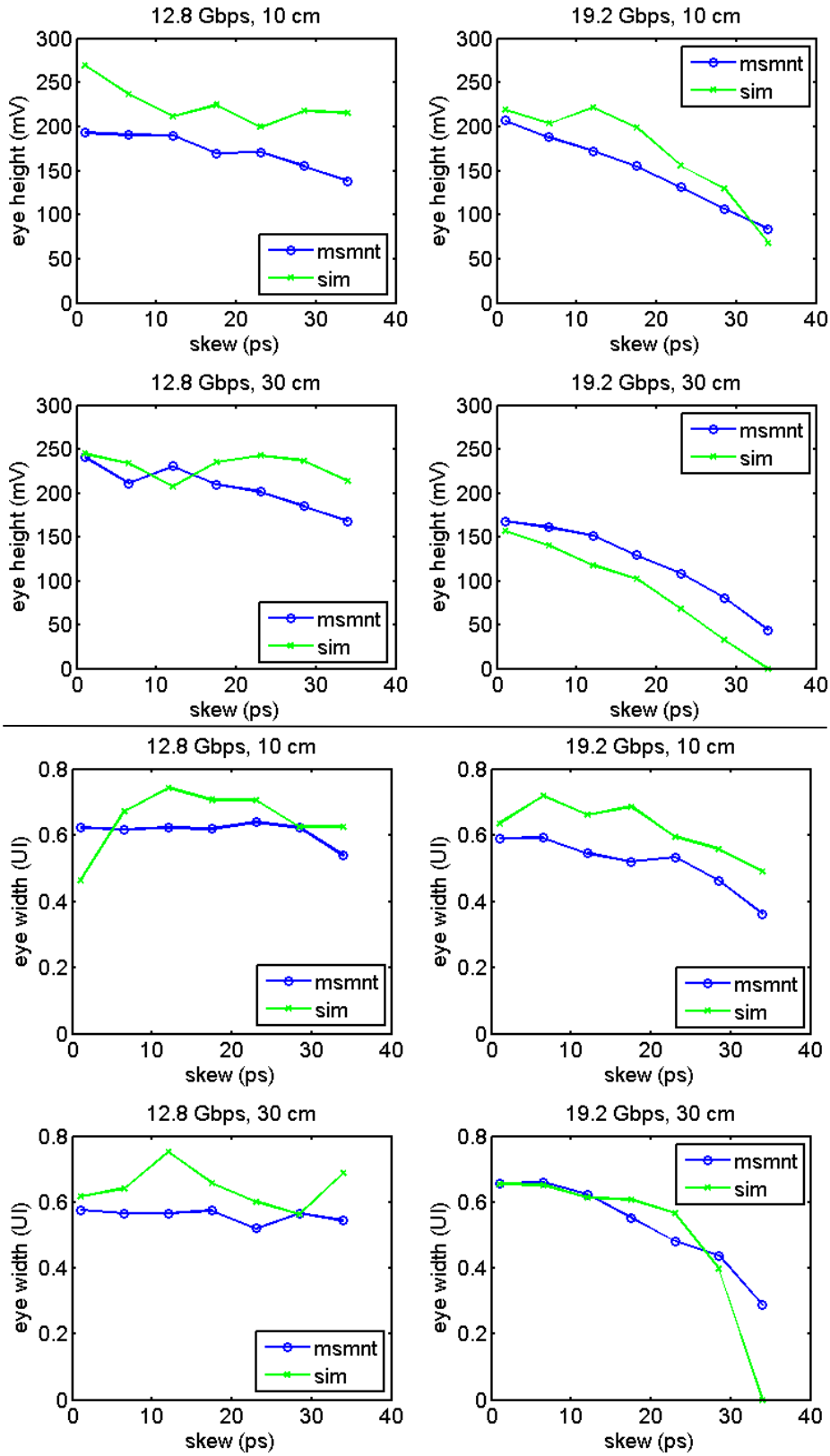
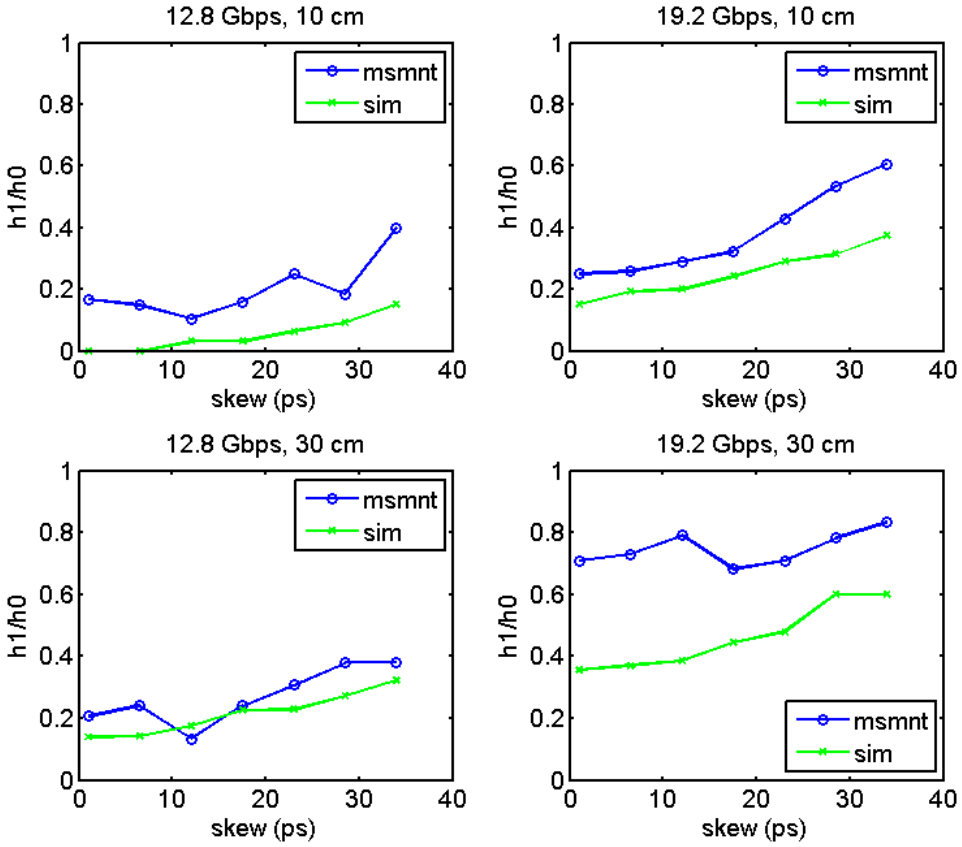


***Figure 14**: Measured and simulated eye dimensions for various amounts of skew. All four conditions are shown: two data rates (12.8 and 19.2 Gbps) and two channel lengths (10 and 30 cm)*


12.8 Gbps, 10 cm
19.2 Gbps, 10 cm
12.8 Gbps, 30 cm
19.2 Gbps, 30 cm
msmnt
sim
h1/h0
skew (ps)

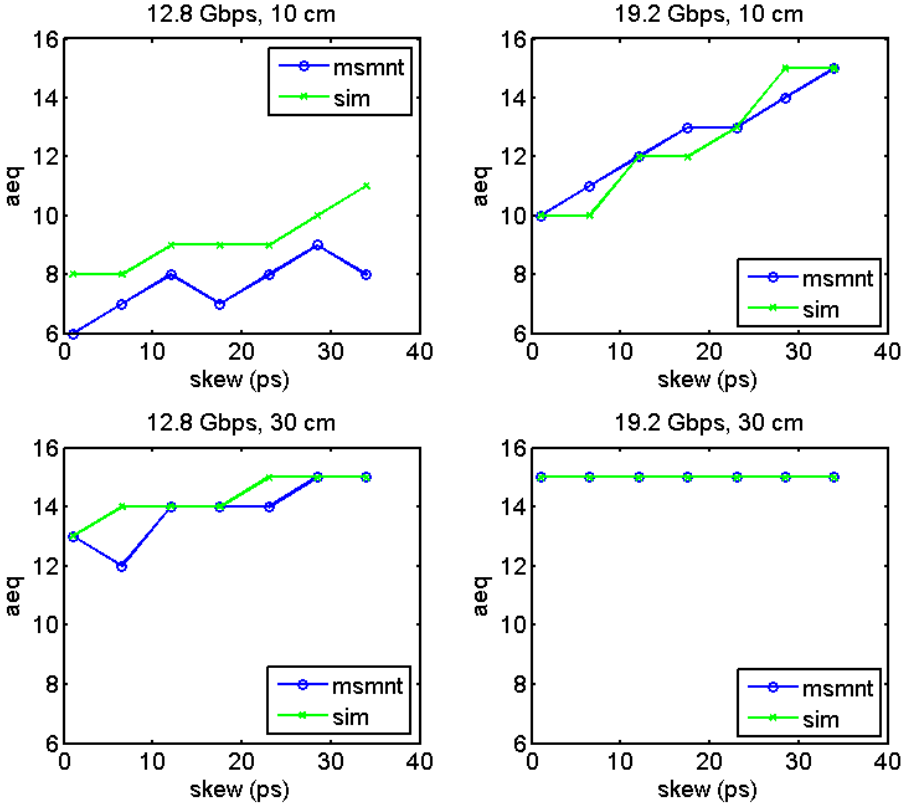

12.8 Gbps, 10 cm
19.2 Gbps, 10 cm
12.8 Gbps, 30 cm
19.2 Gbps, 30 cm
msmnt
sim
aeq
skew (ps)

***Figure 15**: Measured and simulated tap values for various amounts of skew. All four conditions are shown: two data rates (12.8 and 19.2 Gbps) and two channel lengths (10 and 30 cm)*

To help us understand the impact of skew on the channel that the receiver is seeing, we also ran our simulations using a single pulse input. *Figure 16* shows the pulse response at the input of the receiver including the driver IBIS-AMI model and the receiver model load. We see that as skew increases, the pulse response amplitude decreases, and the pulse gets wider. These changes are similar to the changes we expect in a pulse response as the channel loss increases. We see greater loss and slightly more impact due to increased skew at the higher data rate. This makes sense since at the higher data rate we have a smaller pulse width. For the same amount of actual skew, this means that the relative impact of skew on performance is more significant.

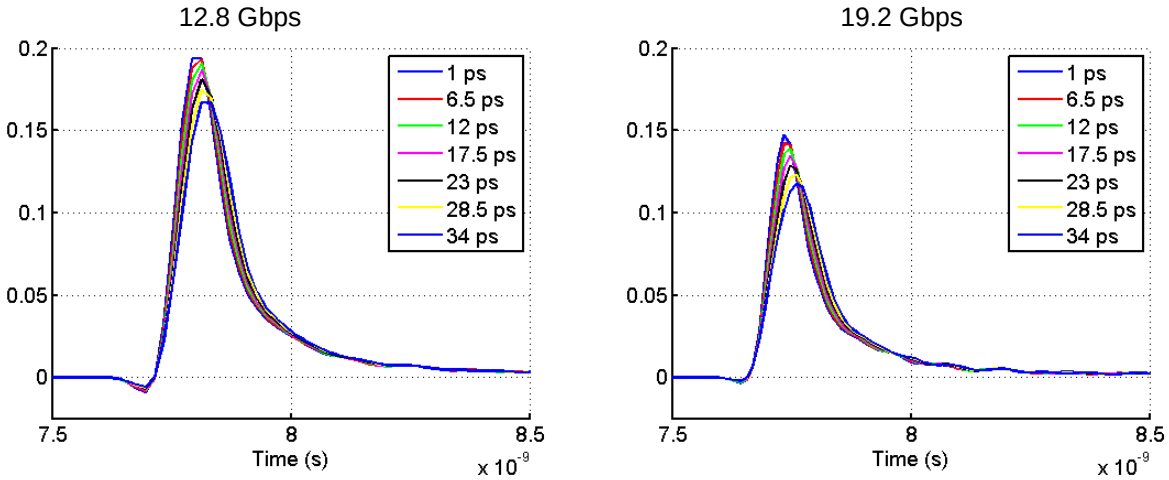


***Figure 16**: Simulated pulse responses at the input to the receiver of channels with varying skew at using 10 cm etched channel length*

Skew Translates to Insertion Loss

Besides insertion loss, skew also has many other negative impacts on channel performance, such as extra mode conversion and crosstalk, but in our test cases none of those seemed to affect our results very much. Considering that such high levels of skew have not broken our SerDes receiver, we can take the view that additional skew as a first order effect translates to additional insertion loss as shown in *Figure 6* and predicted in equation (1). To test this hypothesis we simulated two channels with no skew but different amounts of insertion loss at 10 GHz. As shown in *Figure 17*, the first channel has roughly 20 dB of loss at 10 GHz while the second channel has 30 dB of loss at this frequency. These two channels are imitating the cases with 1 ps and 23 ps of skew from our earlier measurements and simulations using the 10 cm etch length.

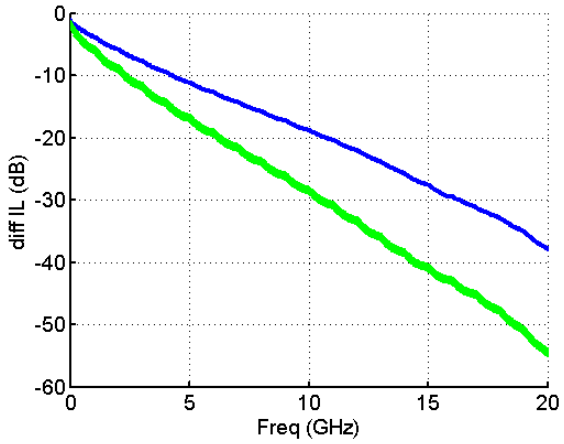


***Figure 17**: Channels with varying loss but no skew*

Our simulations at 19.2 Gbps in these two cases show quite similar results to the measurements due to added skew. Namely, in the lossier case the eye width and height decrease by roughly 20%. The decrease in eye height is comparable to what we observed in the case of 23 ps of added skew at 19.2 Gbps. In the case of added loss but no skew the eye width decreases by roughly the same amount as the eye height; whereas, in the case of added skew the eye width does not change as significantly. Looking at the phase delay of these four models (not shown), we see that in the case of added skew, the phase of the insertion loss does not change, but in the case of added loss, the phase delay changes significantly, resulting in the decreased eye width.

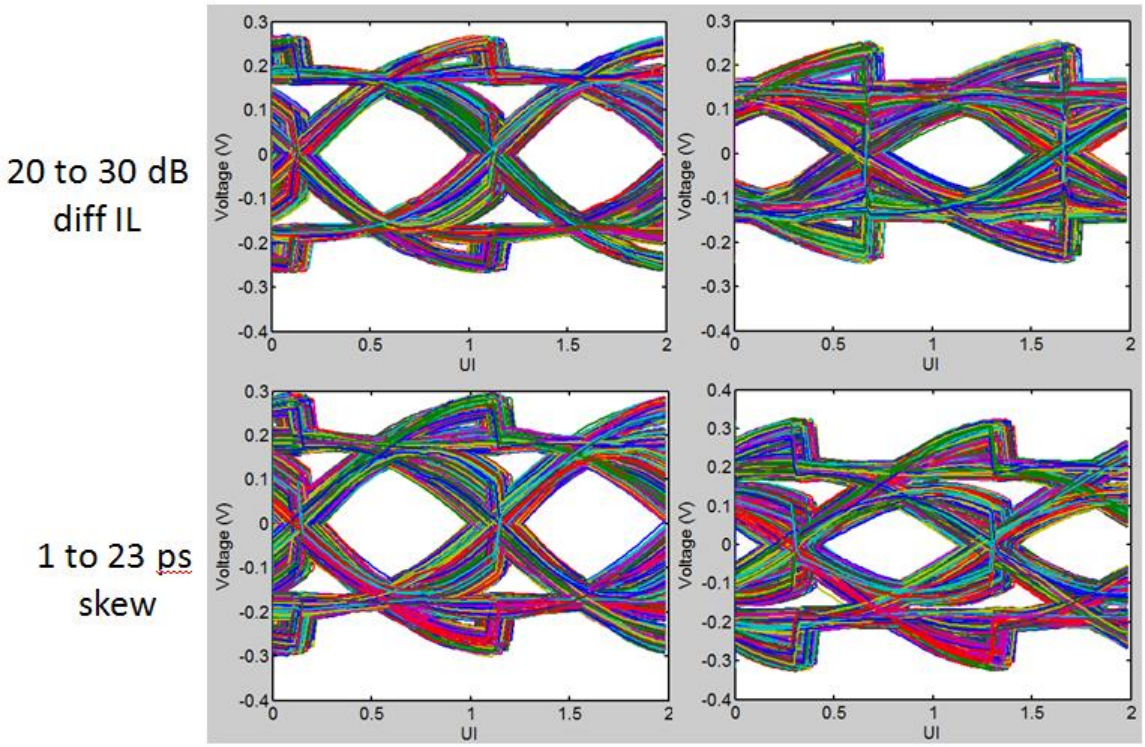


***Figure 18**: Simulations showing the similarity between increased insertion loss (top row) and added skew (bottom row)*

Simulations at Higher Data Rates

Although our measurements are limited to 19.2 Gbps at most, we performed simulations going up to 25.6 Gbps. At this data rate the unit interval is only 39 ps, so our skew models represent almost an entire UI of skew. Below we are showing the eye diagrams obtained using the channel models using the 10 cm compliance card as outline in section III. Looking at the eye widths and heights against skew, we see that channels with more than 20ps of skew give results that do not yield BERs of 10^{-8}. Therefore we see that in this case the receiver cannot tolerate as much skew as a fraction of the UI width because the insertion loss of the channel at this frequency is higher than it was at 19.2 Gbps where we were seeing a functioning channel with 34 ps of skew (more than 60% of the UI).

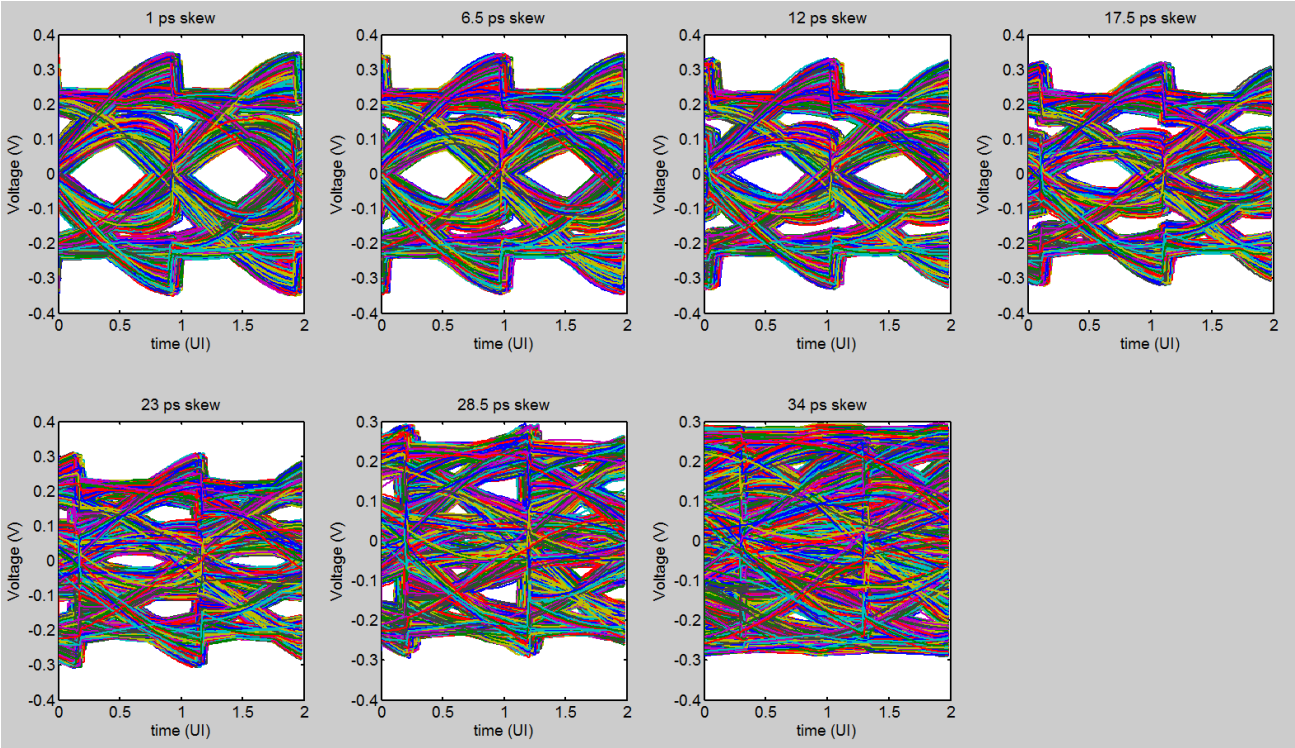


***Figure 19**: Simulated eye diagrams with varying amounts of skew at 25.6 Gbps for 10 cm etched channel length*

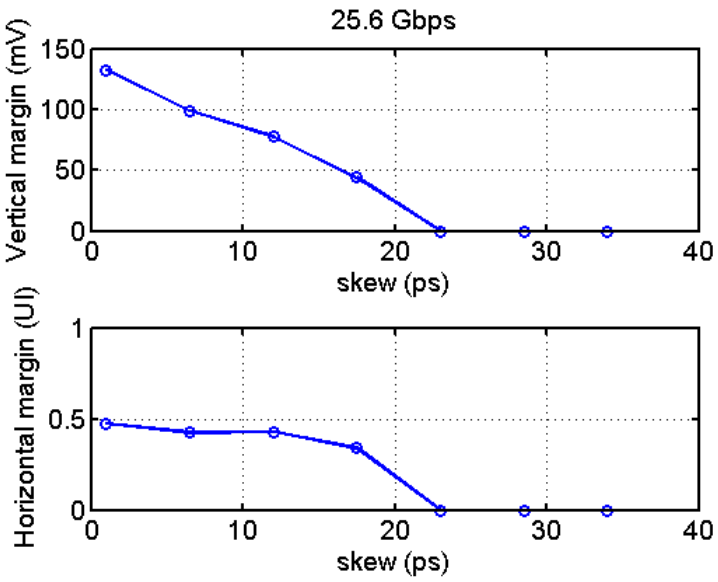


Figure 20*: Simulated eye dimensions with varying amounts of skew at 25.6 Gbps for 10 cm etched channel length*

Conclusions

The main motivation of this study is to understand the level by which we have to control skew in our boards while maintaining enough margin for our SerDes. Should we try to control it by ± 3 ps or maybe ± 20 ps? The answer to this question has great implications for system complexity and cost.

From our measurements and simulations of an actual SerDes channel, we determine that only looking at the passive channel skew was not sufficient for determining the tolerable skew level. There is no correct answer to the above question unless we also include the active models of the SerDes transmitter and receiver. With an industry standard SerDes available in our test, the receiver tuning methods show a great ability to "correct" large amounts of skew (up to 34ps) at high data rates (up to 19.2 Gbps) in a very lossy channel (up to 20 dB loss at the Nyquist frequency).

With the above in mind, we can see a few very simple but important points:

1. As a first order effect, skew translates to insertion loss (for typical values of skew at current <25GB/s data rates).
2. As skew increases second order effects start to show up such as mode conversion and crosstalk.
3. Ultimately (1) and (2) will reduce the signal to noise ratio. We believe as long as margin is still available, extra skew can be sustained in a channel without compromising BER.
4. Regarding common-mode, this is more difficult to account for since it's heavily dependent on the common-mode-rejection-ratio of the receiver. Furthermore, IBIS-AMI does not support common mode simulations. Therefore, even though we have not seen any effect on skew's effect of common mode, ultimately this has to be discussed with the active vendor.
5. We see that standard input tuning methods such as VGA, DFE, AEQ, etc are very good at correcting for skew.

Finally, we believe skew has to be analyzed on a case by case basis and is dependent on the particular system and its cost and performance goals. Different strategies can be applied to compensate for skew to maximize margins and obtain the best BER possible under all conditions.

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