

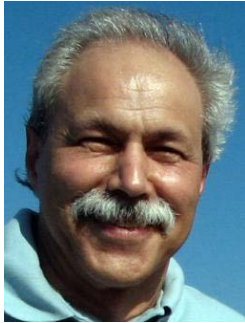
# A Generic Test Tool for Power Distribution Networks

Istvan Novak, Oracle

Peter J. Pupalais, Teledyne LeCroy



# SPEAKERS



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# Agenda

- Introduction
- Common PDN Test Tasks
- Universal PDN Test Tool, Concept
- Universal PDN Test Tool, Implementation
- Summary and Conclusions



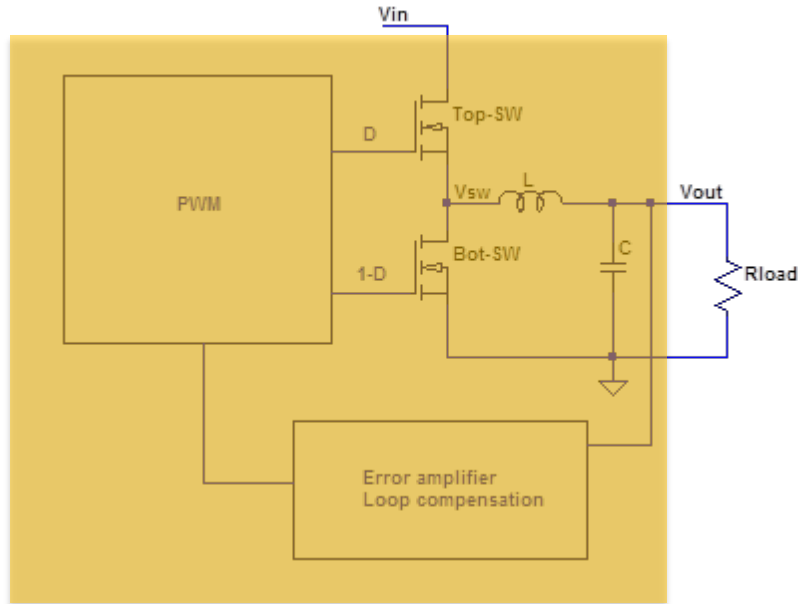
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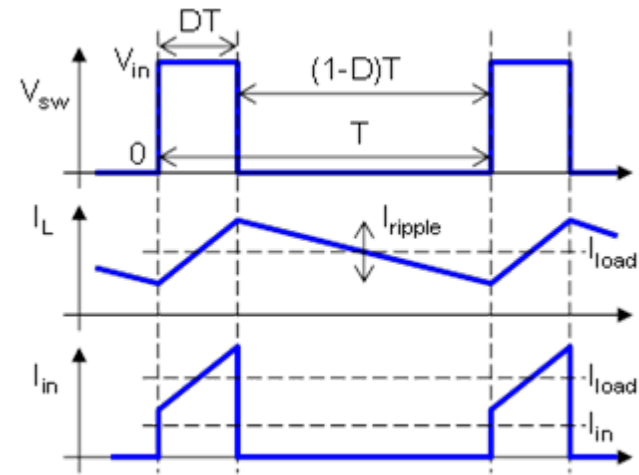


# Introduction

## Non-isolated single-phase buck converter



## Typical waveforms



# Agenda

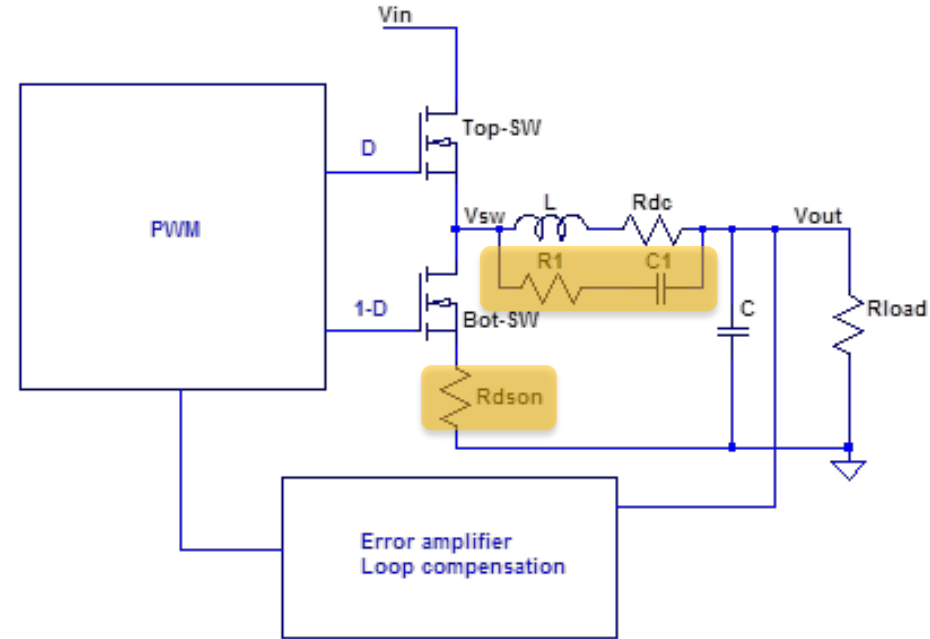
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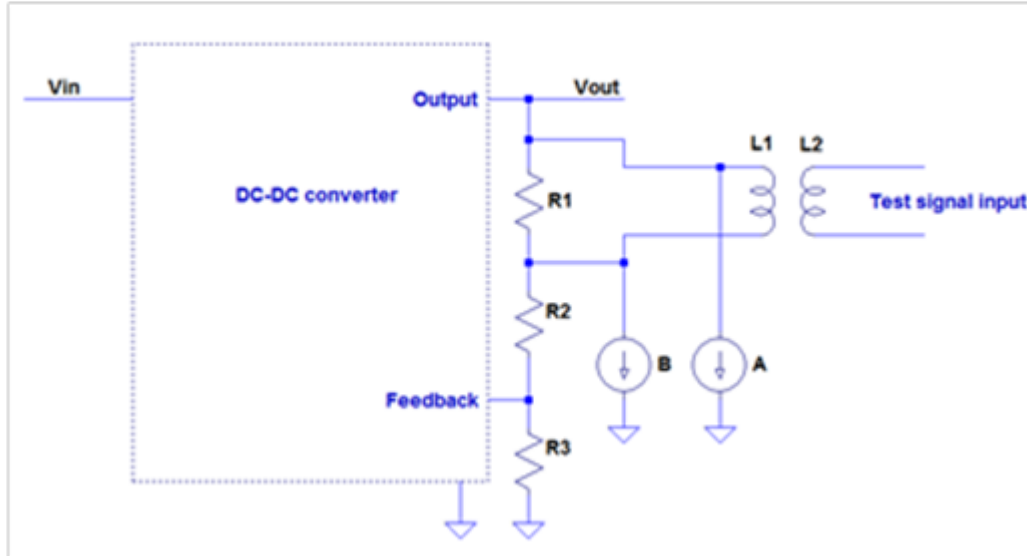
# Input and Output Current, Current Sharing

Options:

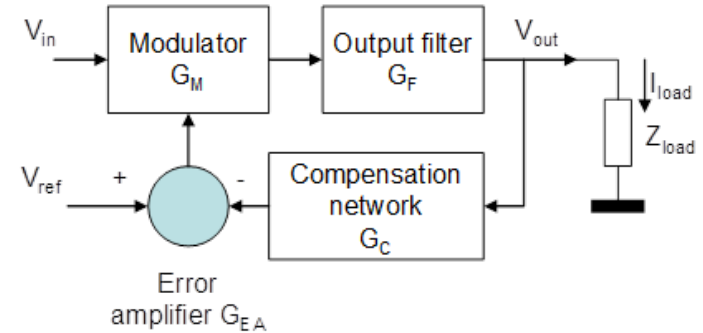
- Inductor current with R-C
- Voltage drop across low-side FET
- Voltage drop across high-side FET
- Voltage drop across shunt element
- Current sensor, shunt



# Voltage Loop Gain

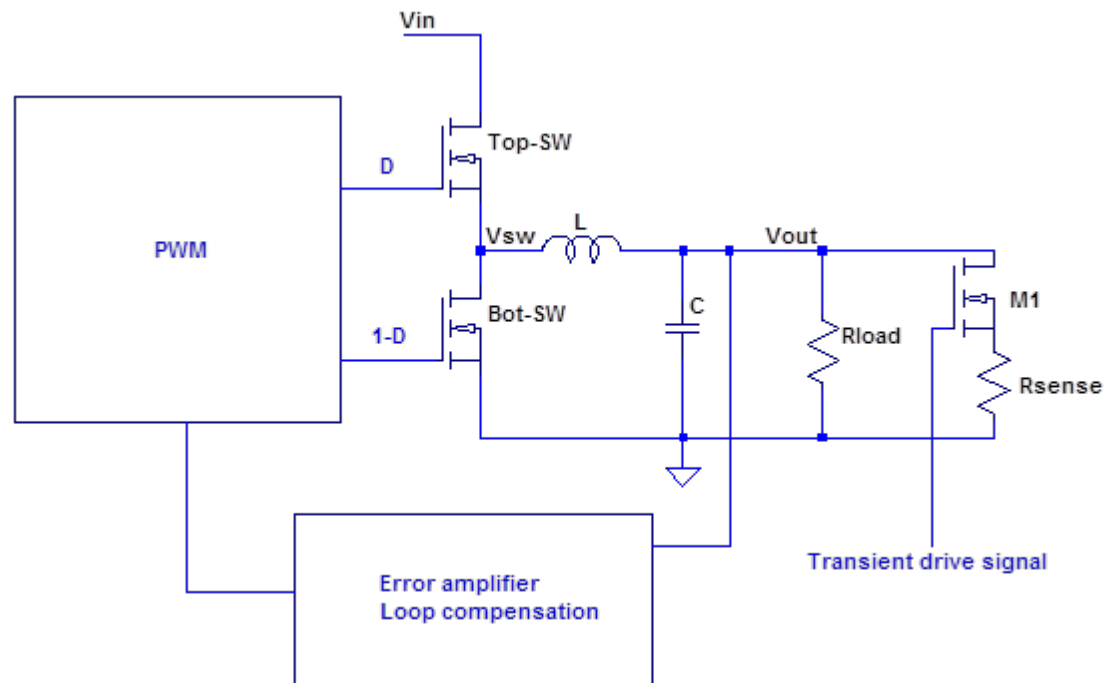


$$G_{loop} = G_M \ G_F \ G_C \ G_{EA}$$

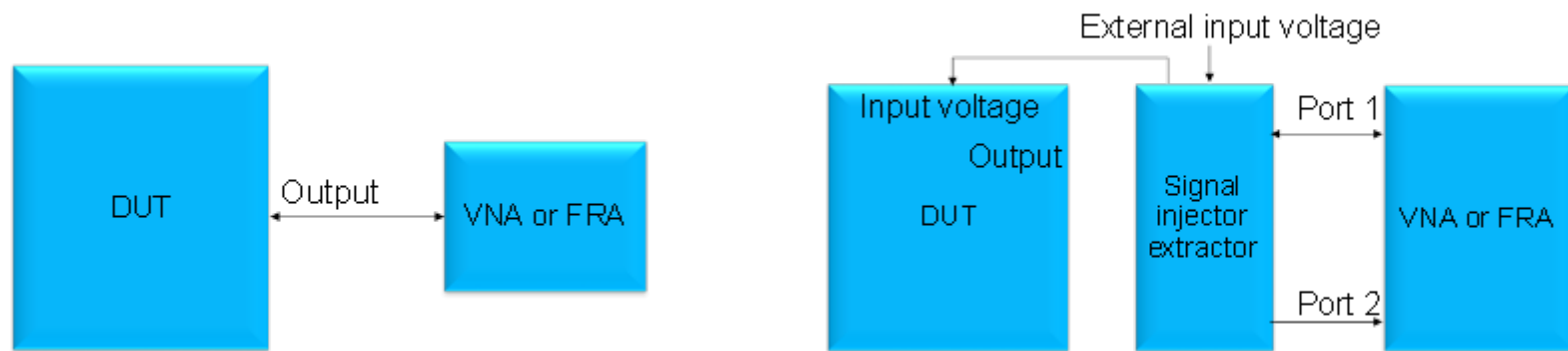




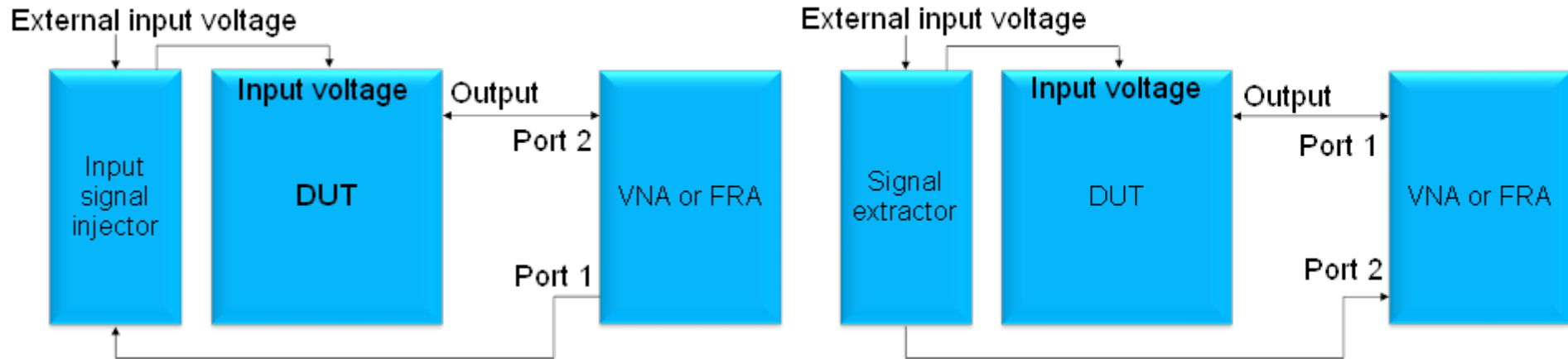
# Transient Response to Load Current



# Output and Input Impedance



# Input-to-Output and Output-to-Input Transfer

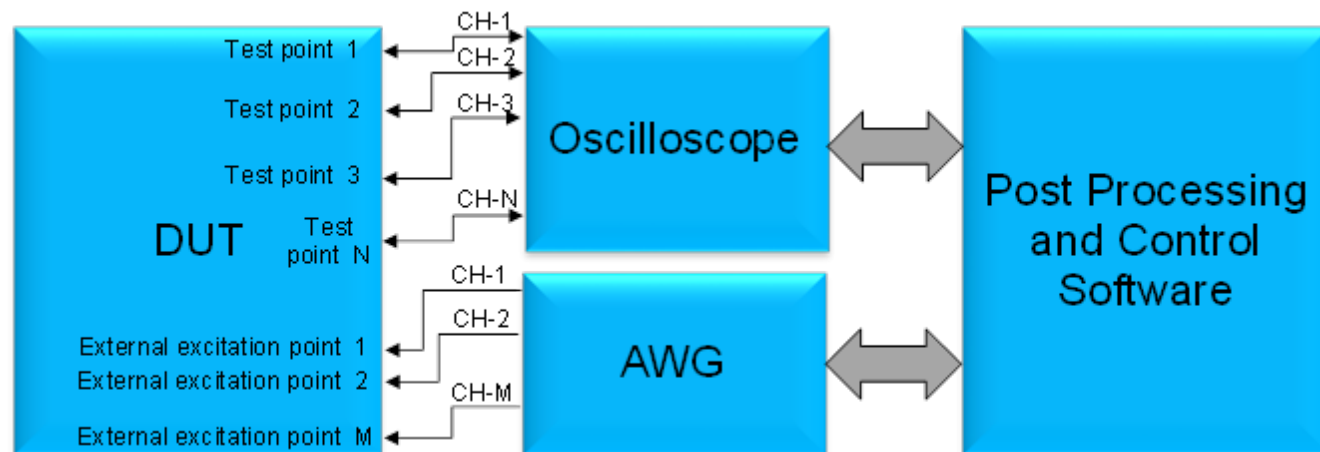


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# Universal PDN Test Tool, Concept



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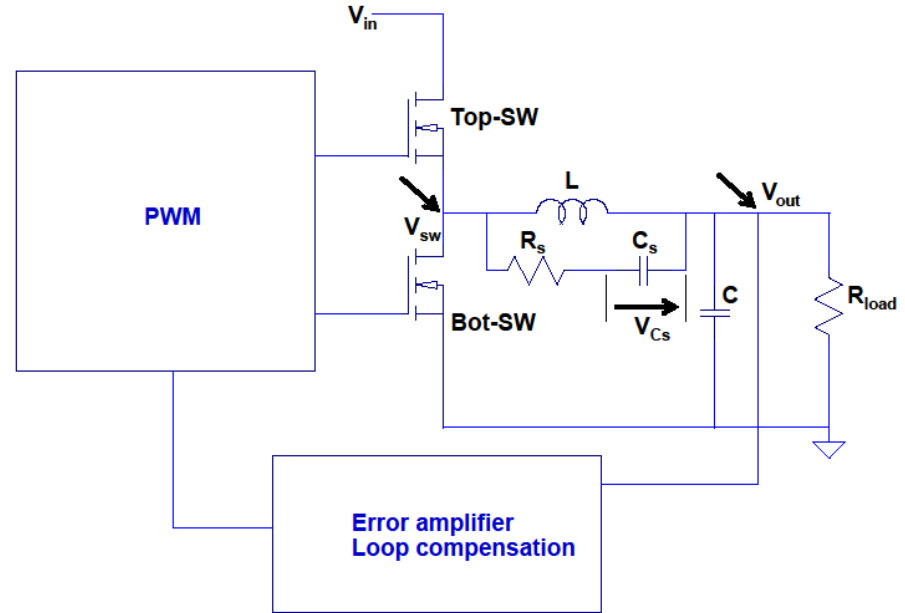
# Implementation

- **Voltage Monitoring Points:**

- $V_{sw}$  – the switch node voltage
- $V_{cs}$  – the differential voltage across  $C_s$
- $V_{out}$  – the output voltage

- **Goal:**

- To correlate the inductor current inferred from  $V_L$  ( $V_{sw} - V_{out}$ ) and the inductor current inferred from  $V_{cs}$ .



# Calculation of IL

$$I_L(s) = V_L(s) \cdot \frac{\frac{1}{L}}{s + \frac{R_L}{L}} \quad s \approx \frac{1}{T} \cdot (1 - z^{-1})$$

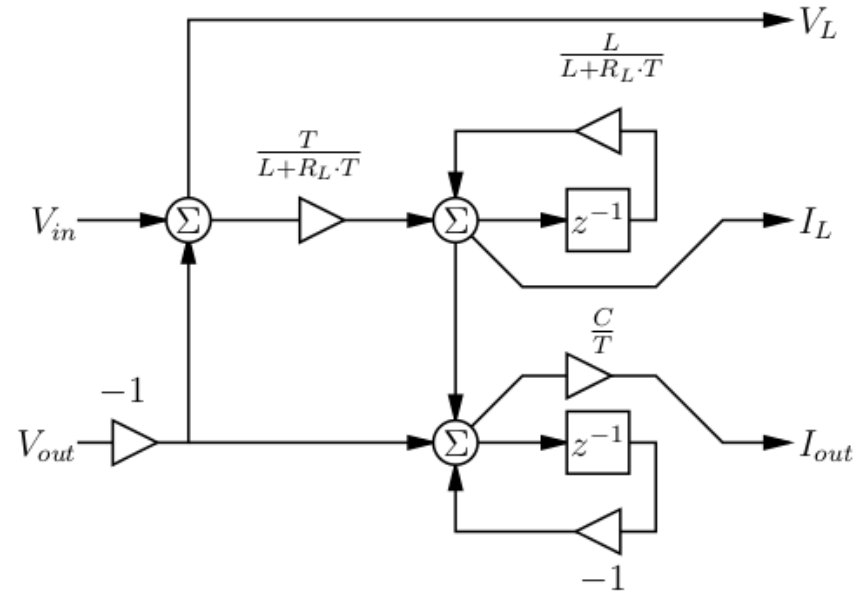
$$H_L(z) = \frac{T}{L + R_L \cdot T} \cdot \frac{z}{z - \frac{L}{L + R_L \cdot T}}$$

$$H_L(z) = \frac{L}{L + R_L \cdot T} \approx 1 - 17.6 \cdot 10^{-6}$$

$$= 0.9999824$$

$$\tau = \frac{L}{R_L} = \frac{15\mu}{26.4m} = 568.2\mu s$$

$$5 \cdot \tau = 2.841ms = 284.1kS@100MS/s$$





# Noise Considerations

Extreme gain at DC

- $Gain = 20 \cdot \log\left(\frac{1}{R_L}\right)$

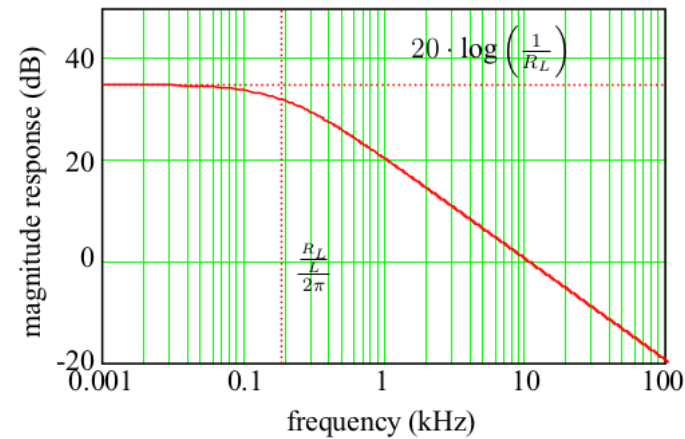
Noise Density depends heavily on VDIV:

- $N_{dBm} = 20 \cdot \log\left(\frac{VDIV \cdot 4}{\sqrt{2}}\right) + 13.010 - SNR - 10 \cdot \log(F)$

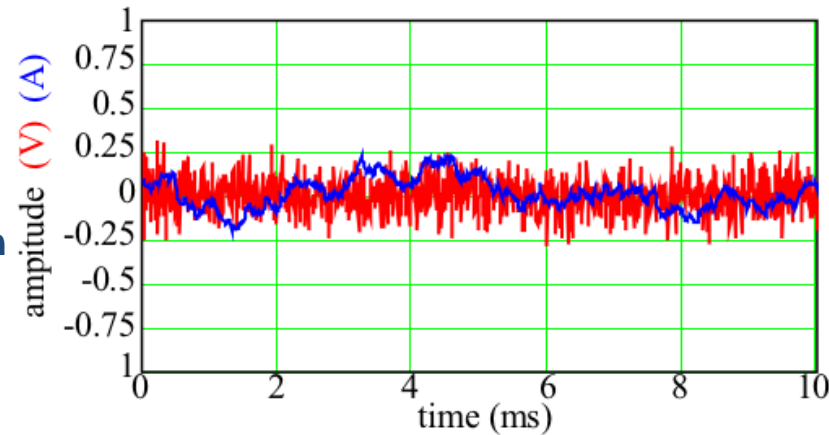
Effect of noise is not necessarily intuitive, but can be simulated.

The expectation for this application is a low frequency wander of +/- 250 mA.

Response of IL  
Calculation



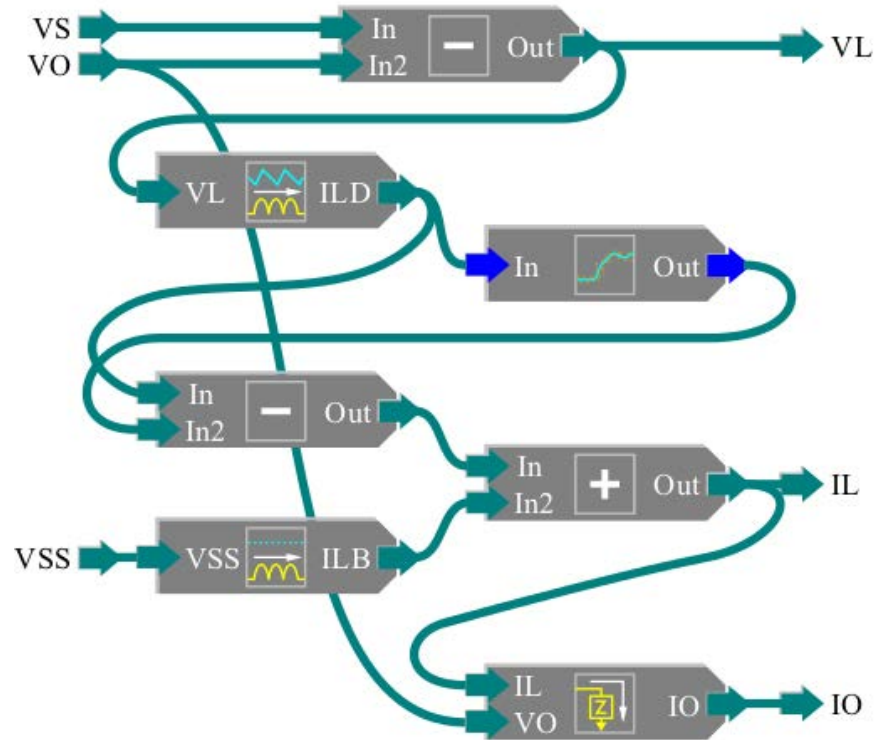
Noise  
Simulation



# Full Inductor Current Processing

- **Makes use of the LeCroy Processing Web**
  - Many special purpose components wired together to produce various output waveforms.
- **Dynamic Current:**
  - Calculated by processing VL (the difference between Vsw and Vout)
  - Filtered to remove low frequency wander (i.e. High pass filter with single pole cutoff around 10 kHz.).
- **Static Current:**
  - Sample switch node waveform at flat spot during off time.

The static and dynamic currents are summed to form IL

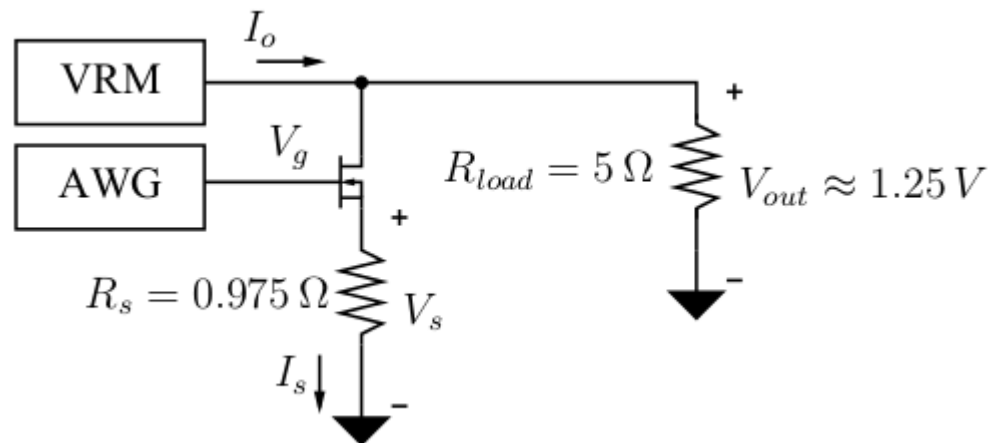
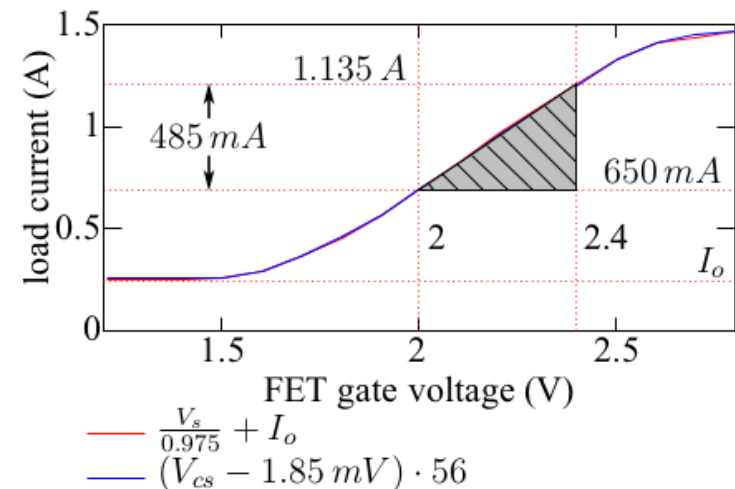


# Transient Load Circuitry

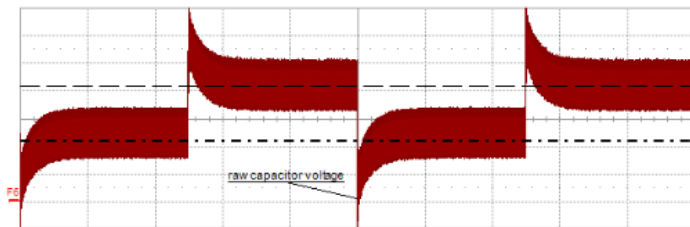
Constant static 5 Ohm load.  $I_{out} \approx \frac{1.25}{5} = 250mA$

Dynamic Load controlled by FET of up to a parallel 0.975 Ohms.

Vs is monitored with scope



# An Unlikely Capacitor Voltage Measurement



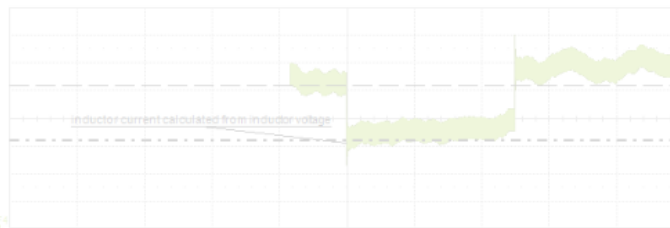
(a) raw capacitor voltage  $V_{cs}$



(b) inductor current calculated from  $V_{cs}$



(c) transient current



(d) inductor current calculated from  $V_L$

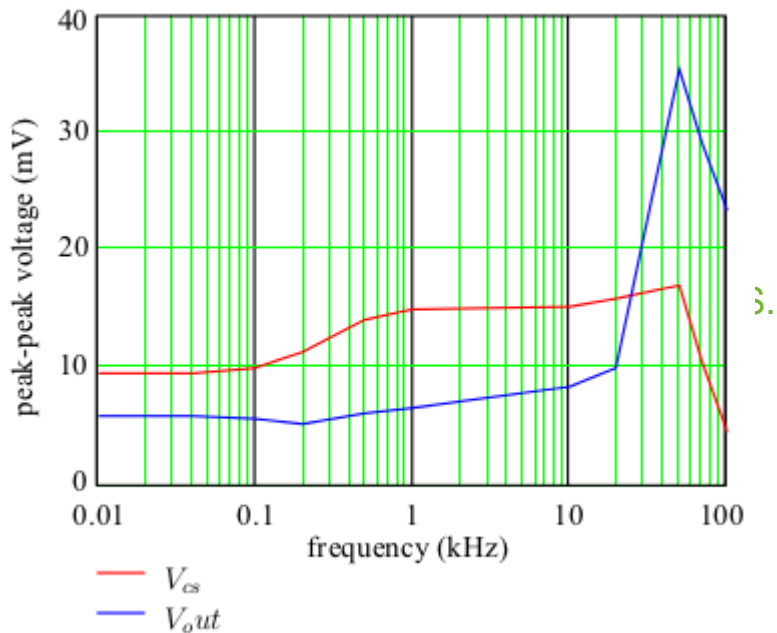
F3	web edit	F4	web edit	F6	web edit	F7	web edit	F8	web edit
250 mA/div		250 mA/div		5.00 mV		250 mA/div		250 mA/div	
2.00 ms/div		2.00 ms/div		2.00 ms/div		2.00 ms/div		2.00 ms/div	
650 mA		1.923 A		10.79 mV		420 mA		650 mA	
1.135 A		2.408 A		20.50 mV		905 mA		1.135 A	
Δ 485 mA		Δ 485 mA		Δ 9.70 mV		Δ 485 mA		Δ 485 mA	

Tbase	0.00 ms	Trigger	C4	DC
	2.00 ms/div	Stop	250 μV	
2 MS	100 MS/s	Edge	Positive	

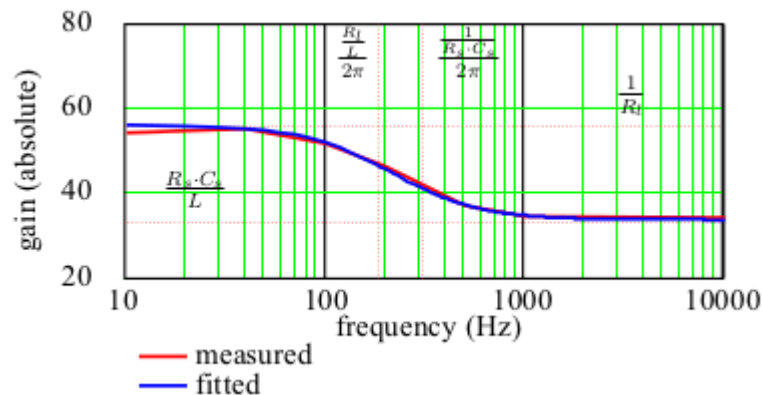
(e) scope settings



# AC Calibration of IL



AC Calibration

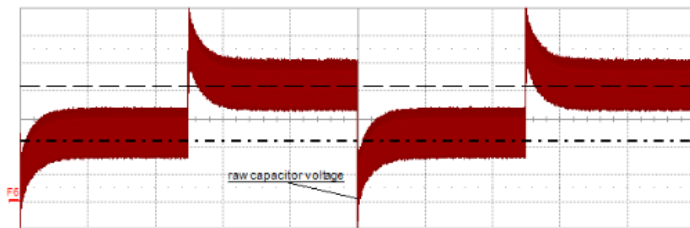


Fitted Results

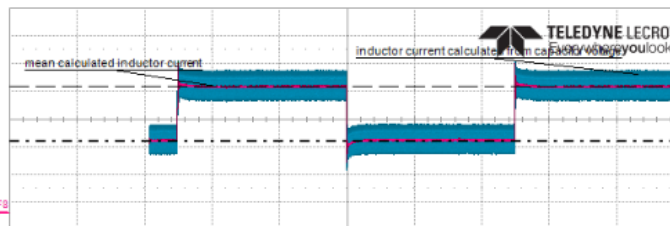
$$H(s) = \frac{s + \frac{1}{R_s \cdot C_s}}{s + \frac{R_L}{L}} \cdot \frac{R_s \cdot C_s}{L}$$

Results fitted to:  $H(s)^{-1}$

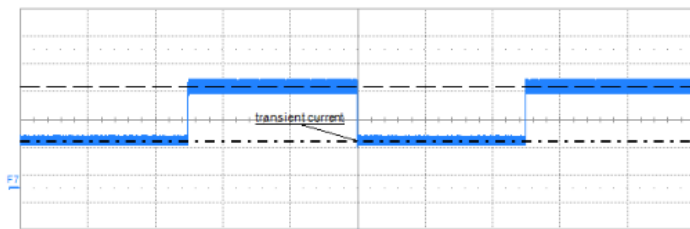
# Correct Calculation of IL



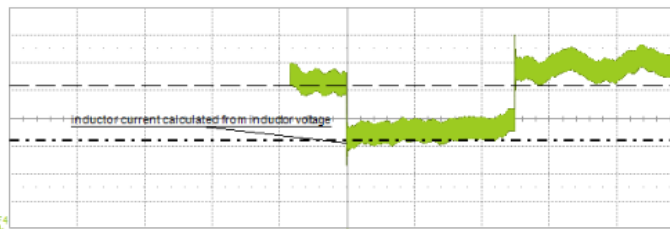
(a) raw capacitor voltage  $V_{cs}$



(b) inductor current calculated from  $V_{cs}$



(c) transient current



(d) inductor current calculated from  $V_L$

F3	web edit	F4	web edit	F6	web edit	F7	web edit	F8	web edit
250 mA/div		250 mA/div		5.00 mV		250 mA/div		250 mA/div	
2.00 ms/div		2.00 ms/div		2.00 ms/div		2.00 ms/div		2.00 ms/div	
650 mA		1.923 A		10.79 mV		420 mA		650 mA	
1.135 A		2.408 A		20.50 mV		905 mA		1.135 A	
Δ 485 mA		Δ 485 mA		Δ 9.70 mV		Δ 485 mA		Δ 485 mA	

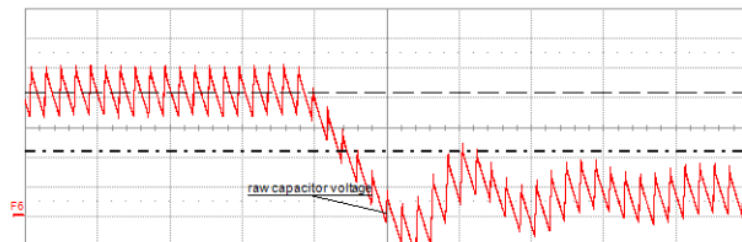
Tbase	0.00 ms	Trigger	C4	DC
	2.00 ms/div	Stop	250 μV	
2 MS	100 MS/s	Edge	Positive	

(e) scope settings

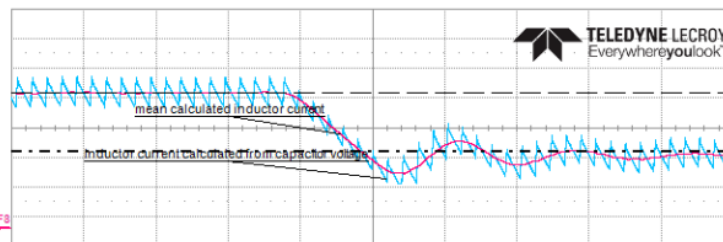




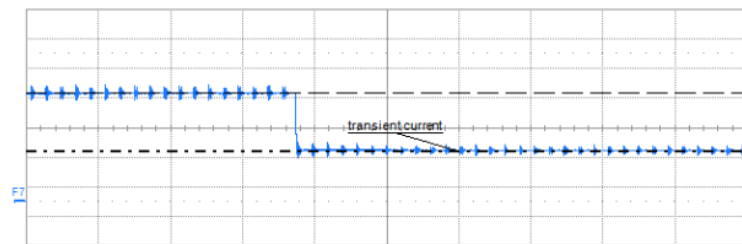
# Correct Calculation of IL



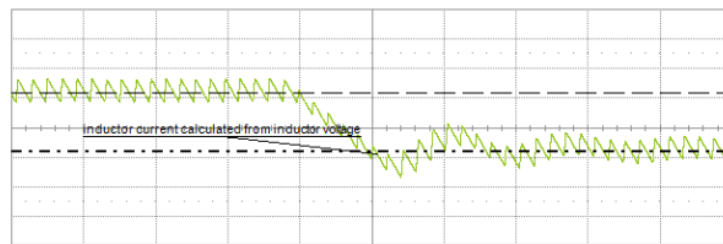
(a) raw capacitor voltage  $V_{Cs}$



(b) inductor current calculated from  $V_{Cs}$



(c) transient current



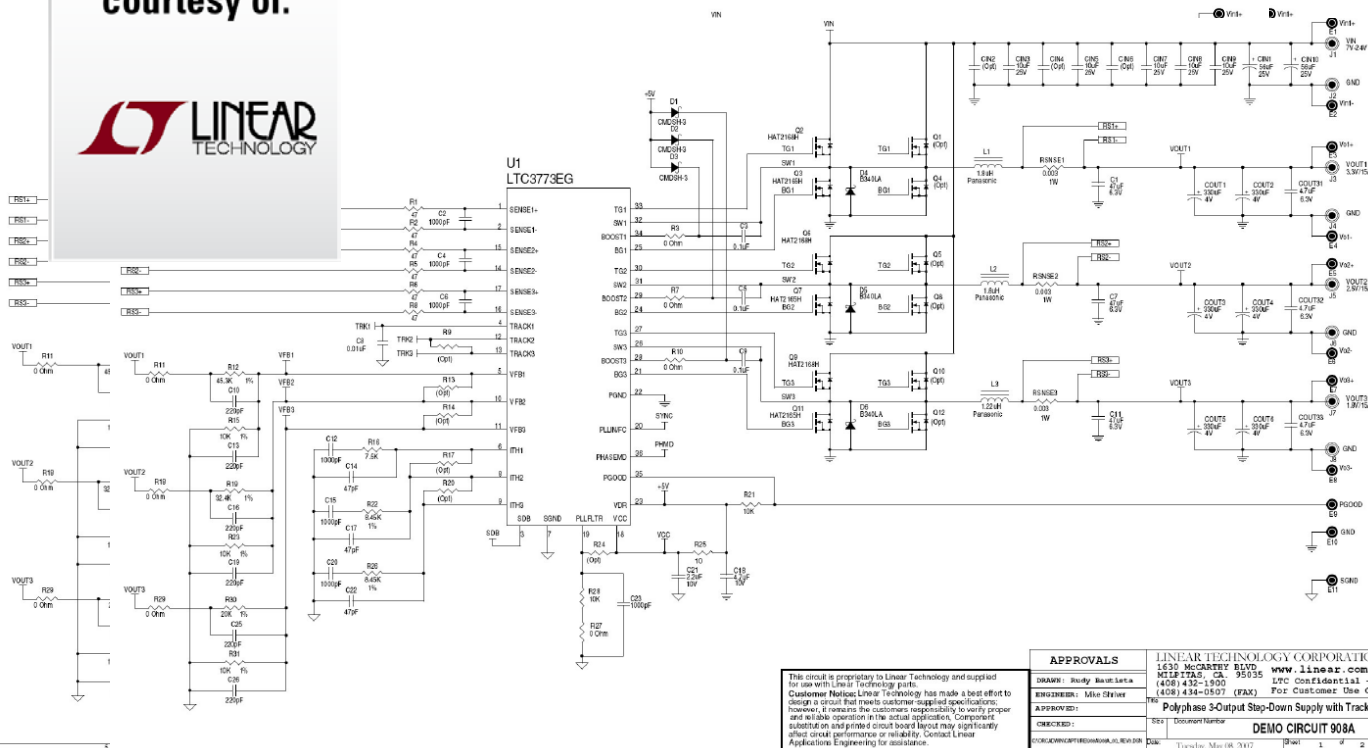
(d) inductor current calculated from  $V_L$

F3	web edit	F4	web edit	F6	web edit	F7	web edit	F8	web edit
250 mA/div		250 mA/div		5.00 mV		250 mA/div		250 mA/div	
10.0 μs/div		10.0 μs/div		10.0 μs/div		10.0 μs/div		10.0 μs/div	
650 mA		1.923 A		10.79 mV		420 mA		650 mA	
1.135 A		2.408 A		20.50 mV		905 mA		1.135 A	
Δ 485 mA		Δ 485 mA		Δ 9.70 mV		Δ 485 mA		Δ 485 mA	

Tbase	0.00 ms	Trigger	C4 DC
	2.00 ms/div	Stop	250 μV
2 MS	100 MS/s	Edge	Positive



**Board  
courtesy of:**



**VOLT1**

**DLC#1**

Pulse Gen1+ E16

Pulse Gen1- E17

Q13 SUD50N03-07

R42 10K

R43 0.310 5% 1W

R44 10K

LOAD STEP1 J1

**VOLT2**

**DLC#2**

Pulse Gen2+ E18

Pulse Gen2- E19

Q14 SUD50N03-07

R44 10K

R45 0.310 5% 1W

R46 10K

LOAD STEP2 J1

**VOLT3**

**DLC#3**

Pulse Gen3+ E20

Pulse Gen3- E21

Q15 SUD50N03-07

R46 10K

R47 0.310 5% 1W

R48 10K

LOAD STEP3 J1

<b>APPROVALS</b> DRAWN: Rudy Bautista ENGINEER: Mike Chirier APPROVED: CHECKED:		LINEAR TECHNOLOGY CORPORATION 1635 McCarthy Blvd. Milpitas, CA 95035 (408) 432-1900 (408) 434-0507 (FAX) www.linear.com LTC Confidential - For Customer Use Only	
POLYPHASE 3-OUTPUT STEP-DOWN SUPPLY WITH TRACKING		DEMO CIRCUIT 908A	
DATE: Tuesday, May 08, 2012		TIME: 1:02	



**JAN 31-FEB 2, 2017**

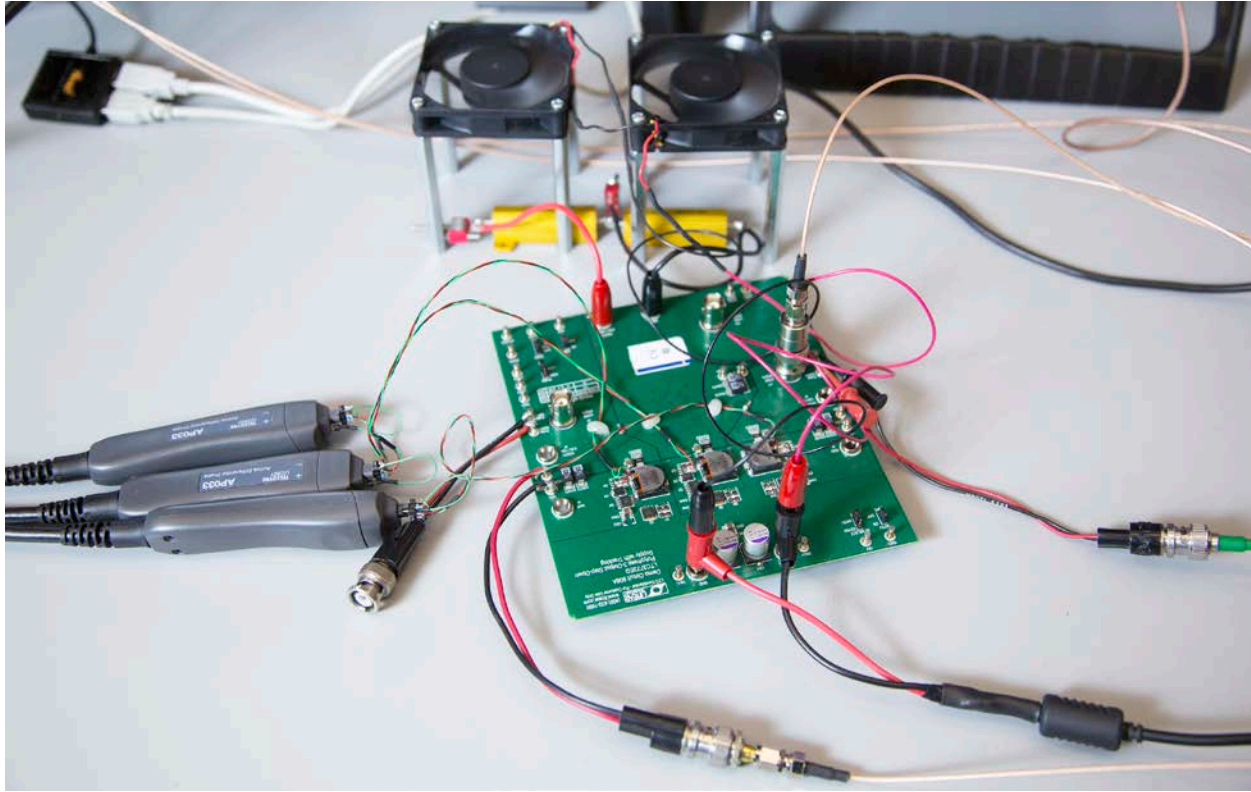


# Disclaimer

- In the development of this paper we worked rapidly in a manner to explore various measurement possibilities and sometimes handled metrology and full measurement accuracy somewhat loosely.
- This most certainly results in measurement inaccuracies that will be addressed in the future and should not reflect badly on the DUT.
- The results shown are our best efforts at reasonable calibration but are mostly indicative of potential instrument capabilities that can be provided in the future.



# Device Under Test Setup

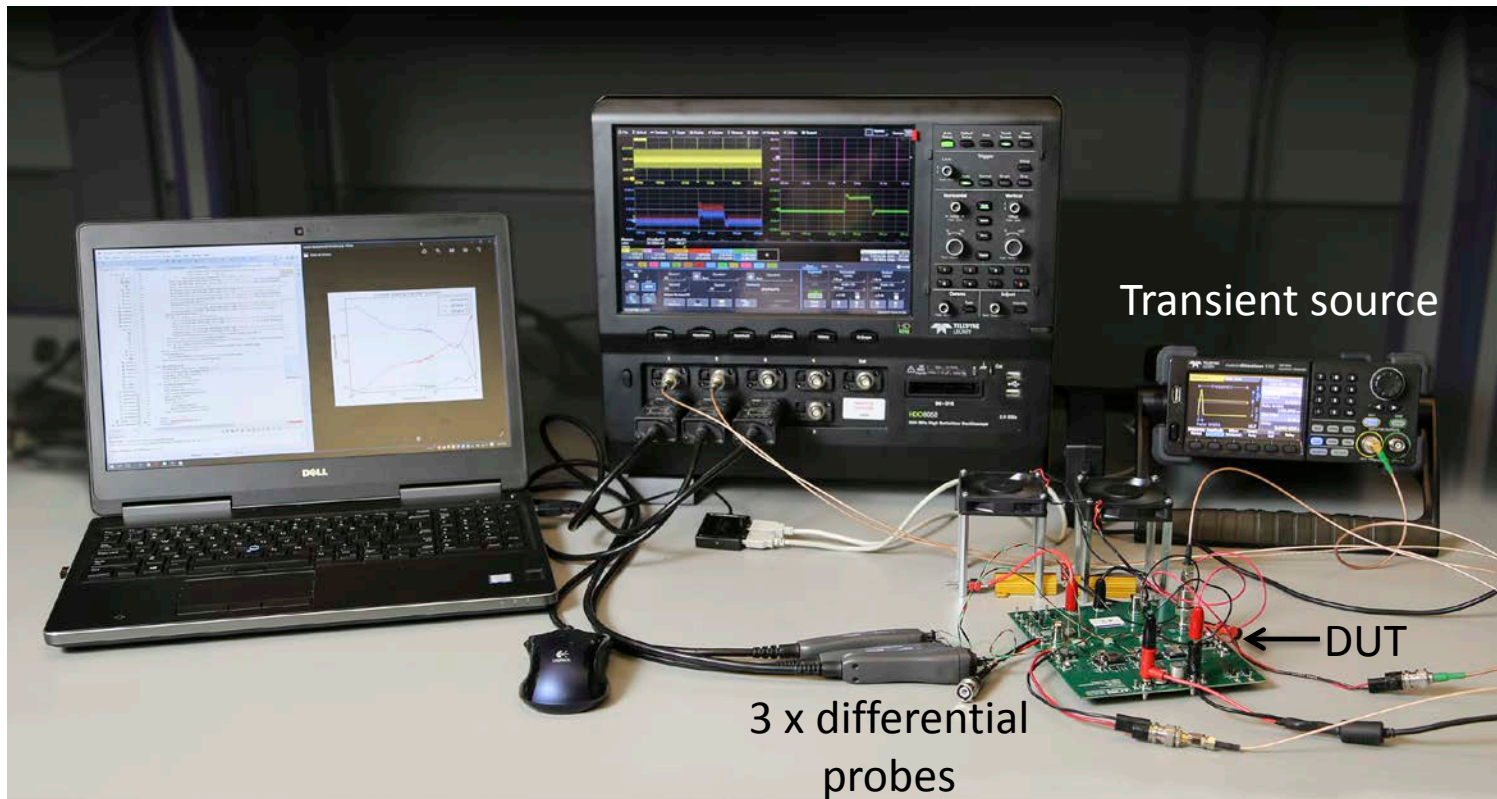


DUT: 3-phase non-isolated  
buck converter

**Board  
courtesy of:**



# Lab Setup



# Transient Generator Limits

- FET max power dissipation: 4 W
- Maximum drain current: 20 A
- Max Vout: 1.22 V
- Source resistor: 10 mOhms, 2W max
- Rdson 10 mOhms

Drain current must be restricted to 3.372 A due to FET power dissipation specification.

At this current, the maximum source resistor voltage ( $V_t$ ) measured will be 33.72 mV.

Complete list of remaining drain current limitations:

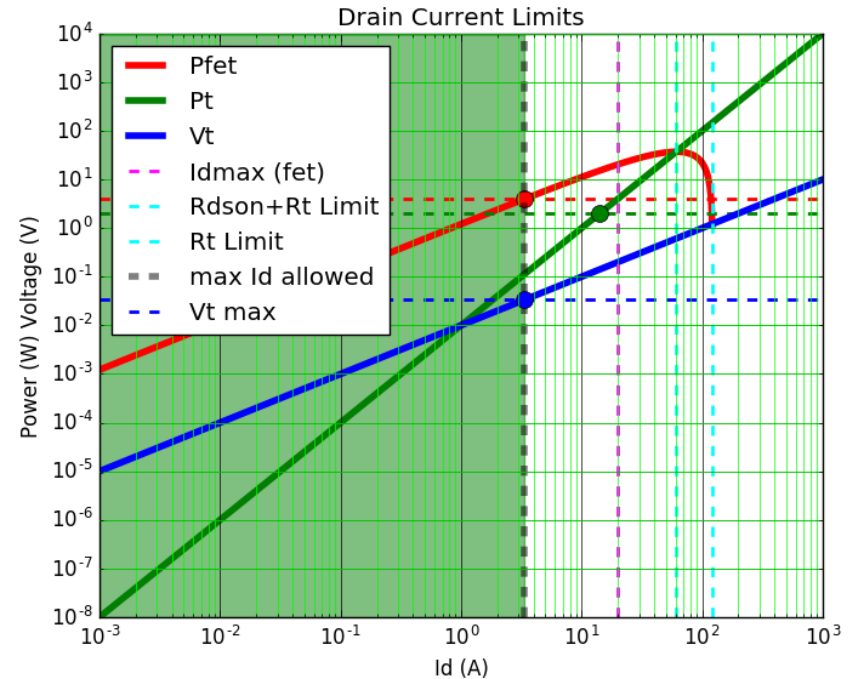
14.14 A allowed due to source resistor power rating.

20.0 A allowed due to fet max drain current specification.

61.0 A possible due to Rdson and source resistor values.

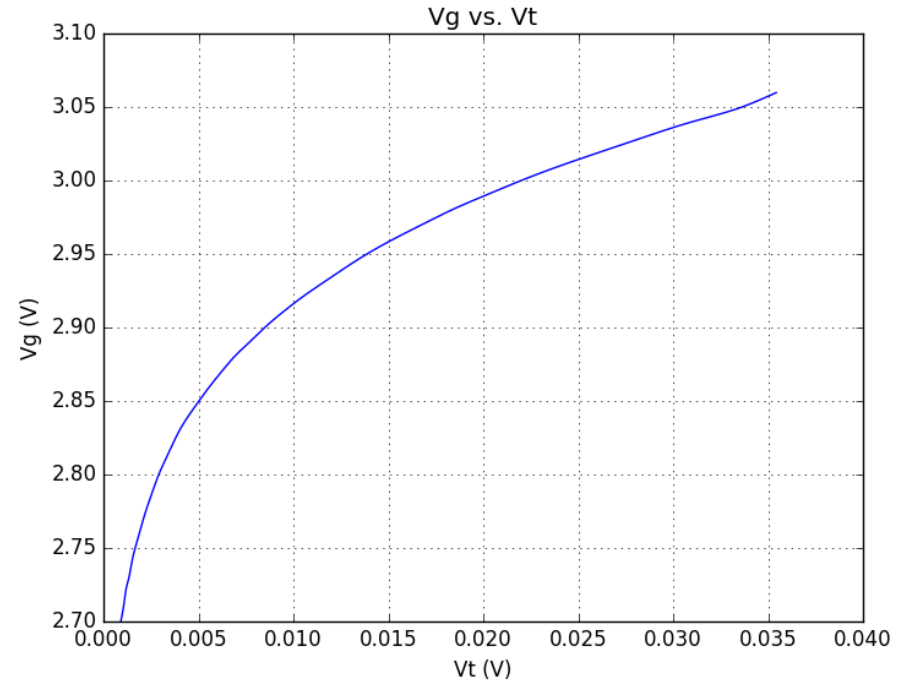
anything below this line is not possible based on the values provided.

122.0 A possible due to source resistor value.



# Transient Generator Calibration

- The FET gate voltage is slowly raised, while measuring the voltage across the source resistor.
- We stop when the voltage across the source resistor reaches the max voltage of 33.72 mV
- A spline is fit to the data so that we can interpolate values of gate voltage needed to generate desired drain currents.
- Idea is to operate in a linear region with given signal swing – bias for class A operation is subtracted from DC load current supplied by electronic load.

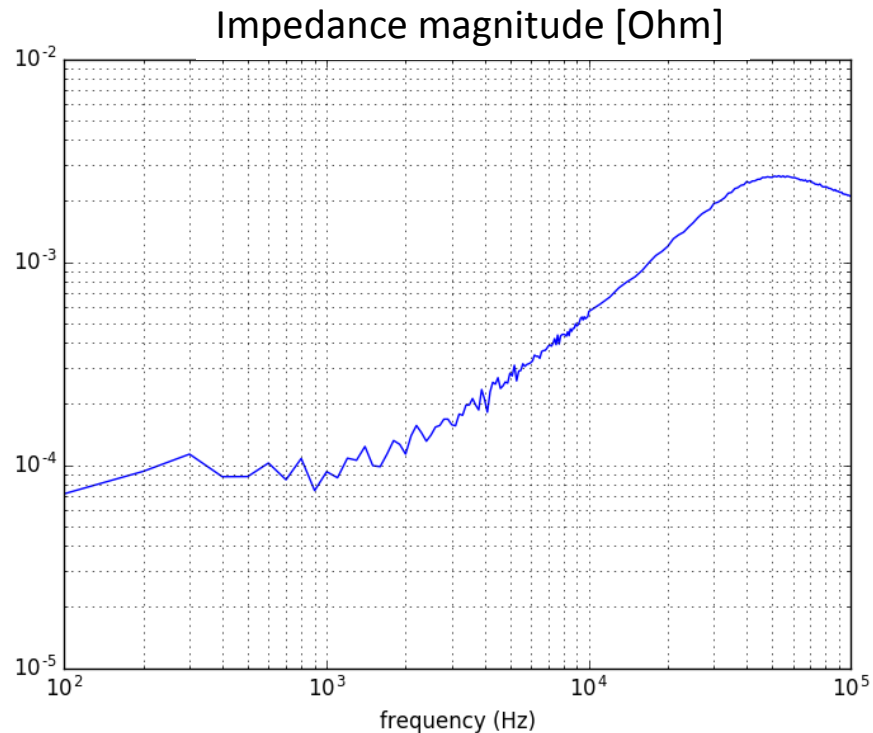
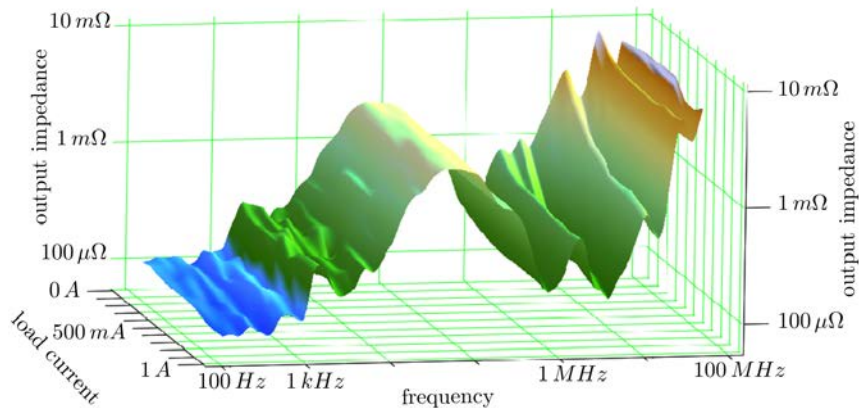




# Output Impedance vs. DC Load Current (Light Load)

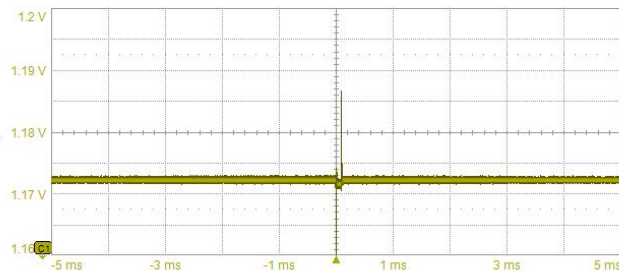
Potential variables:

- DC load current
- DC input voltage
- DC output voltage
- Temperature
- AC excitation current

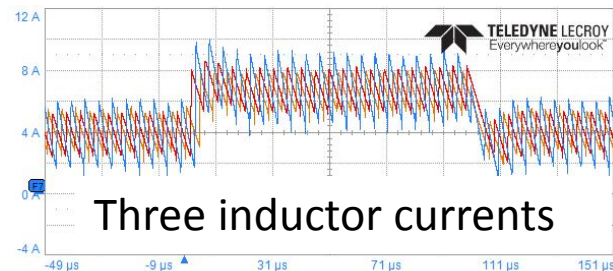
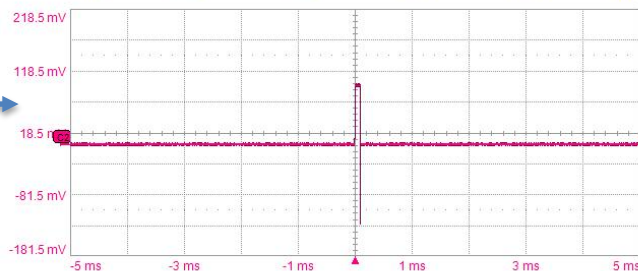


# Transient Current Step

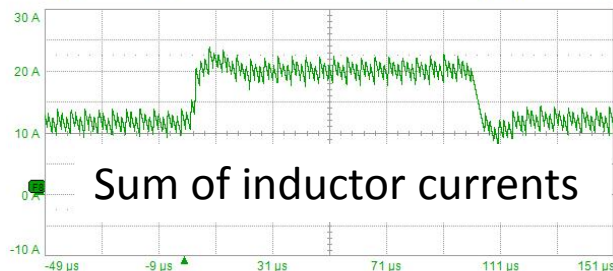
Output  
voltage  
transient



Current-  
sense  
voltage



Three inductor currents



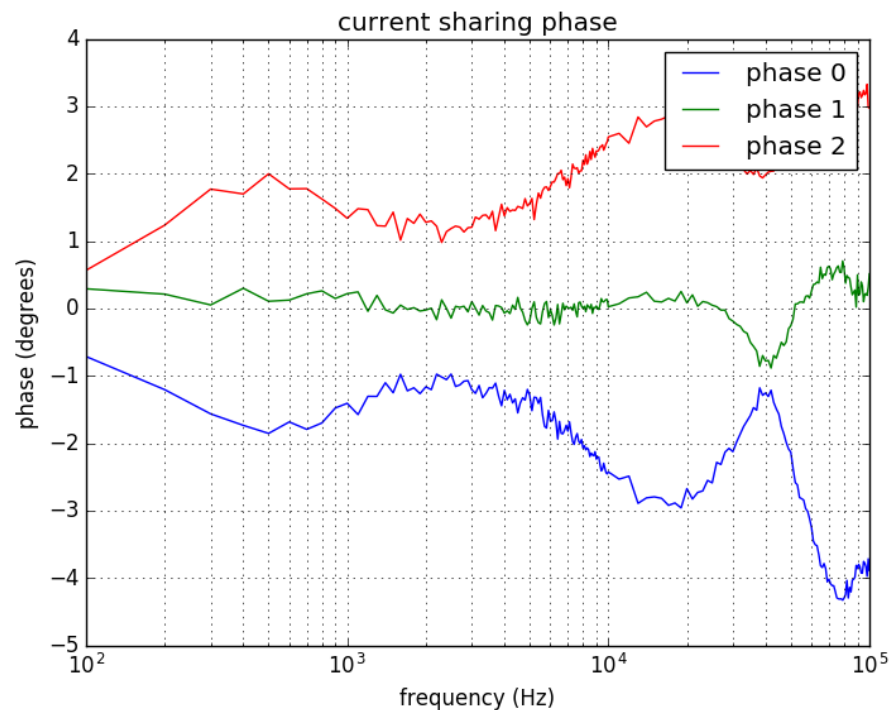
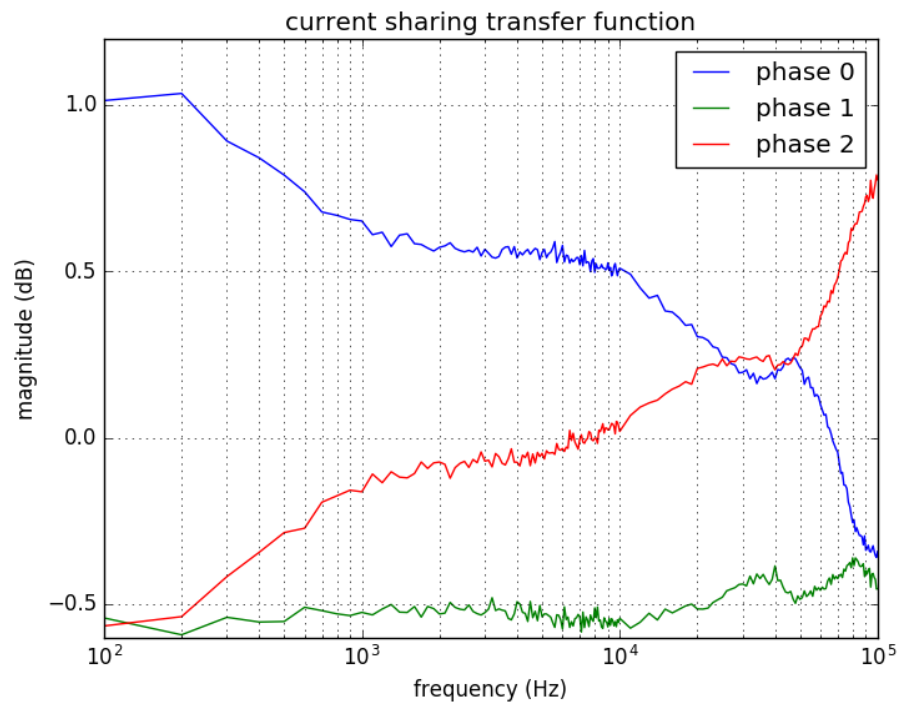
Sum of inductor currents

StdVer	P1.pk(F7)	P2.ampl(F7)	P3.max(F7)	P4.min(F7)	P5.sdev(F7)	P6.mean(F7)	P7.base(F7)	P8.top(F7)	P9:---	P10:---	P11:---	P12:---
value	8.99155 A	8.99147 A	10.00326 A	1.01179 A	1.996851 A	6.862286 A	1.01179 A	10.00326 A				
mean	9.6482 A	9.6482 A	9.9259 A	277.7 mA	2.02196 A	5.7901 A	277.7 mA	9.9259 A				
min	8.62923 A	8.62918 A	9.53236 A	-546.62 mA	1.965231 A	5.247878 A	-546.62 mA	9.53236 A				
max	10.40299 A	10.40290 A	10.31239 A	1.18111 A	2.066058 A	6.953764 A	1.18111 A	10.31239 A				
sdev	433.1 mA	433.1 mA	151.2 mA	430.1 mA	25.71 mA	688.0 mA	430.1 mA	151.2 mA				
num	200	200	200	200	200	200	200	200				
status	✓	✓	✓	✓	✓	✓	✓	✓				
C1	A[B]050	C2	BW[0]50	F5 InductorD	F6 InductorD	F7 InductorD	F8 (F5+F6)+					
	5.00 mV	50.0 mV	2.00 A/div	2.00 A/div	2.00 A/div	5.00 A/div						
	-1.18000 V	-18.50 mV	20.0 μs/div	20.0 μs/div	20.0 μs/div	20.0 μs/div						
	200 #											

Tbase	0.00 ms	Trigger	C2	UC
	1.00 ms/div	Norm.	10.5 mV	
1 MS	100 MS/s	Edge	Positive	



# Current Sharing vs. Frequency





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# Summary

- Various PDN measurement tasks today are covered with different instruments and connections
- A universal PDN test tool is proposed, which produces multiple metrics with the same instruments and minimum number of connections
- Inductor current measurements are possible using Vcs and VL
  - *Although VL measurement may need low frequency correction*
- Next Steps are to use sampled switch node voltage to restore low frequency accuracy
- Extensive calibration is required for any measurement because of large component variability (especially estimation of RL).
- The same instrumentation can be used for time-domain and frequency-domain tests
- Post-processing of inductor currents of multi-phase converters provides current-sharing transfer function



# Thank you!

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## QUESTIONS?

