

Case Studies Isolating Types of Power-Integrity Effects on Signal-Integrity, and Means of Mitigation

Nitin Bhagwath (Mentor Graphics, A Siemens Business)

Rula Bakleh, Scott McMorrow, Istvan Novak (Samtec Teraspeed Consulting)

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Speaker



Nitin Bhagwath

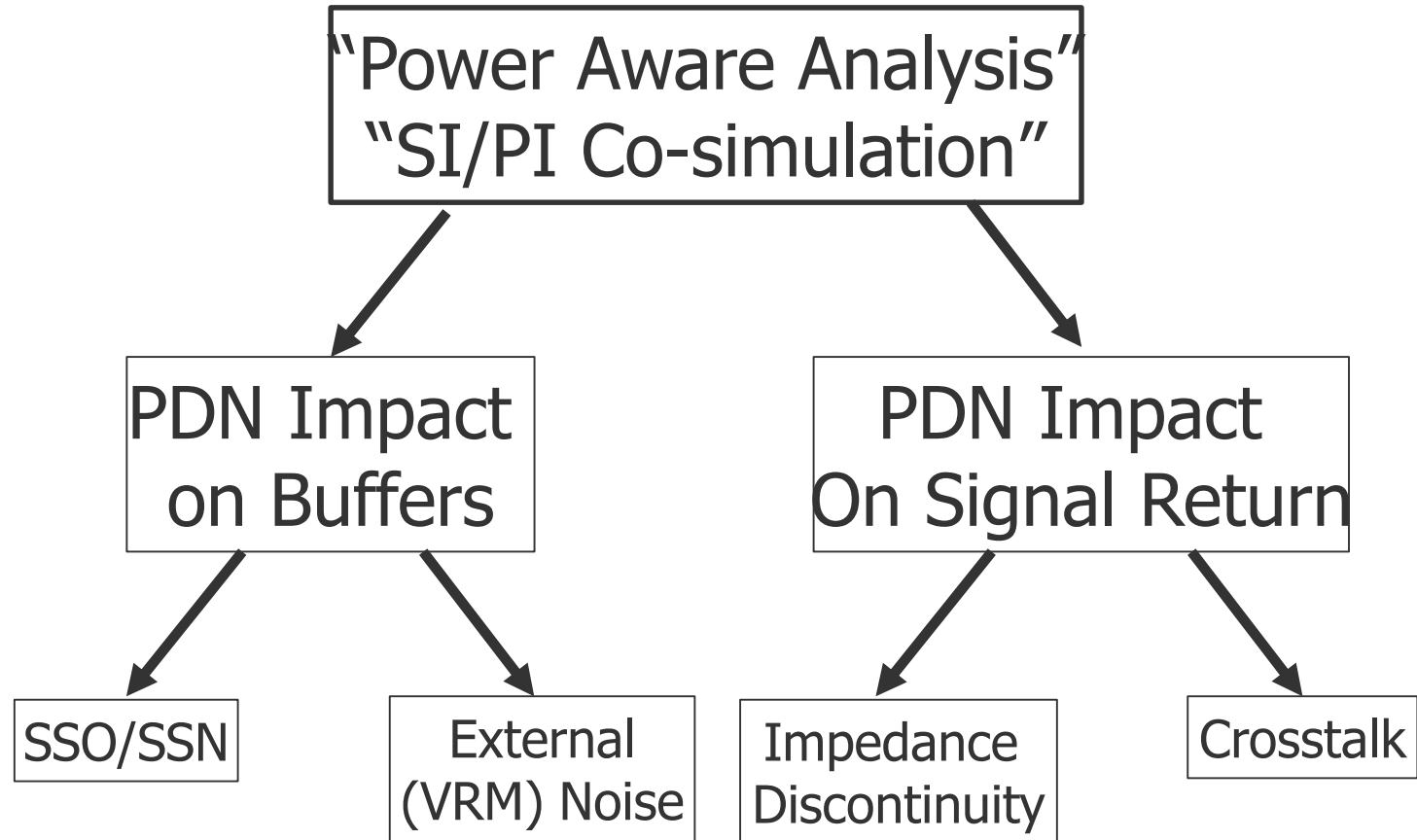
Product Architect, Mentor Graphics (A Siemens Business)

Nitin_Bhagwath@mentor.com

Outline

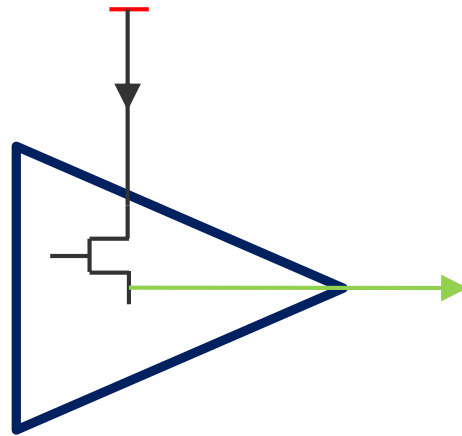
- Background
- PDN effects on Buffer
- Return path PDN effects
- Test Case

Background



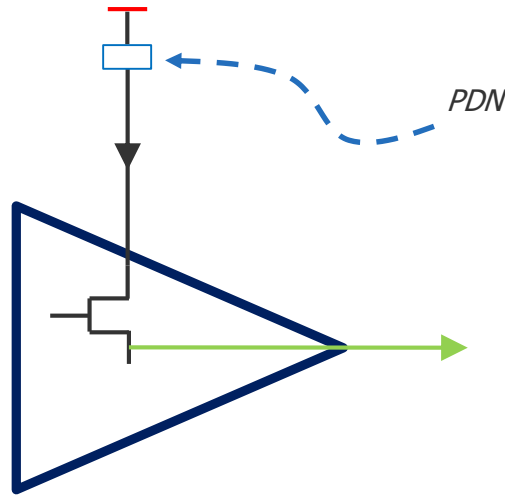
BUFFER EFFECTS

Buffer Effects > Background



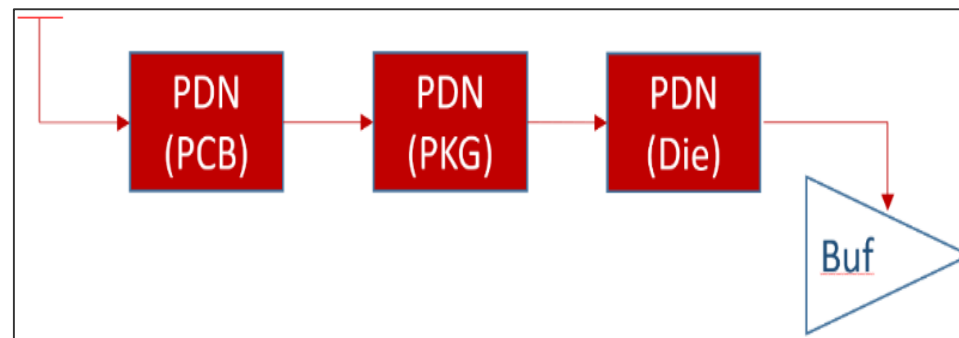
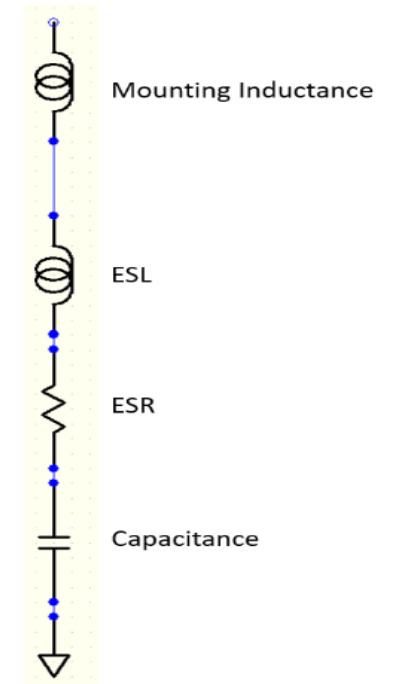
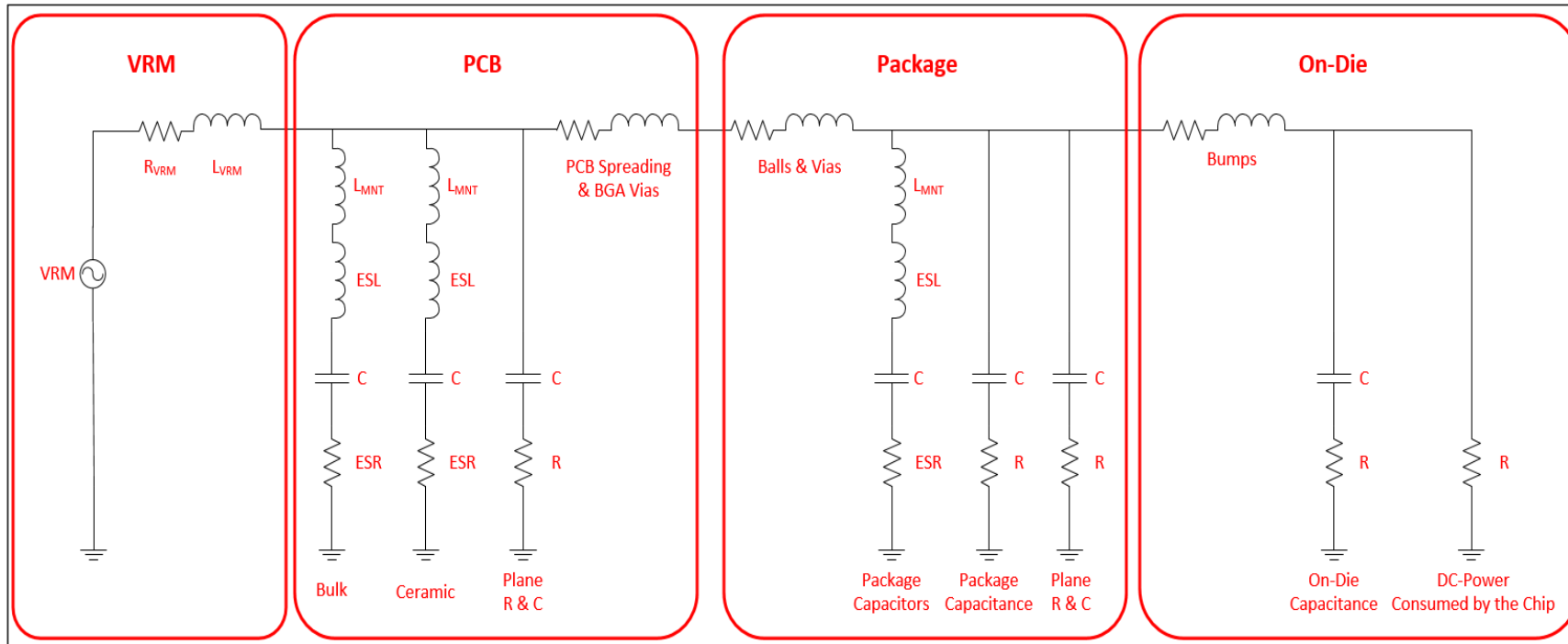
- Traditional driver assumes ideal power supply
- Provide power equally well across all frequencies

Buffer Effects > Background



- In reality, power is delivered to the driver through an imperfect Power Delivery Network (PDN)
- PDN might not be able to react fast enough to provide power to the driver equally well at all frequencies
- Signal quality can be affected

Buffer Effects > Modeling the PDN



Buffer Effects > Two methods of Analysis

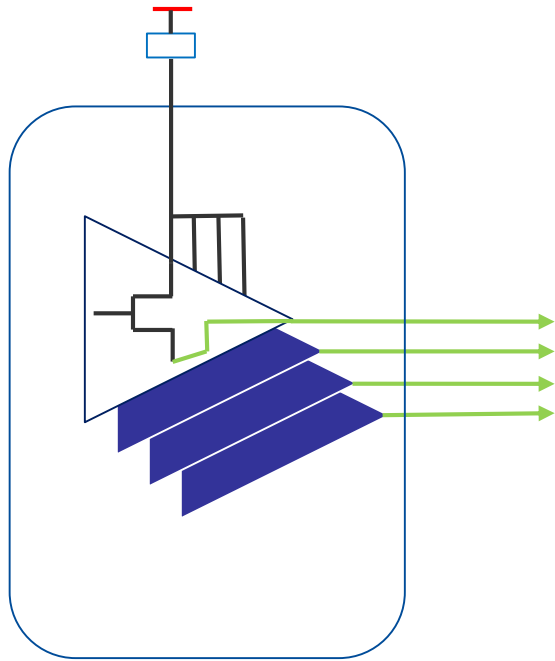
Frequency Domain

- Ensure that impedance in Z-parameter is below requirement across all frequencies of interest
- Easy to visualize and detect errors
- Can be difficult to get frequency dependent impedance requirement
- Does not correspond to Jedec's timing requirements at DRAMs

Time Domain

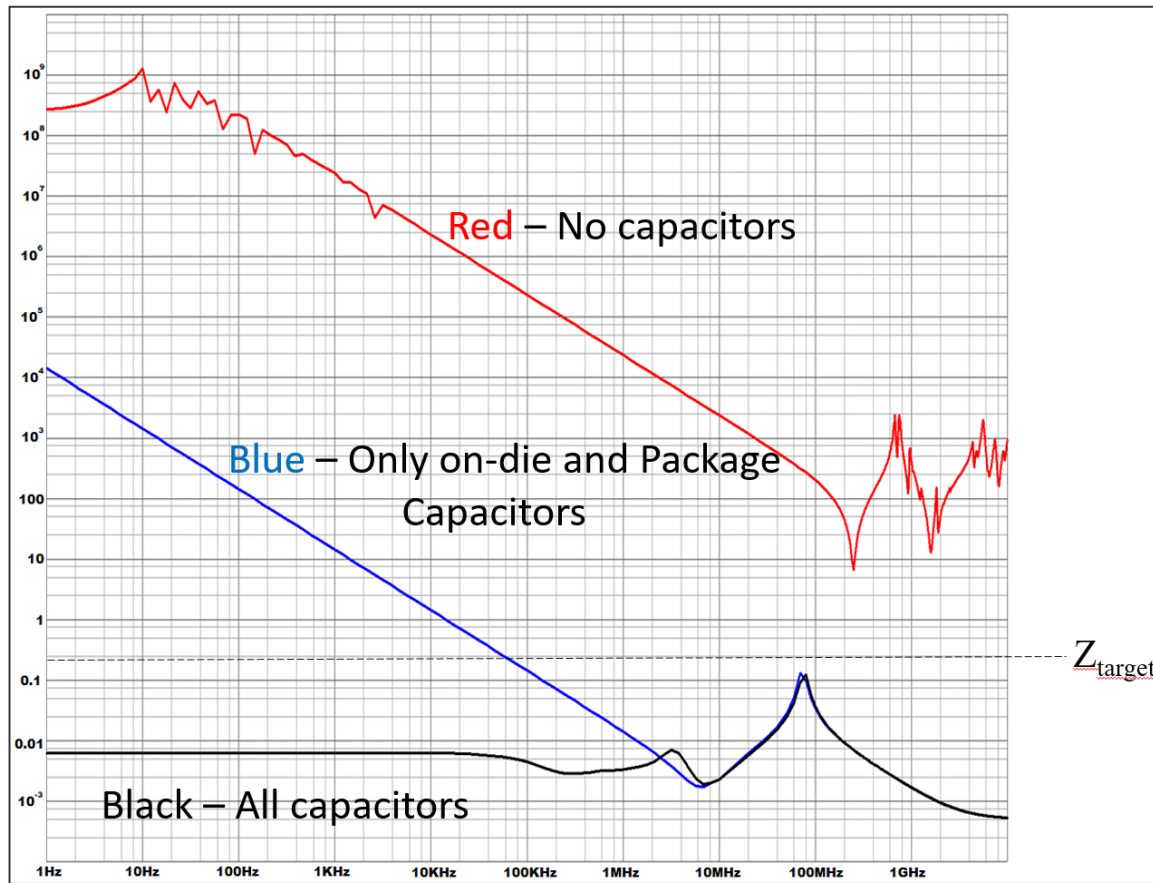
- Complete analysis including timing requirements at controller and DRAM
- Noise visible on signals might not be easily separated from other sources of noise
- Correctly generated Power-Aware IBIS models v5.0 (or equivalent) are required

Simultaneously Switching Noise > Background



- Effect exacerbated when multiple signals demand power at the same time from the same PDN
- Simultaneously Switching Output (SSO) causes Simultaneously Switching Noise (SSN)

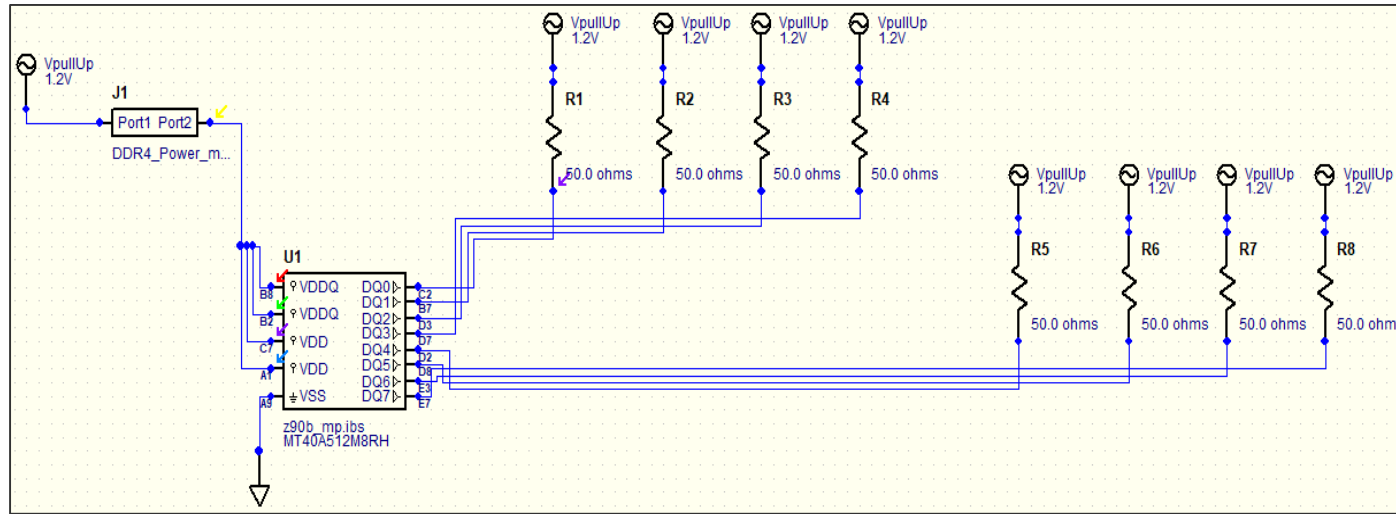
SSN > Frequency Domain Analysis



■ 3 Cases

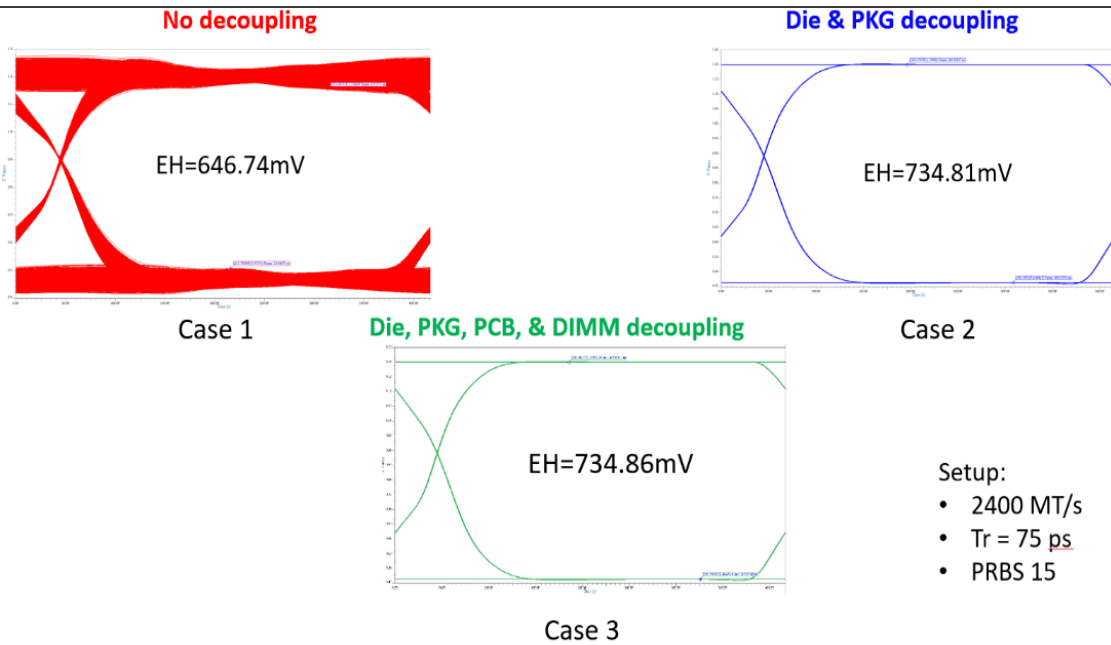
- No Capacitors anywhere
- Add only Pkg/Die Capacitances – helps higher frequencies
- Add all capacitors and DC source

SSN > Time Domain Setup



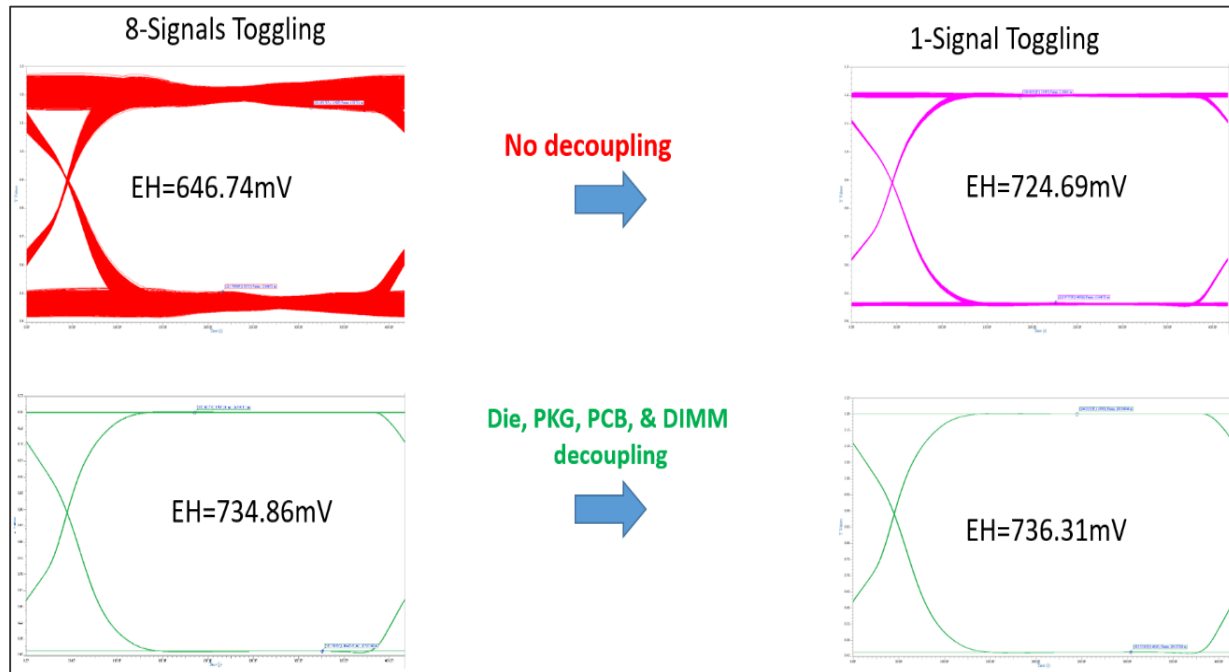
- Actual Board PDN
 - Without any Decoupling Capacitors
 - With only Pkg+Die Capacitors
 - With all Capacitors and DC source
- Signals directly terminated – no transmission line or other “irrelevant” effects

SSN > Time Domain Results – Vary Decoupling



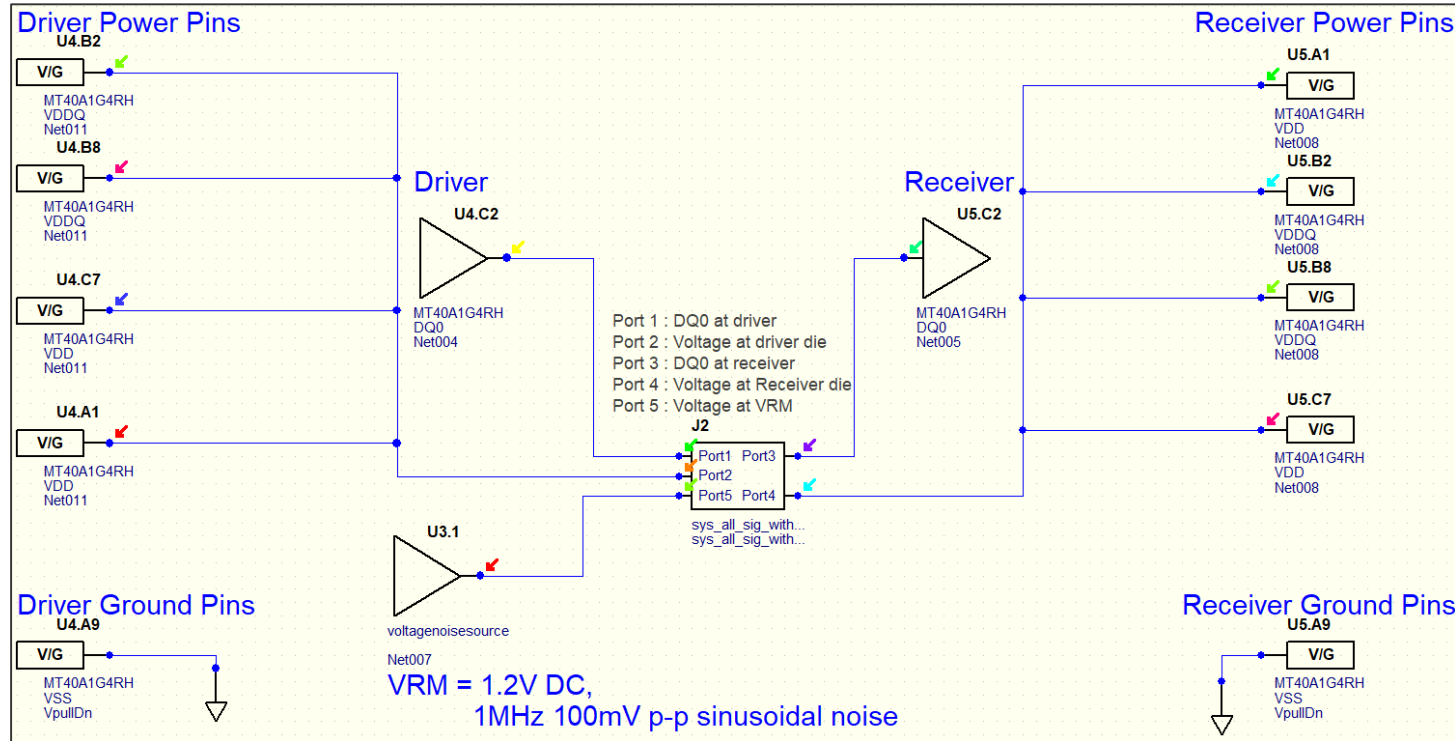
- 8 bits toggling PRBS 15 at 2400MT/s
- Only Pkg+Die
 - Less than **1mV** worse than best case
- No Decoupling
 - **88mV** worse than best case
- ***Only Pkg/On-Die decoupling has real effect on SSN***

SSN > Time Domain Results – Vary Number Bits



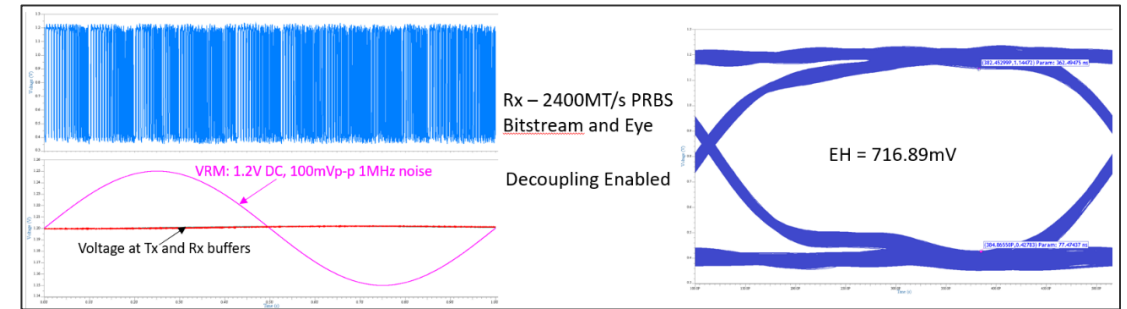
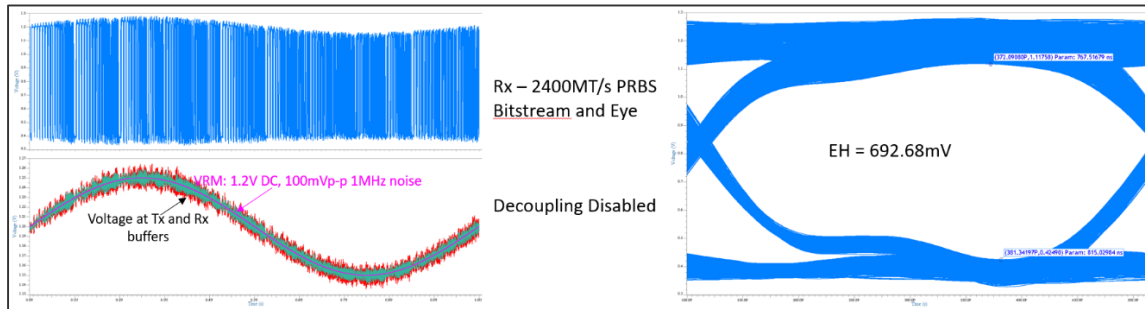
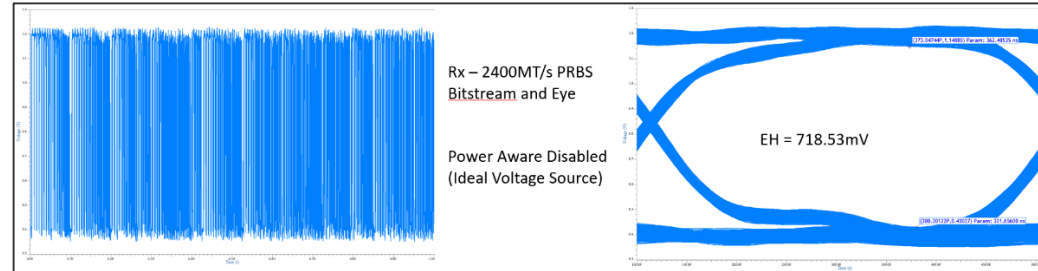
- All bits active vs. one bit active
- All bits active (rest held high)
 - Decoupling impacts **88mV** noise
- One bit active
 - Decoupling impacts **2mV** noise
- ***SSN is Bit-Pattern sensitive***

VRM Noise > Setup



- Same PDN as before
- VRM Assumed to have 1MHz 100mV p-p Sinuosoidal noise

VRM Noise > Results



- 100mV p-p noise causes eye collapse by about 26mV (no decoupling)
- Good Decoupling opens up nearly all of it

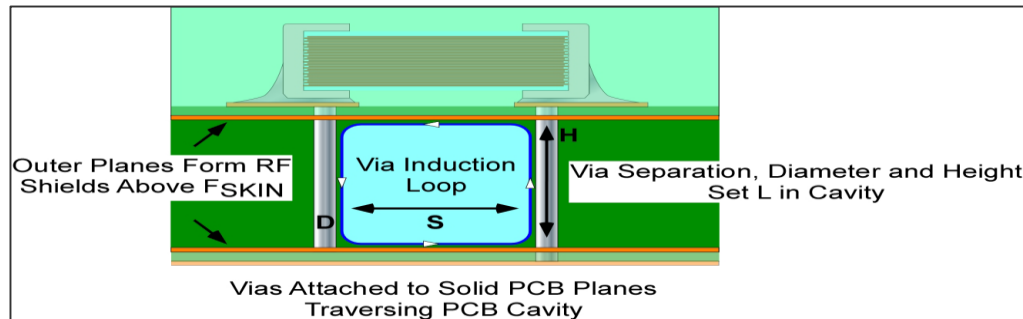
Detection

- Frequency Domain gives quick feedback about potential issues
 - Impedance below target over all frequencies
 - Impedance flat (reduced resonances)

- Find difference in Time-Domain setup
 - With Power-Aware effects Enabled
 - With Power-Aware effects Disabled
- If difference is large, potential PDN related issue
- Can take long time to run with power-aware effects, especially at low frequencies

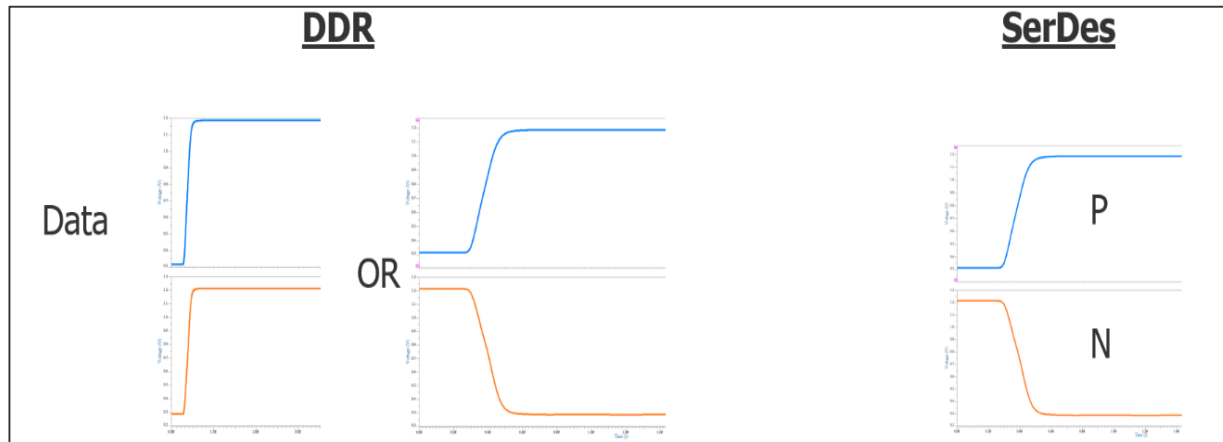
Mitigation

- Reduce inductance for Decoupling capacitors
 - Place close to load
 - Mount with low-inductance method

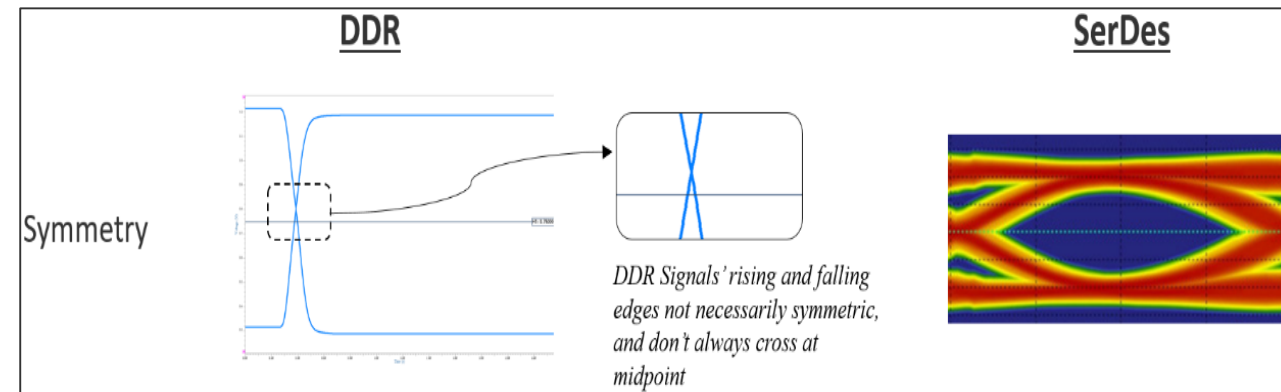


Why is DDR more susceptible to SSN?

Single Ended Signals



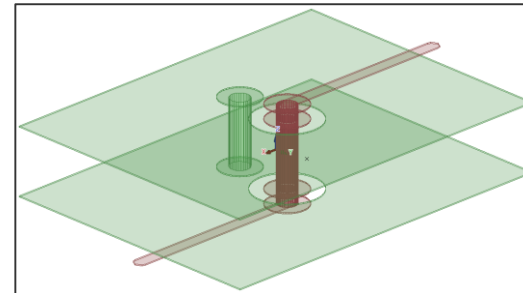
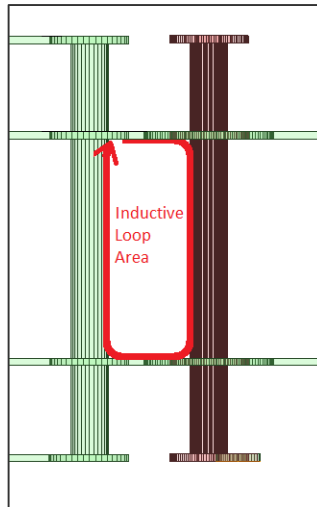
Asymmetric Signals



RETURN PATH EFFECTS

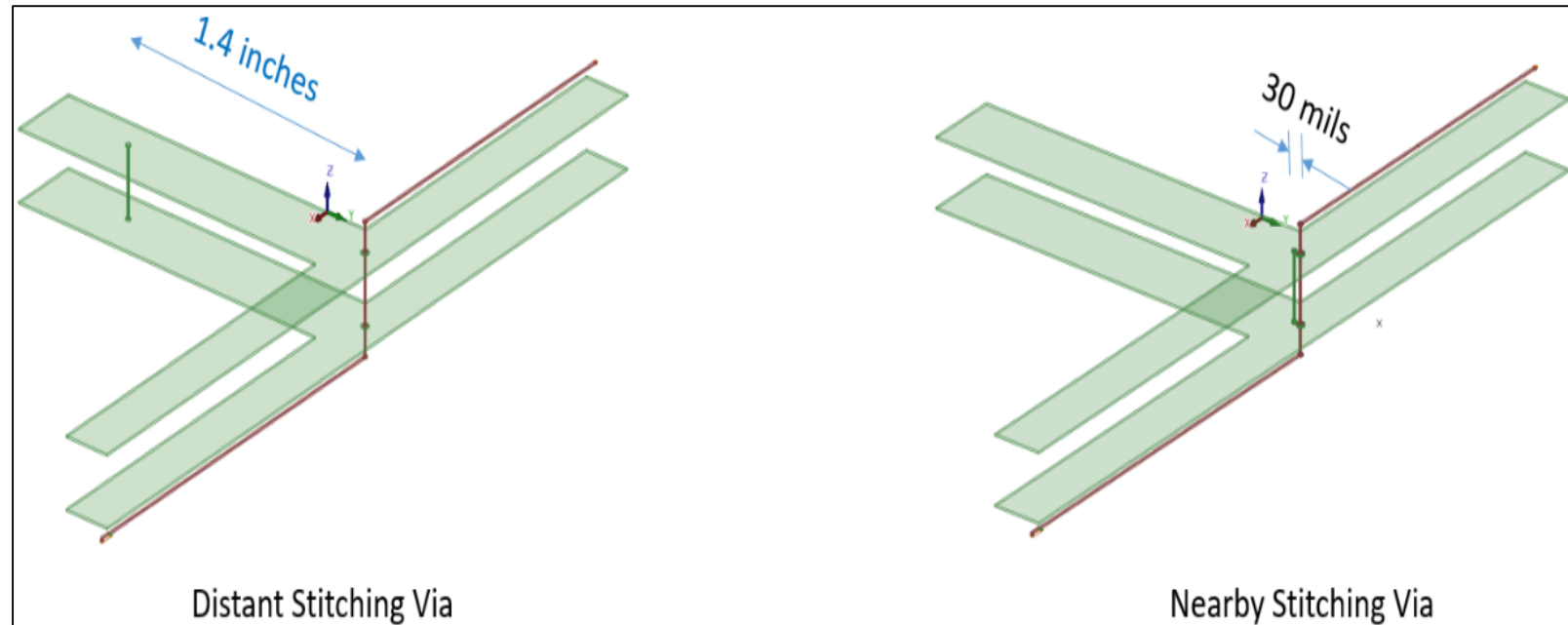
Return Path Effects > Background

- Channel's characteristics must take into account return path
- If return path is too far away, the inductive loop will adversely affect channel behavior



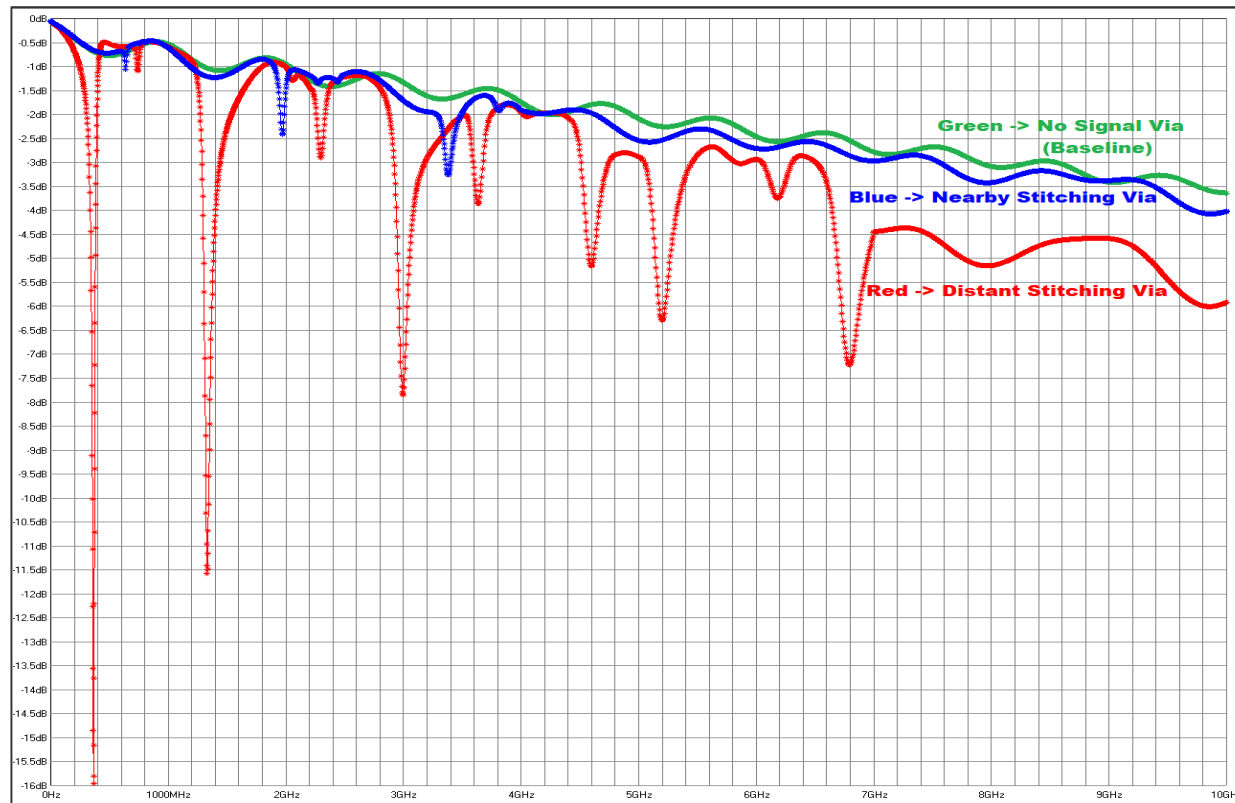
Return Path Effects > Signal Signal Setup

- Compare signal with nearby stitching via vs. distant stitching via
- Ground plane cutout to create some resonances as with many return planes
- Compare:
 - Signal via is ideal short
 - Nearby Stitching via
 - Distant Stitching via

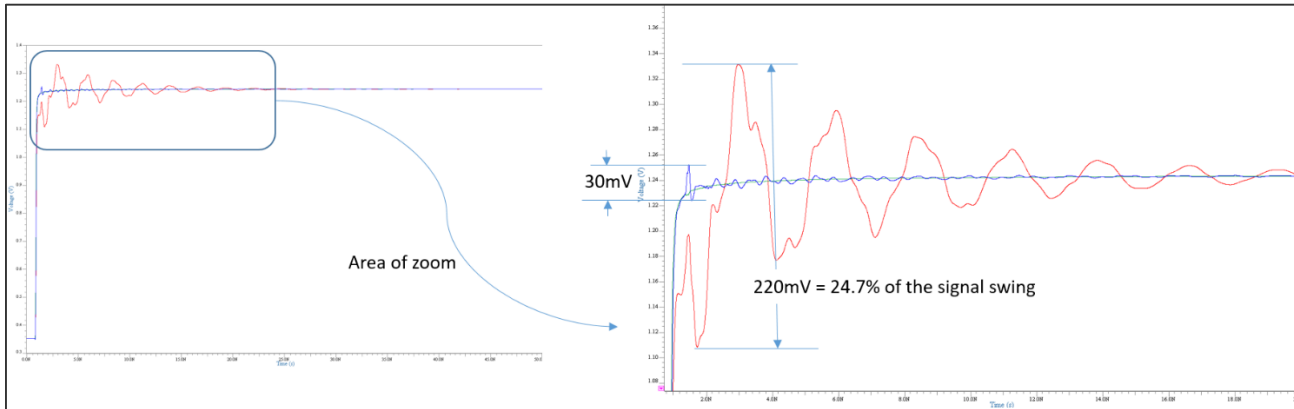


Return Path Effects > Signal Signal FD Results

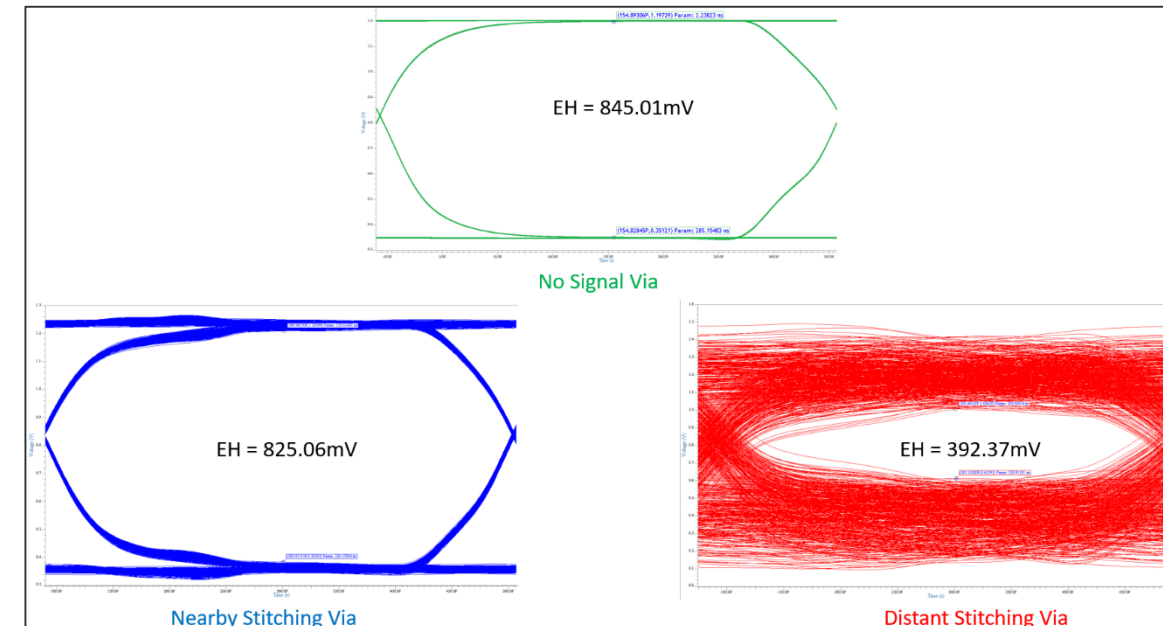
- Board edges are “visible” to channel if stitching via is far from signal via
- Nearby stitching via makes signal close to ideal



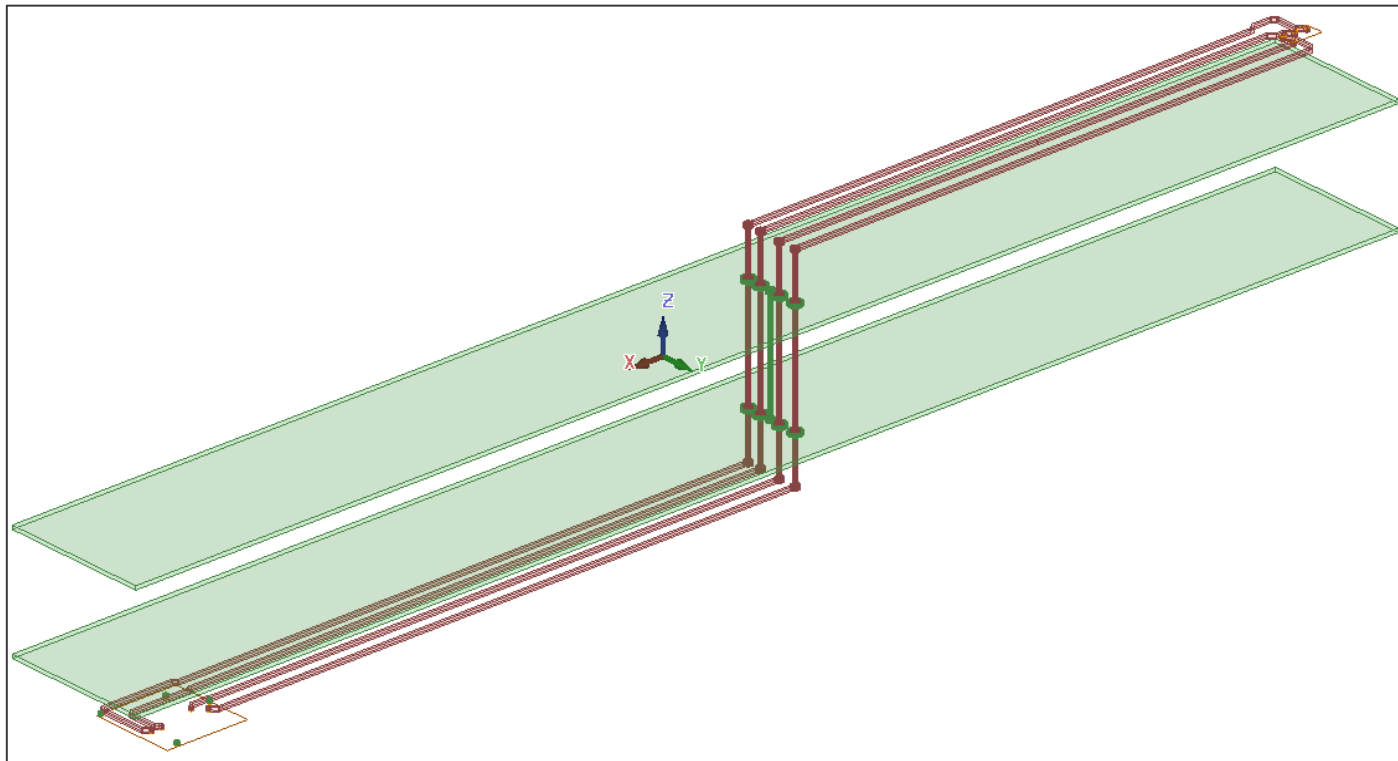
Return Path Effects > Signal Signal TD Results



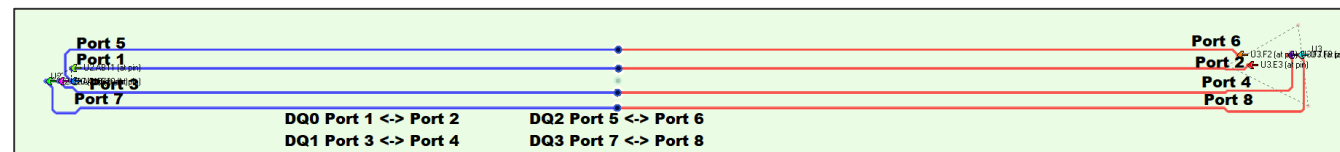
- Nearby Stitching closes eye by about **20mV**
- Distant Stitching closes eye by about **450mV**



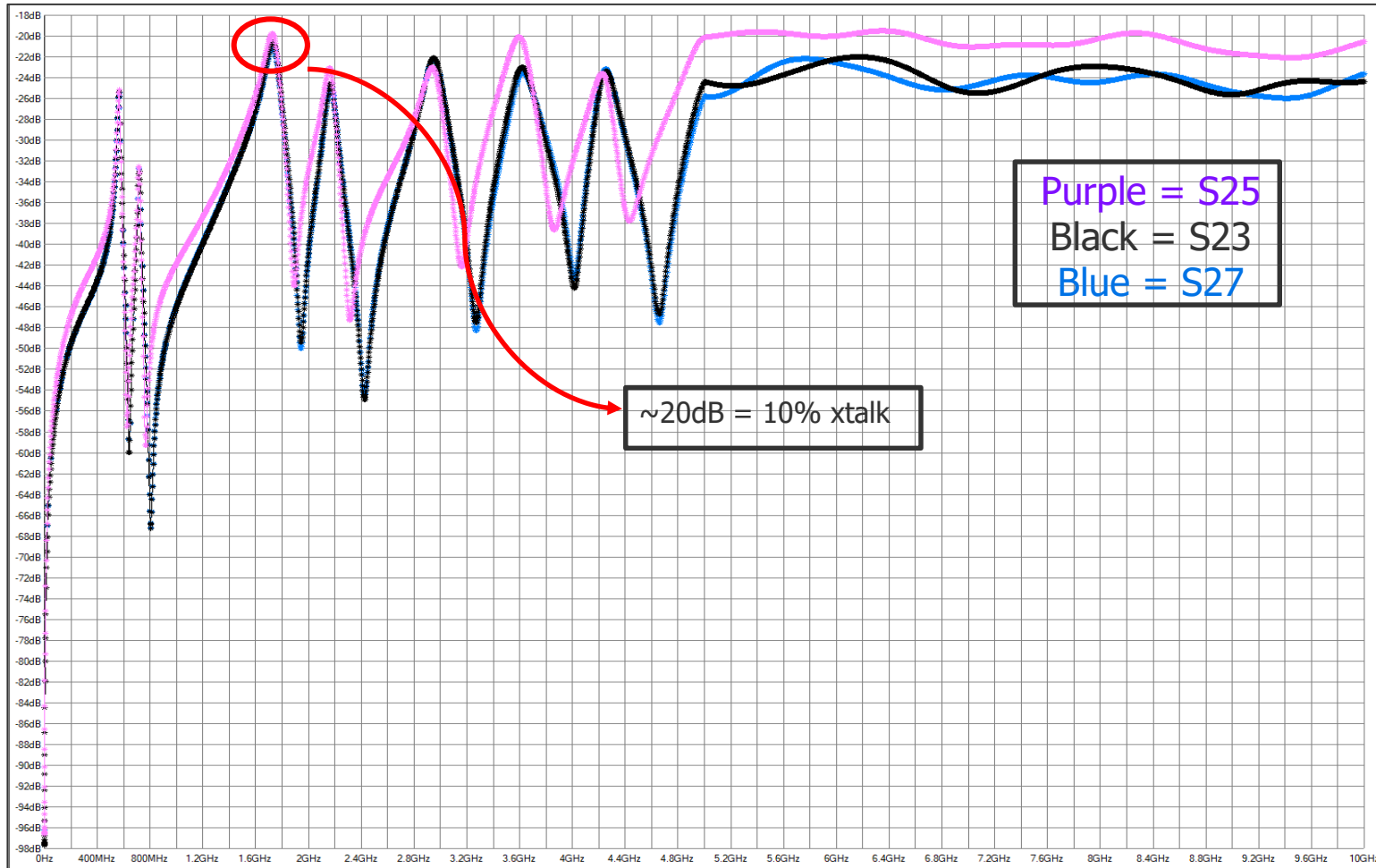
Return Path Effects > Crosstalk Setup



- One Stitching Via being shared by four signals
- 8 mil wide traces
- Outer two signals are separated by 50 mils
- Inner two signals are separated by 80 mils

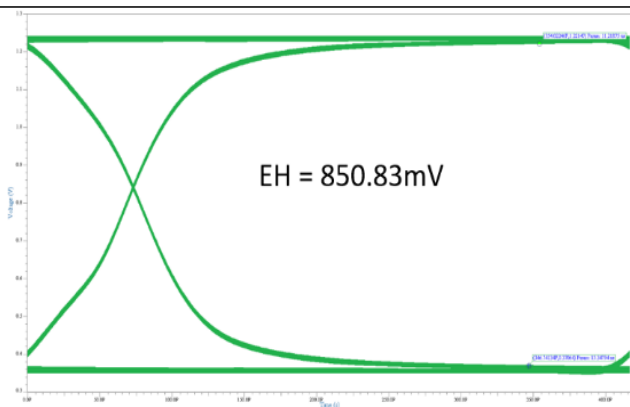


Return Path Effects > Crosstalk FD Results

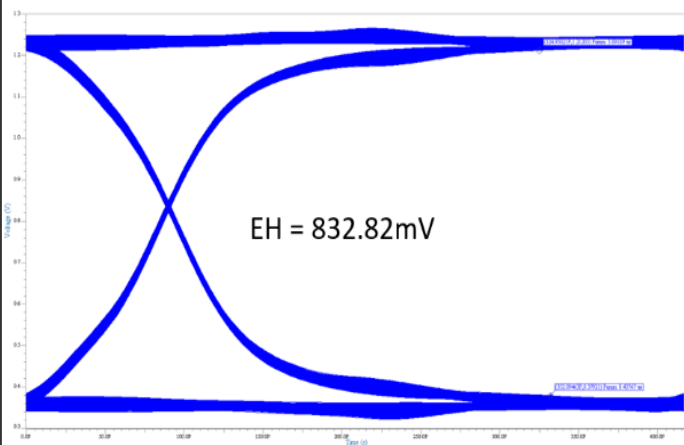


Return Path Effects > Crosstalk TD Results

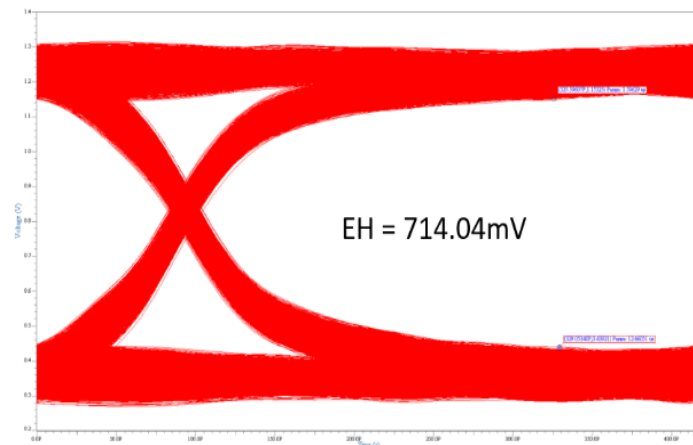
- Crosstalk closes eye by about **135mV**



No Signal Via



Only DQ0 Toggling



All Signals Toggling

Why is DDR More Susceptible?

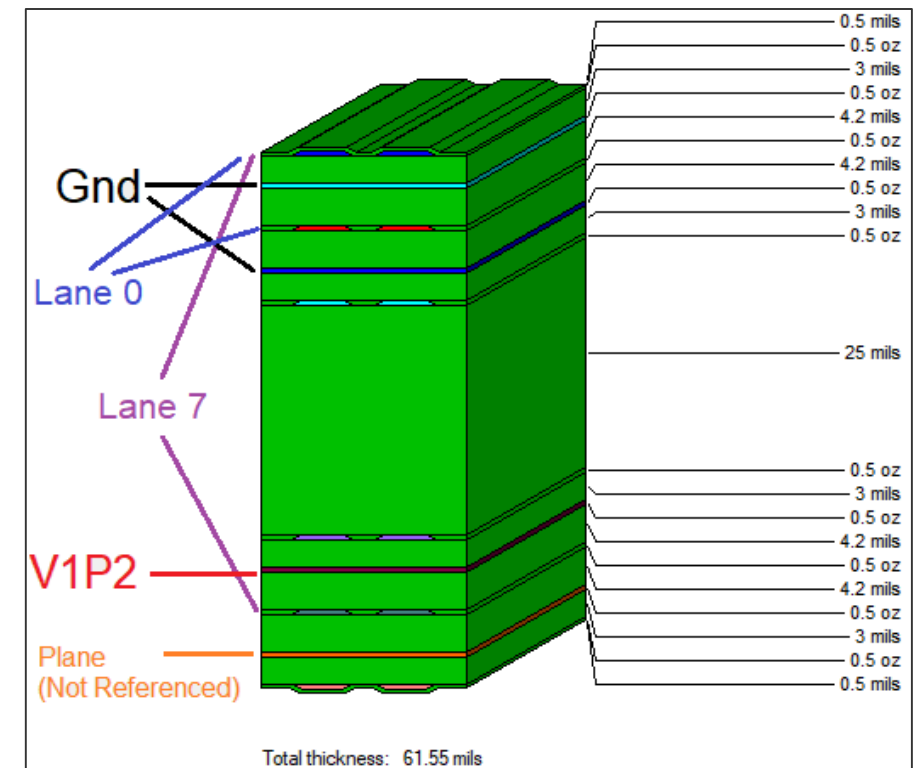
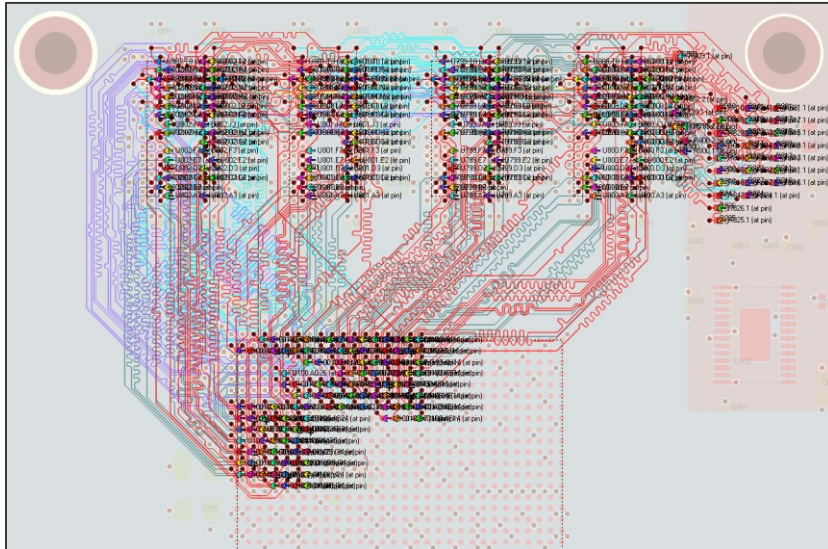
- Single Ended Signals without dedicated return path structures
- Ground vias often not explicitly thought through during design



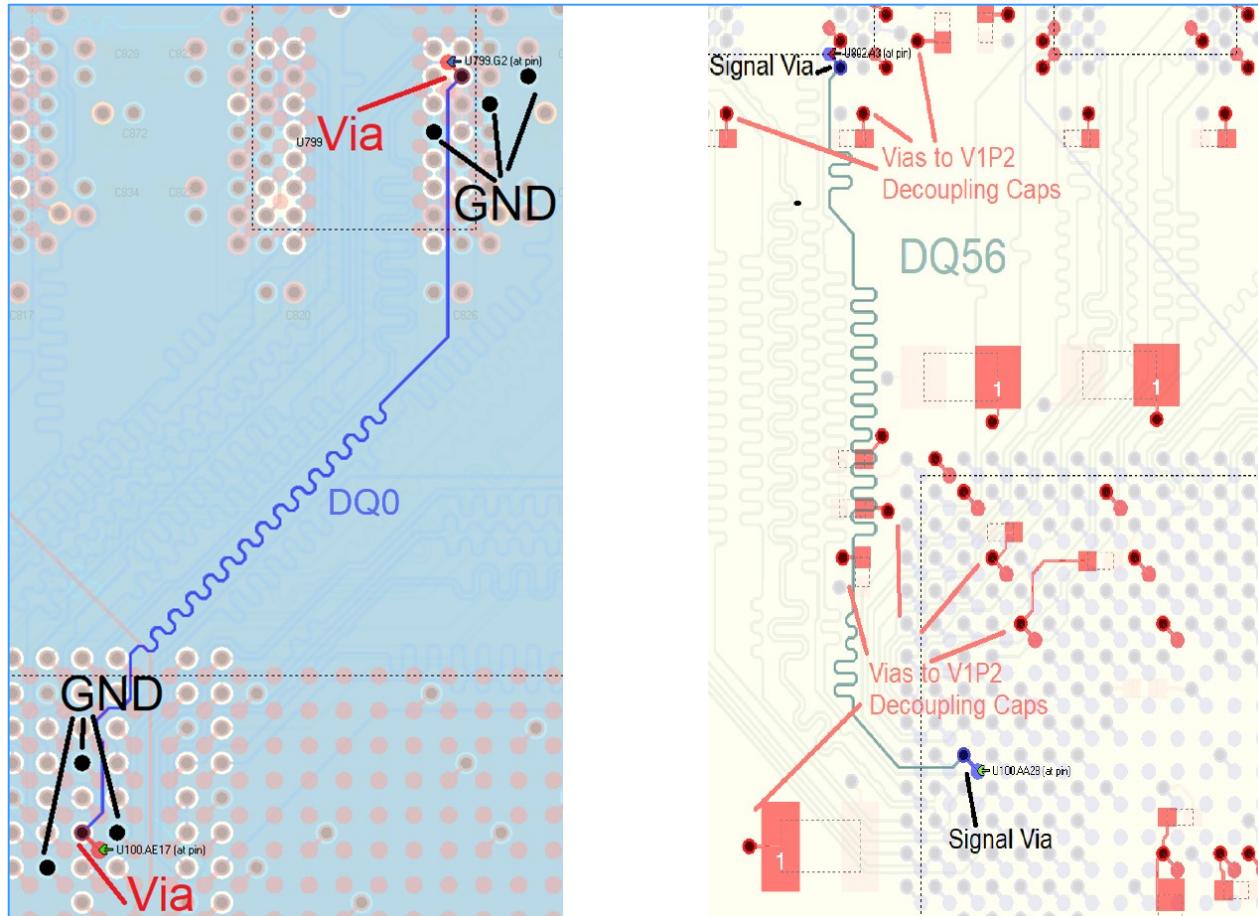
EFFECTS ON TEST CASE

Bringing it all together – Test case

- DDR4 2400 MT/s
- Lane 0 (DQ0) traverses layers 1 and 3
- Lane 7 (DQ56) traverses Layers 1 and 8
- x16 DRAM driving 2400MT/s DDR4 signal

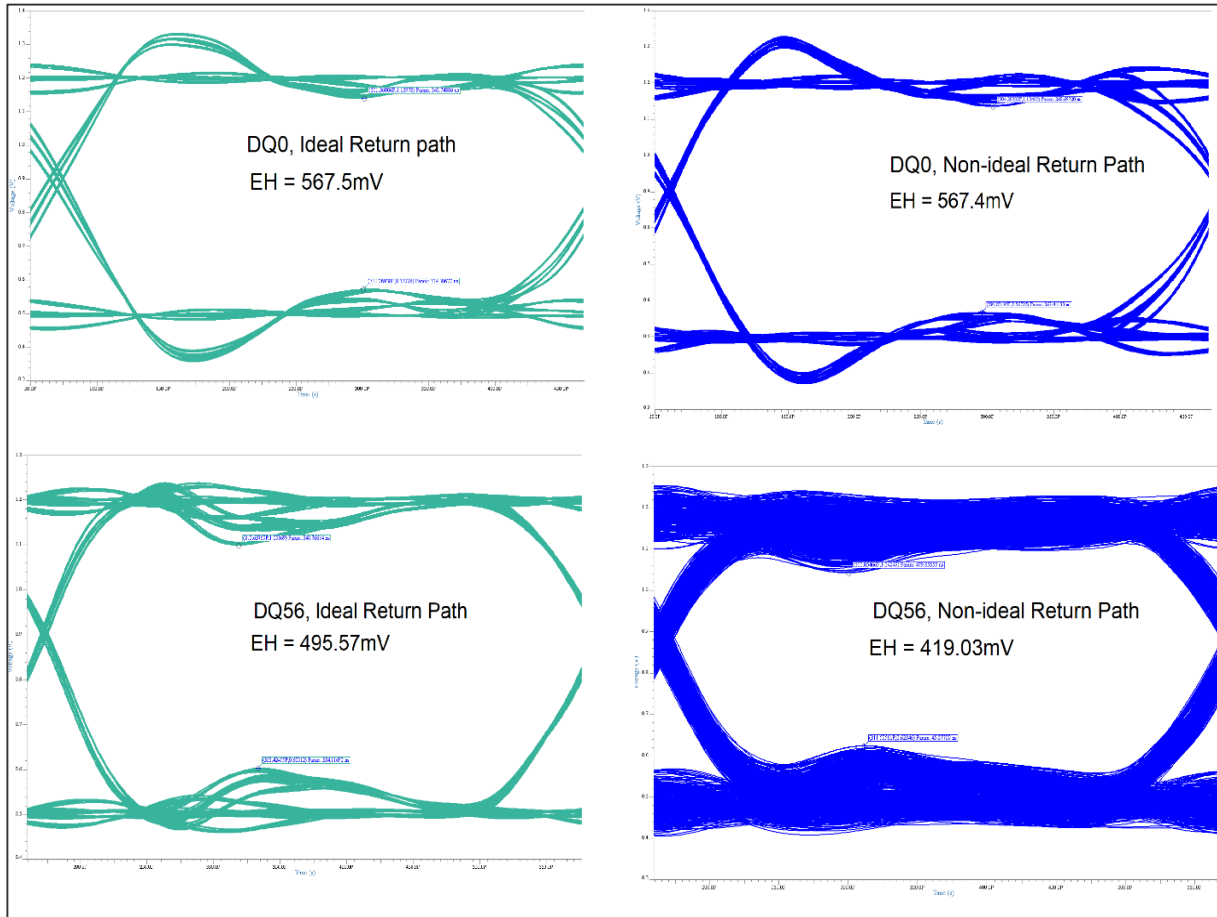


Signal layout – DQ0 and DQ56



- DQ0 does not change reference layers
- DQ56 changes reference layers, but does not have nearby decoupling caps

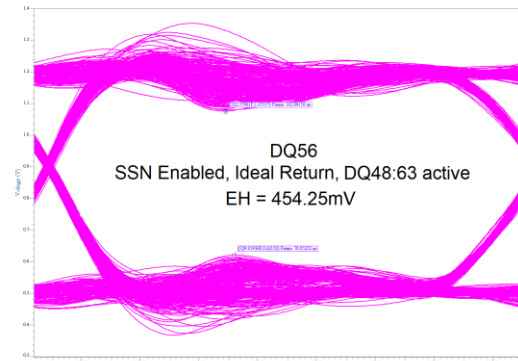
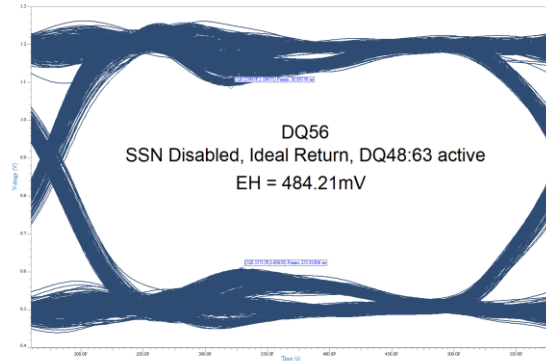
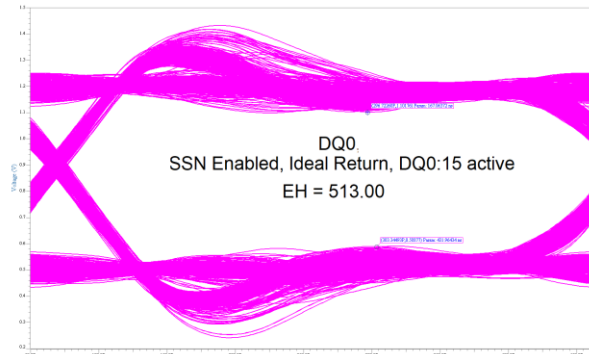
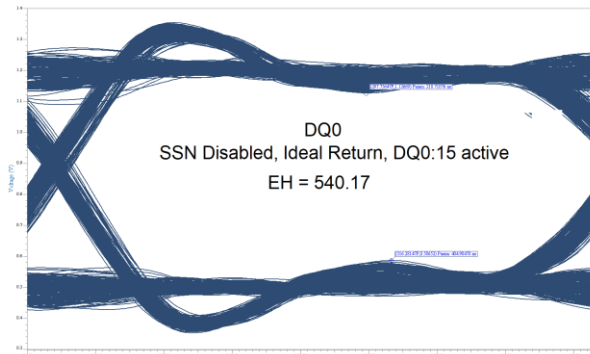
Return Path Effects - Single Signal



	Eye Height with ideal return assumption	Eye Height with actual return path	Impact of imperfect return path
DQ0	567mV	567mV	< 1mV
DQ56	496mV	419mV	77mV

- Baseline assumes signal via has ideal return path
- Single signal active – effect purely due to channel return path discontinuity

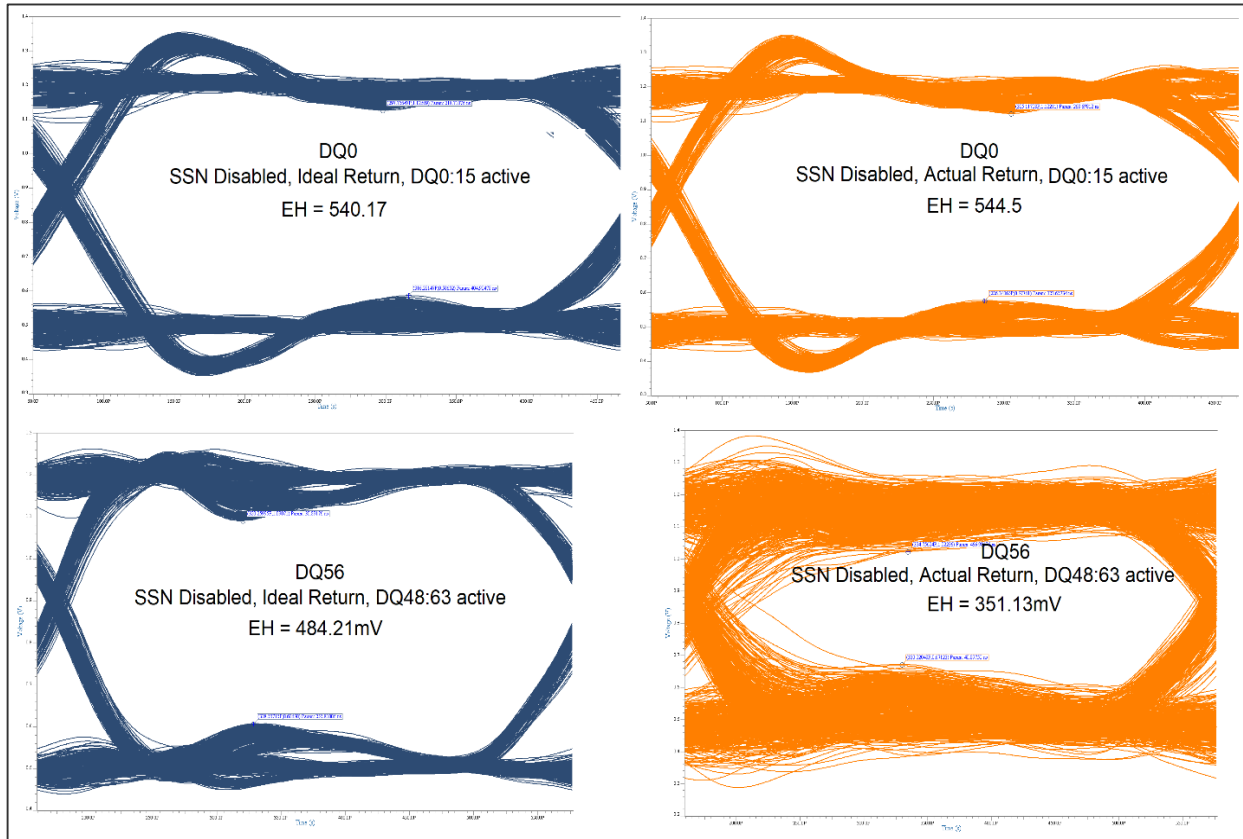
Effect of SSN



	Eye Height baseline with no power effects	Eye Height with SSN	Impact of SSN
DQ0	540mV	513mV	27mV
DQ56	484mV	454mV	30mV

- Baseline has 16 bits toggling and incorporates package xtalk
- Both DQ0 and DQ56 have about **30mV** SSN.
 - Not dependent on layout

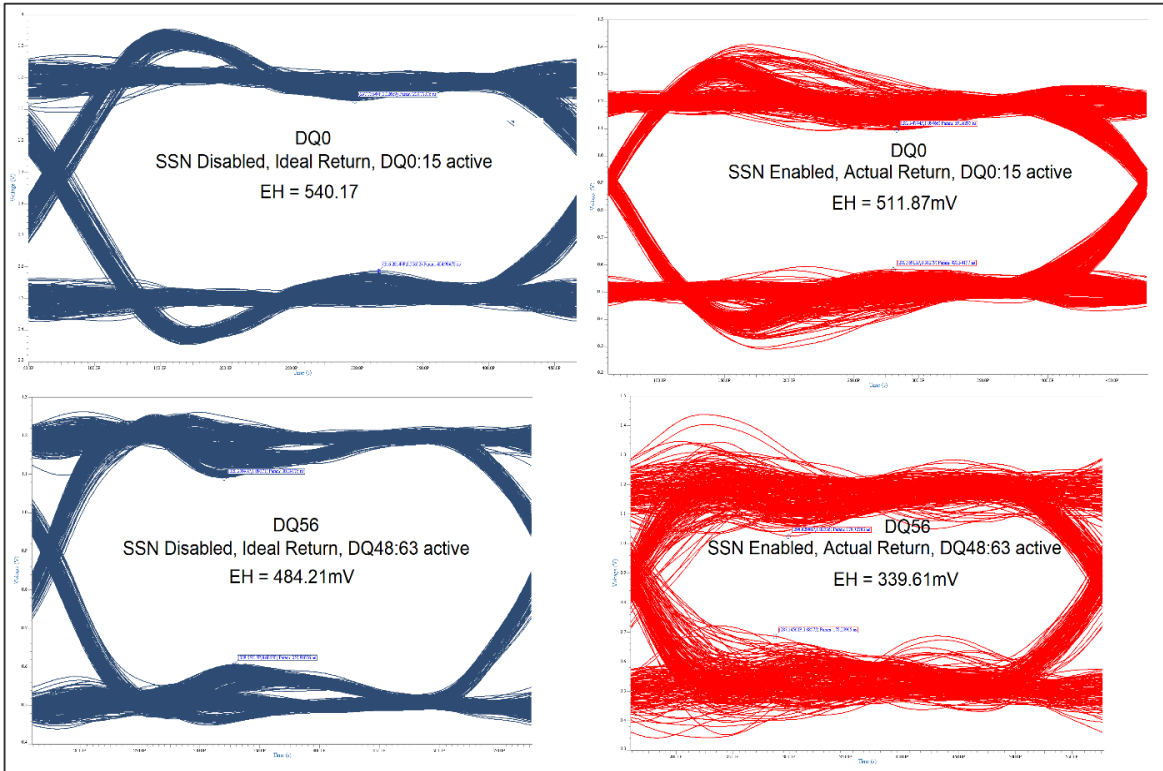
Return Path Effect - Crosstalk



	Eye Height baseline with no power effects	Eye Height with via-via crosstalk	Impact of via-via crosstalk
DQ0	540mV	544	<Negligible>
DQ56	484mV	351	133mV

- Baseline has 16 bits toggling and incorporates package xtalk
- DQ0 is very nearly unaffected by shared return path crosstalk
- DQ56 is very affected by return path crosstalk

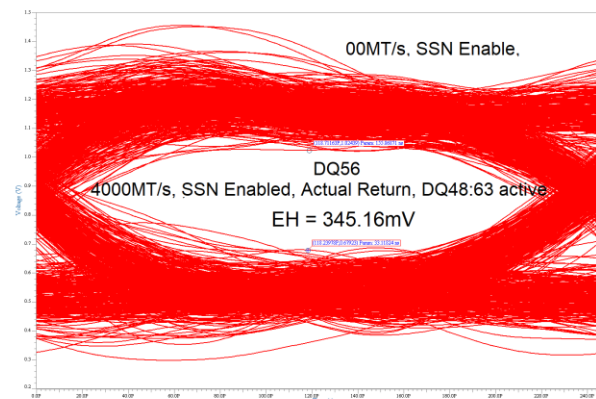
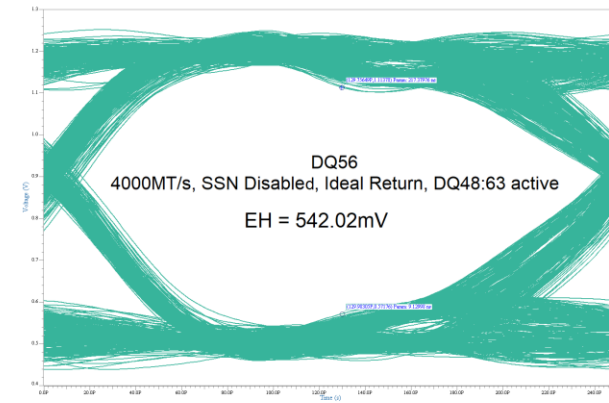
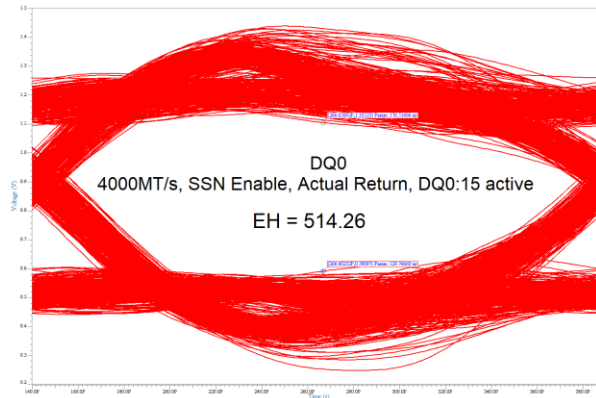
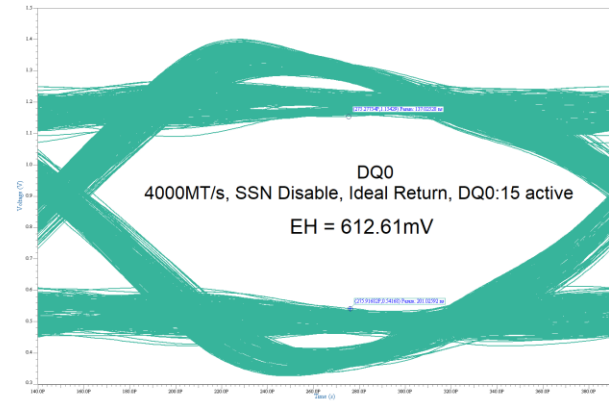
All Effects combined



	Eye Height baseline with no power effects	Eye Height with SSN and actual return path	Impact of SSN+Imperfect return path
DQ0	540mV	512	28mV
DQ56	484mV	340	144mV

- Baseline has 16 bits toggling and incorporates package xtalk
- DQ0 is primarily affected by SSN
 - Good return path layout
- DQ56 is primarily affected by return path crosstalk
 - Poor return path layout

DDR5 Data rate – 4000MT/s



	Eye Height baseline with no power effects	Eye Height with SSN and actual return path	Impact of SSN+Imperfect return path
DQ0	613mV	514mV	99mV
DQ56	542mV	345mV	197mV

- Baseline has 16 bits toggling and incorporates package xtalk
- Overclocking DDR4 IBIS at 4000MT/s
- Impact of both SSN and return path effects increase with increased data rates
- Only single signal return path effect
might be offset by DFE
— Crosstalk effects (SSN or return path) can't

THANK YOU
Q&A