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WHERE THE CHIP MEETS THE BOARD

How to Design Good PDN Filters

Istvan Novak, Samtec

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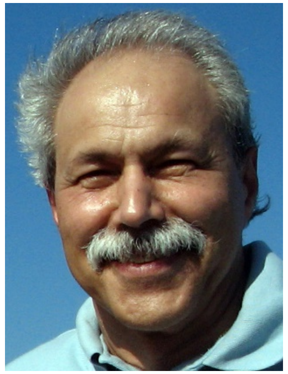
SPEAKER



Istvan Novak

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Istvan Novak is a Principle Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25um power-ground laminates for large rigid computer boards, and worked with component vendors to create a series of low-inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-five patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website.

OUTLINE

* Introduction, scope
* Requirements
* Filter design procedure
* What can go wrong
  * Wrong layout
  * Bias dependence
* Simulations and correlations
* Demos

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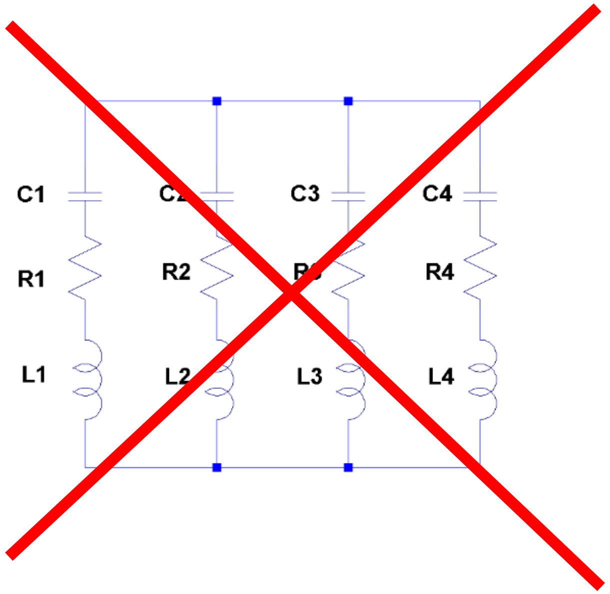
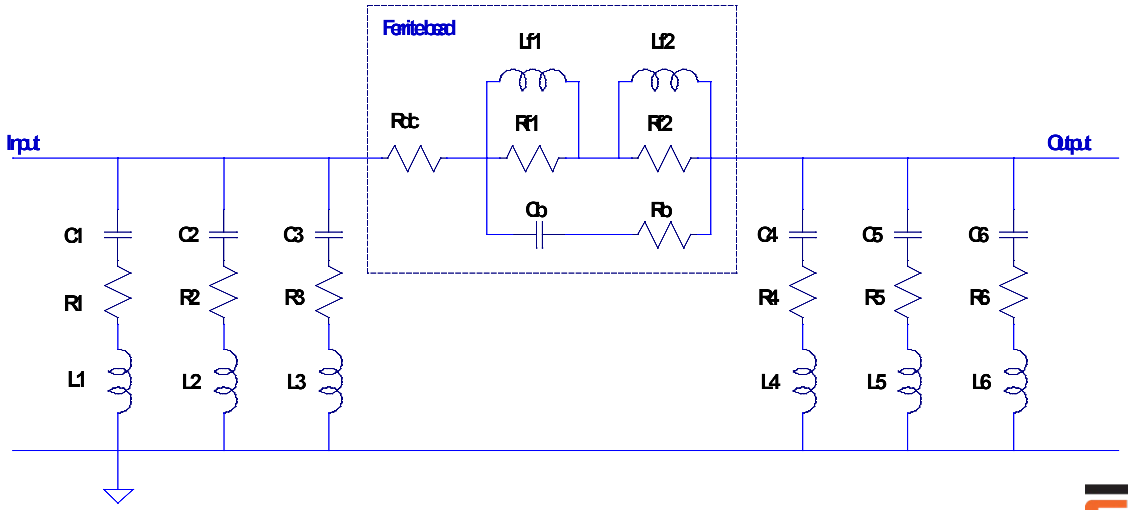
What This Is and What This Is NOT

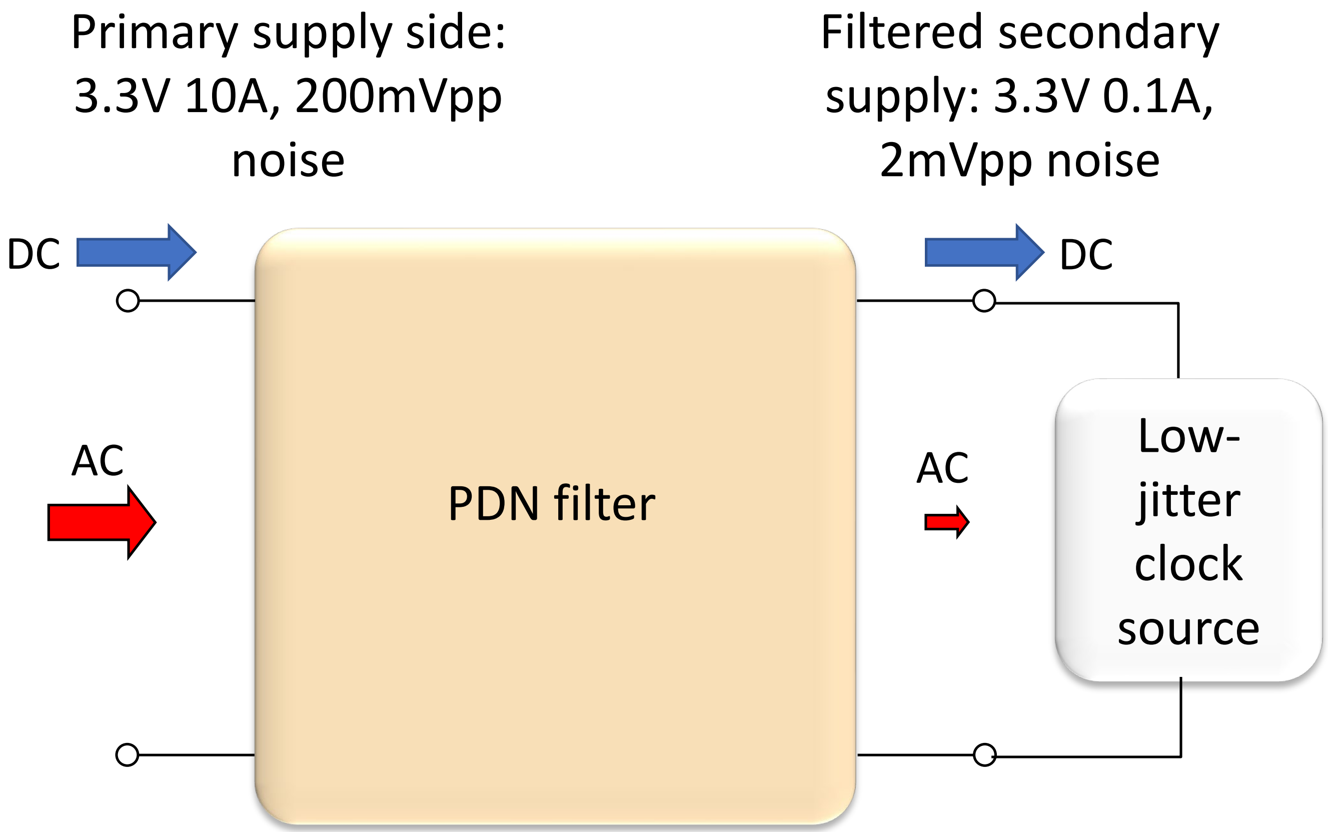


* This tutorial is NOT about all-parallel bypassing
* This tutorial is about PDN structures where series elements (whether intentionally placed or accidentally being in the circuit) matter for the performance



When We Need a Filter

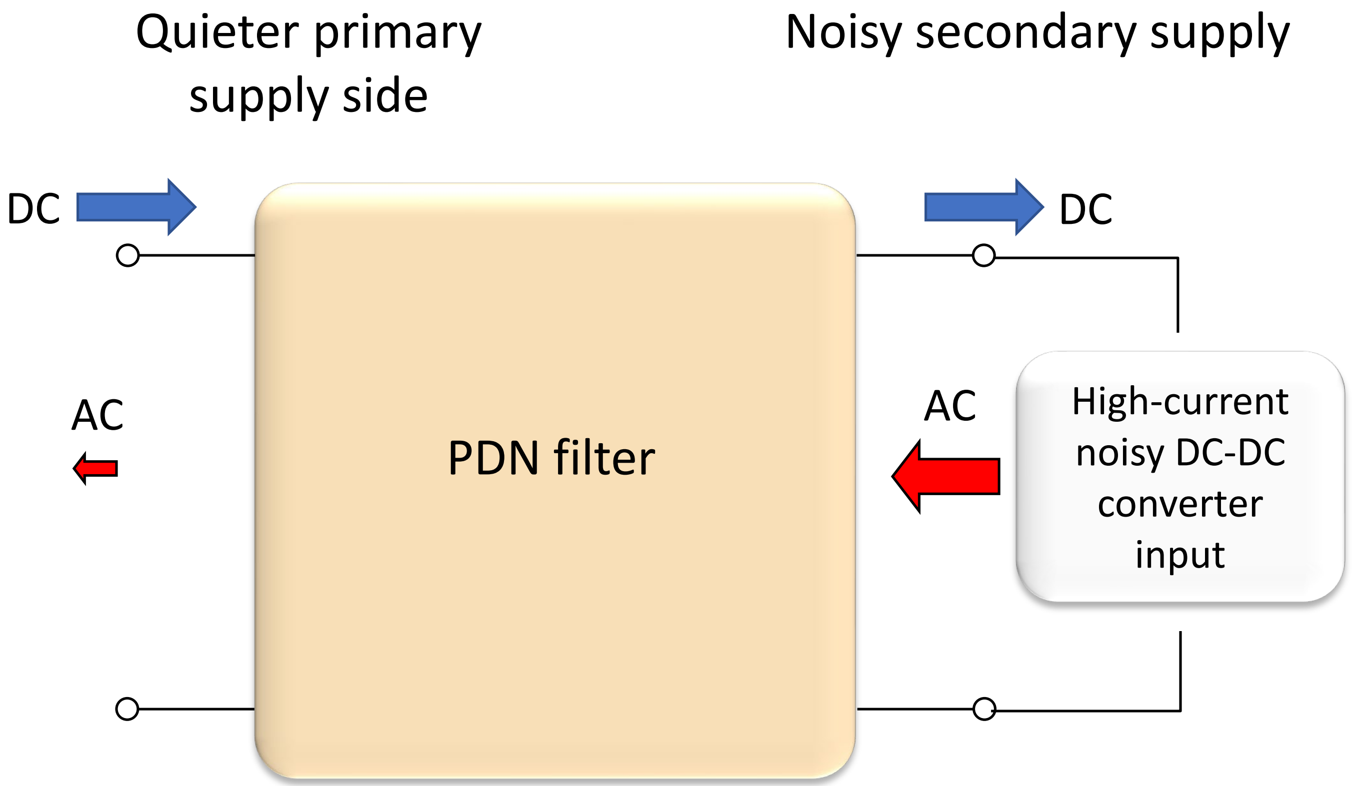
To feed a sensitive low-current load



It is easier to filter for a low-current rail than quiet a high-current rail.

When We Need a Filter

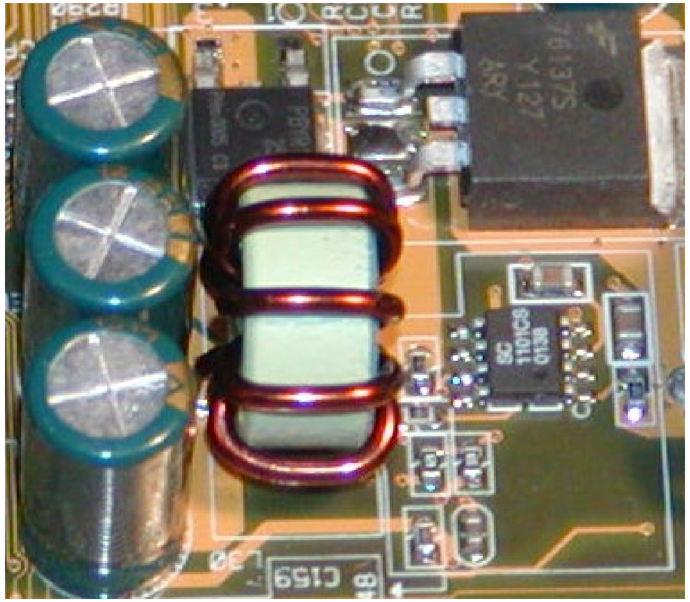
To keep noise spilling out from noisy loads

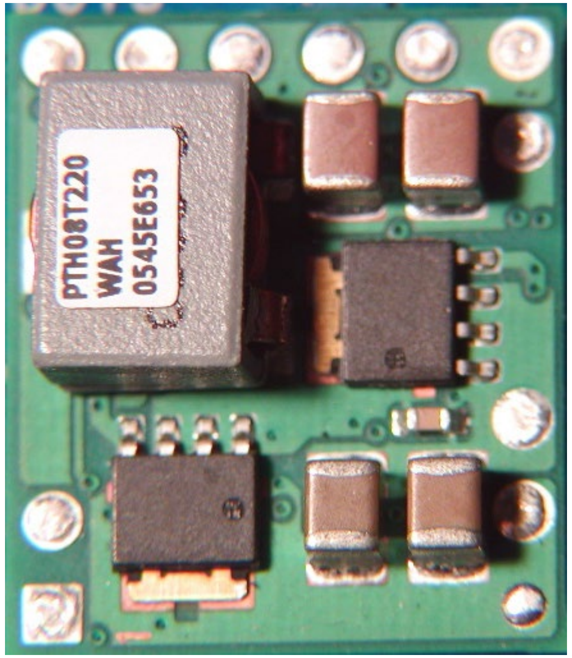


It is easier to contain noise at its source. Main stress parameter is capacitor ripple current.

Typical Noise Source

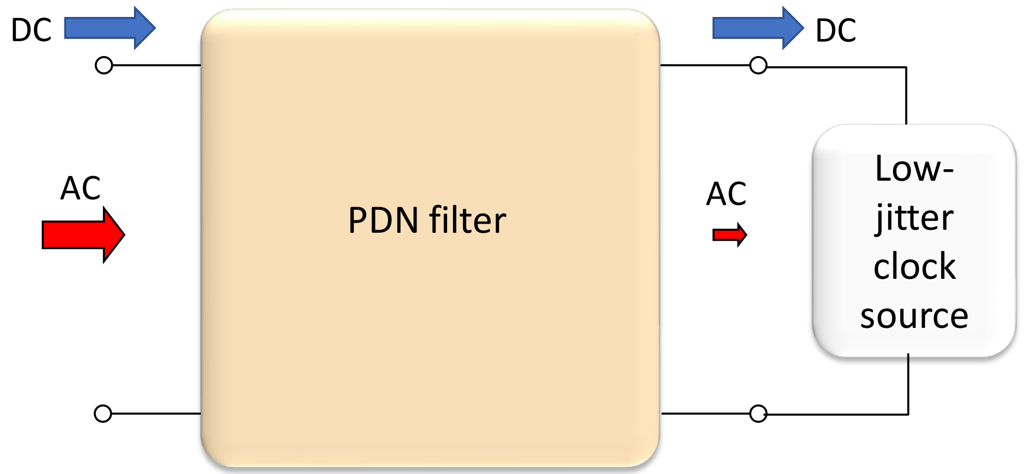
* DC-DC converters are popular and needed for their high efficiency
* They tend to generate a lot of noise

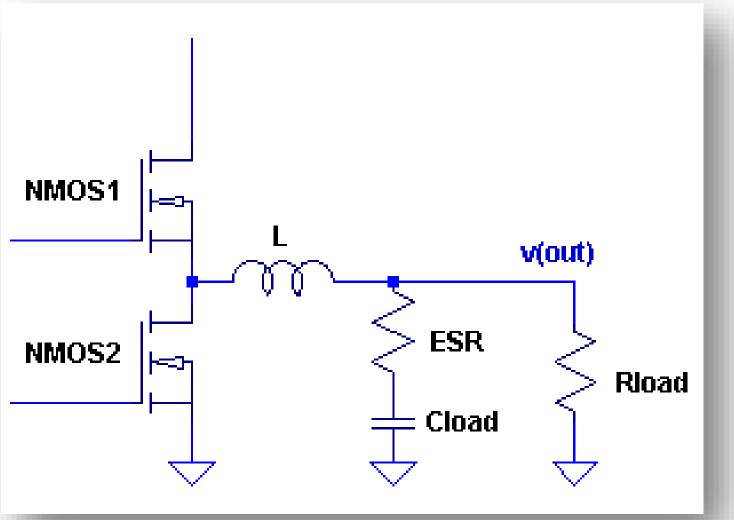


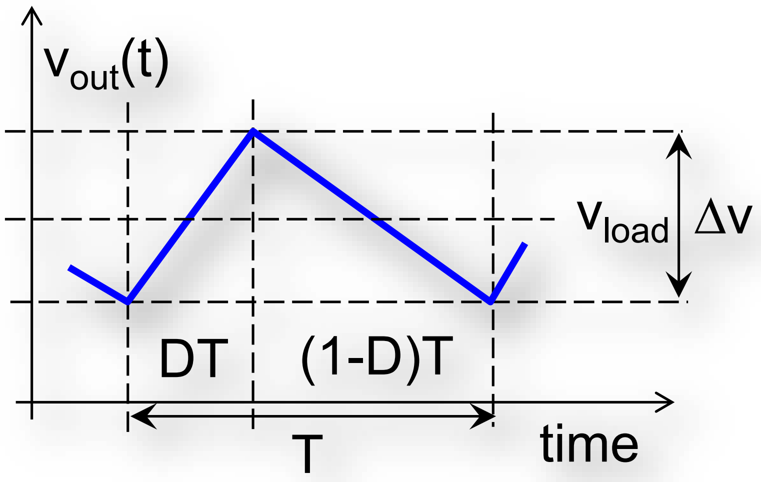


DC-DC Converter Output Ripple Voltage

- The inductor ripple current flows through the output capacitor
- First-order mid-frequency capacitor model = ESR-only
- Output ripple voltage shape closely follows inductor ripple current







If Cload*ESR pole is below Fsw, the output ripple is:

$\Delta v = ESR*\Delta I$

DC-DC Converter Output Ripple Voltage

Time-domain harmonic composition of buck converter switching ripple

	OUTPUT CAPACITORS											
	C1	C2	C3	C4	C5	Fmin [Hz]	Vin [V]	Fsw Hz]	Sweep Min	D [%]	Ripple [mVpp]	m
C [F]	4.70E-04	4.70E-05	1.00E-05	1.00E-06	3.00E-09	1.00E+03	12	5.00E+05	1	8.33	4.53	12.00
R [Ohm]	1.00E-02	3.00E-03	1.00E-02	1.00E+06	1.00E+06	Fmax [Hz]	Vout [V]	L	Max	delta_I [A]	Ripple est [mVpp]	Ratio [-]
L [H]	2.00E-09	2.00E-09	1.00E-09	1.00E-09	1.00E-10	1.00E+08	1	4.70E-07	10	3.9E+00	2.89	1.57
N [-]	3	3	10	0	0							

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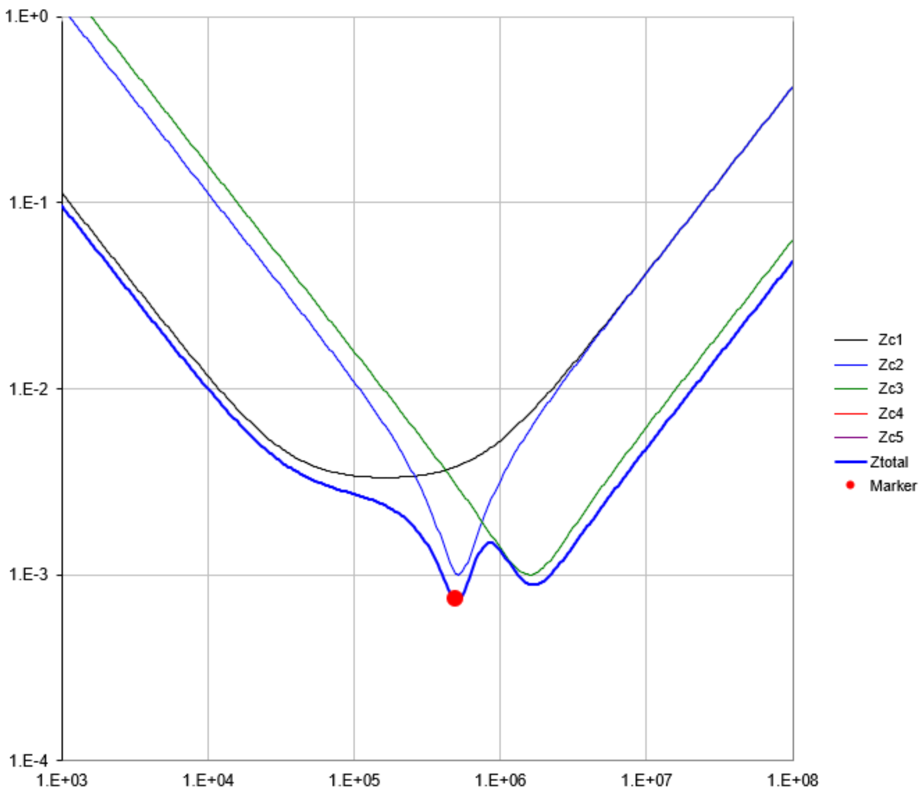
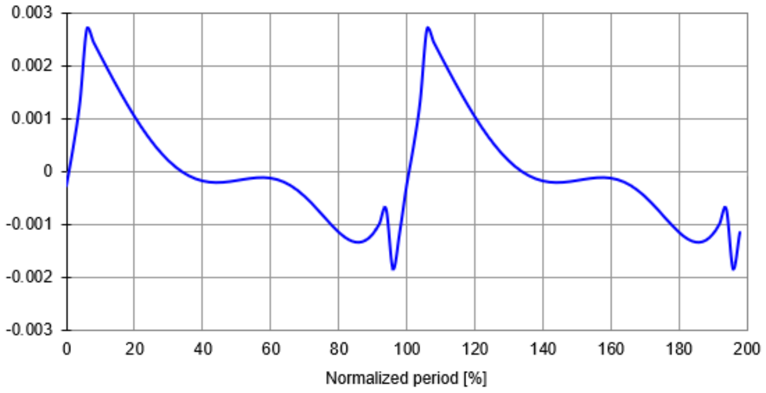
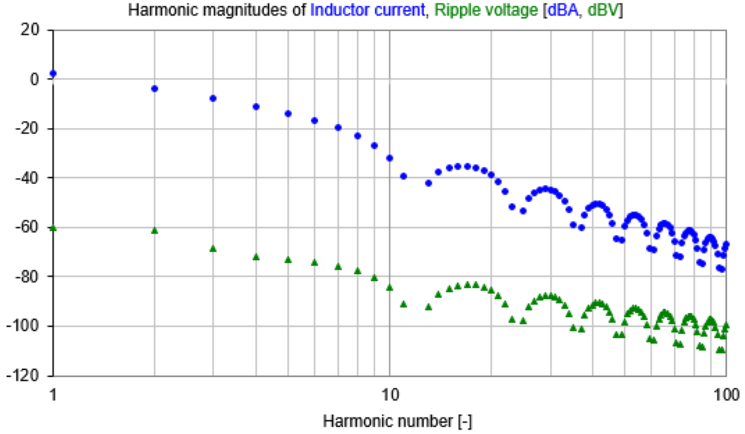
Number of periods
2

Impedance magnitude of output capacitors [Ohm]



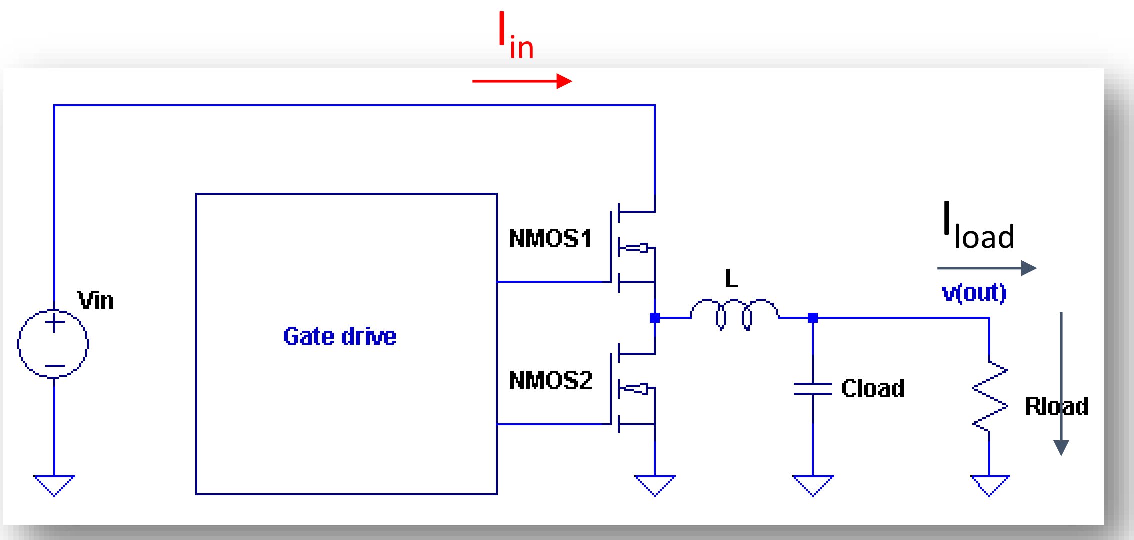


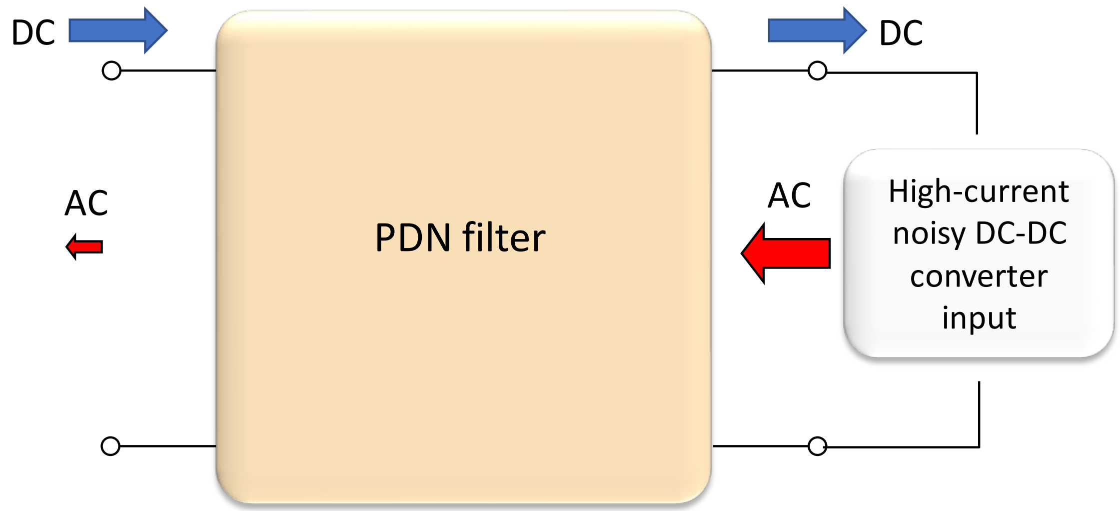


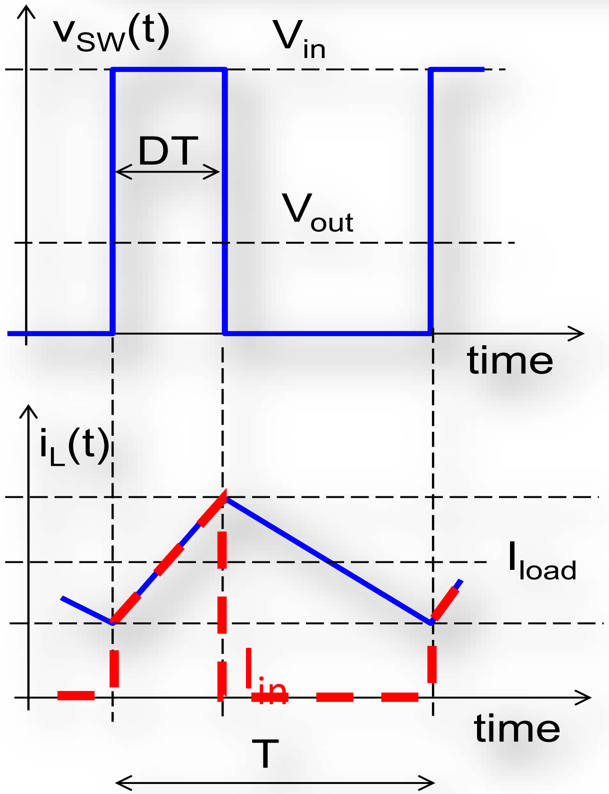
- The inductor ripple current flows through the output capacitor
- First-order mid-frequency capacitor model = ESR-only
- Output ripple voltage shape closely follows inductor ripple current

DC-DC Converter Input

- The input voltage is chopped by the switches
- Inductor current is continuous
- Input current has large jumps

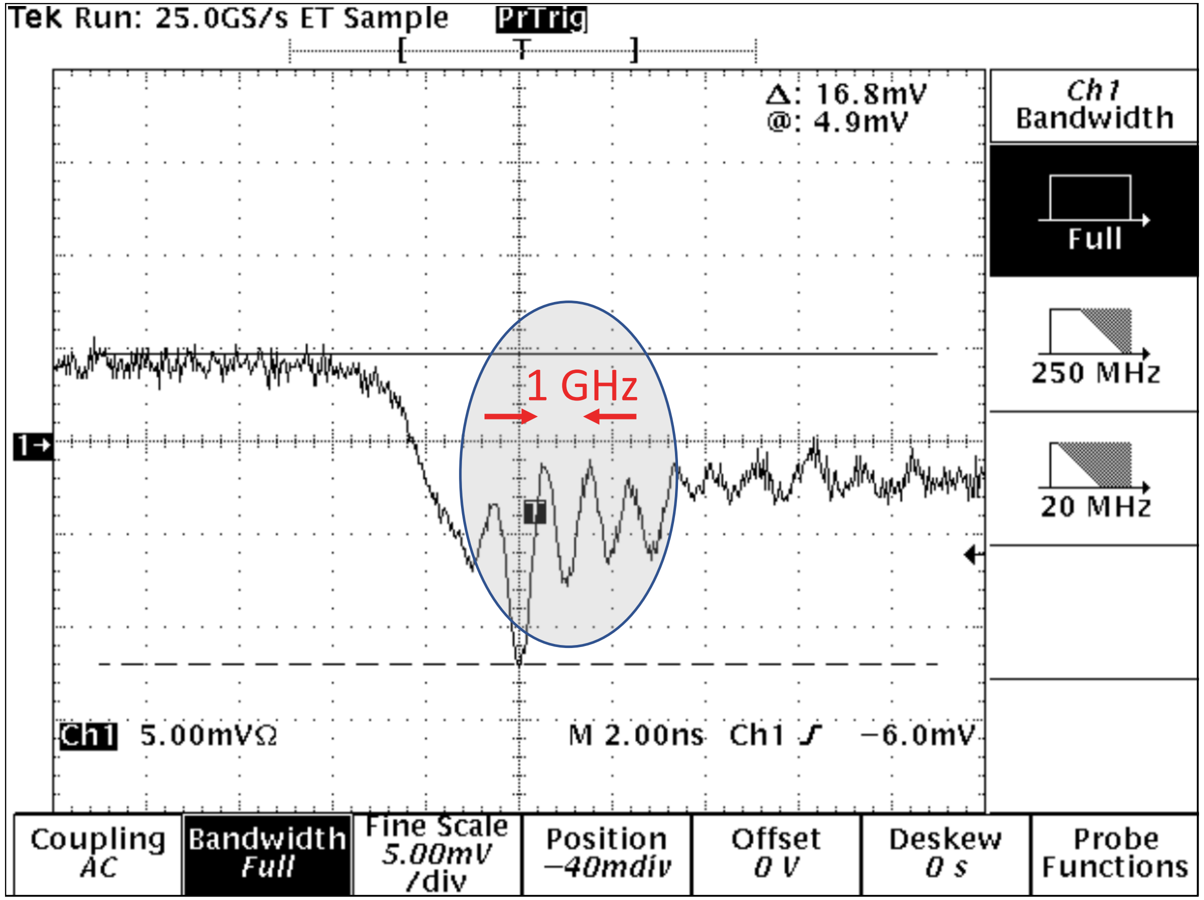


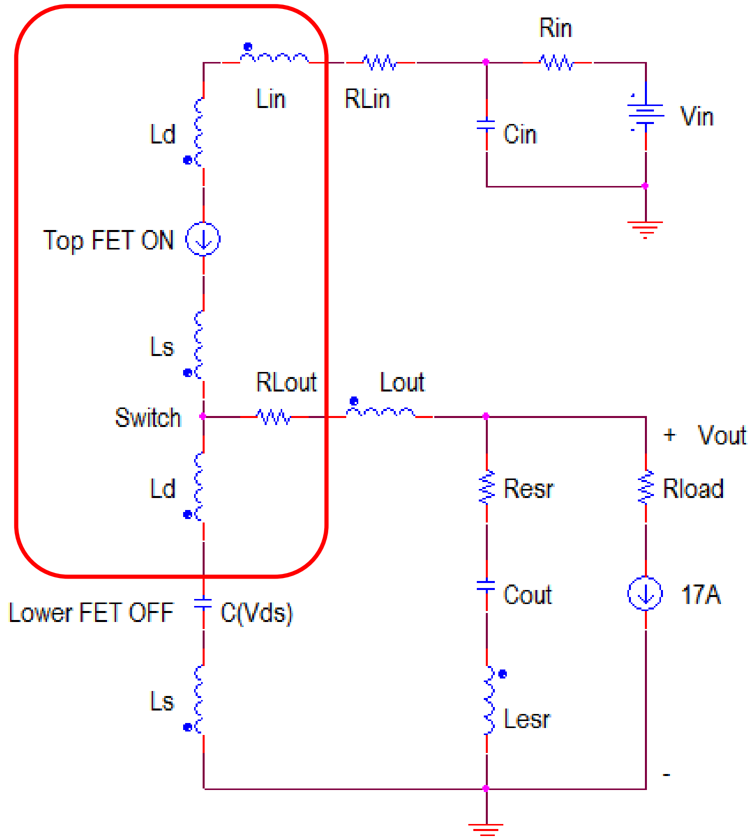




DC-DC Converter Ringing

* The switching edges may have high-frequency transients
* Ringing frequency: 50 – 1000 MHz





Source:
- Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals, DesignCon 2016
- What is New in DC-DC Converters; An OEM's Perspective, DesignCon 2012

OUTLINE

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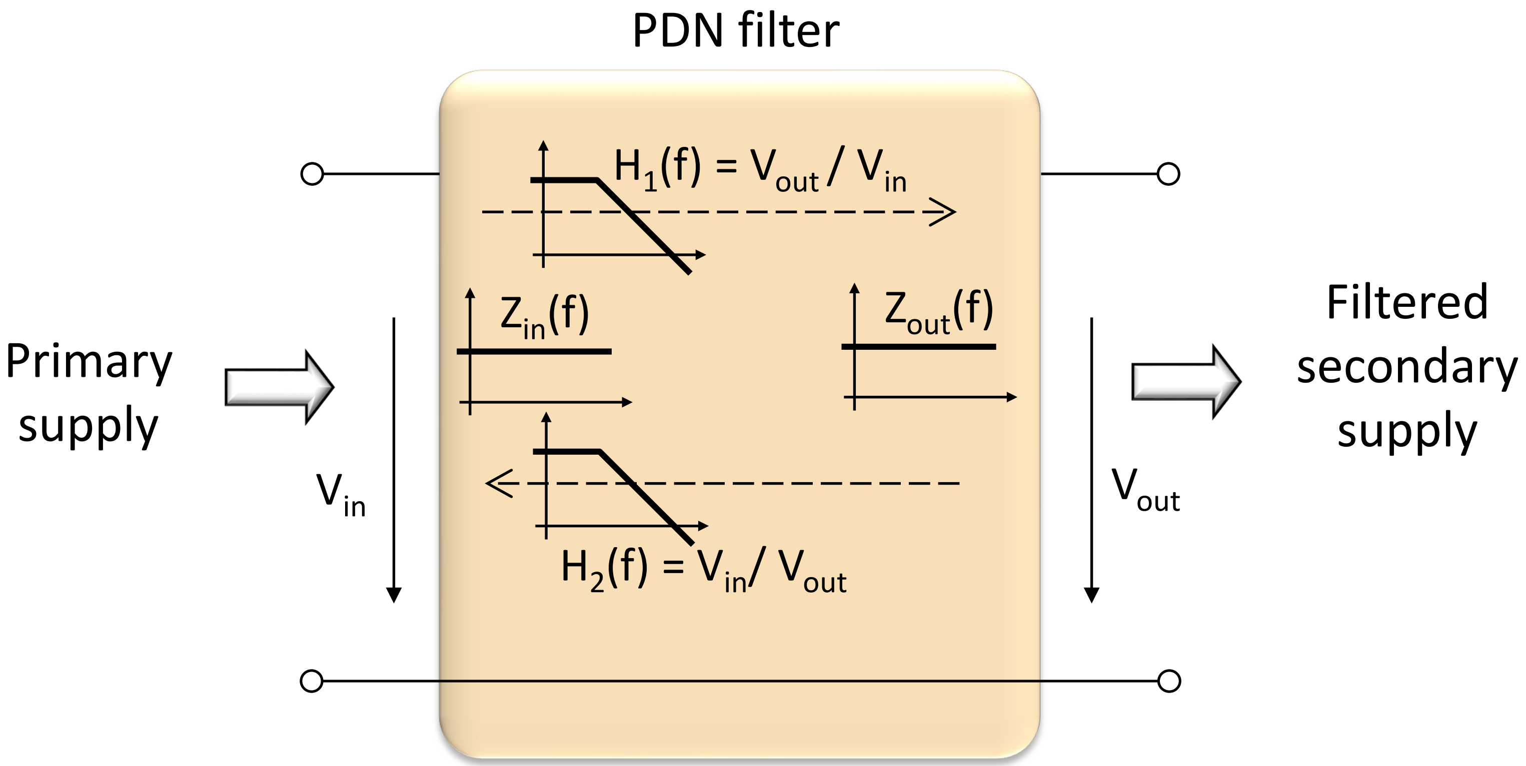
Analog Supply Noise Filter (1)



Typical noise to filter: DC-DC converter output ripple.

Analog Supply Noise Filter (2)

Possible functions and requirements:

* Low-pass filtering from main to secondary
* Low-pass filtering from secondary to primary
* Output impedance for the load (*)
* Input impedance for the source (*)

(*) Optional requirement

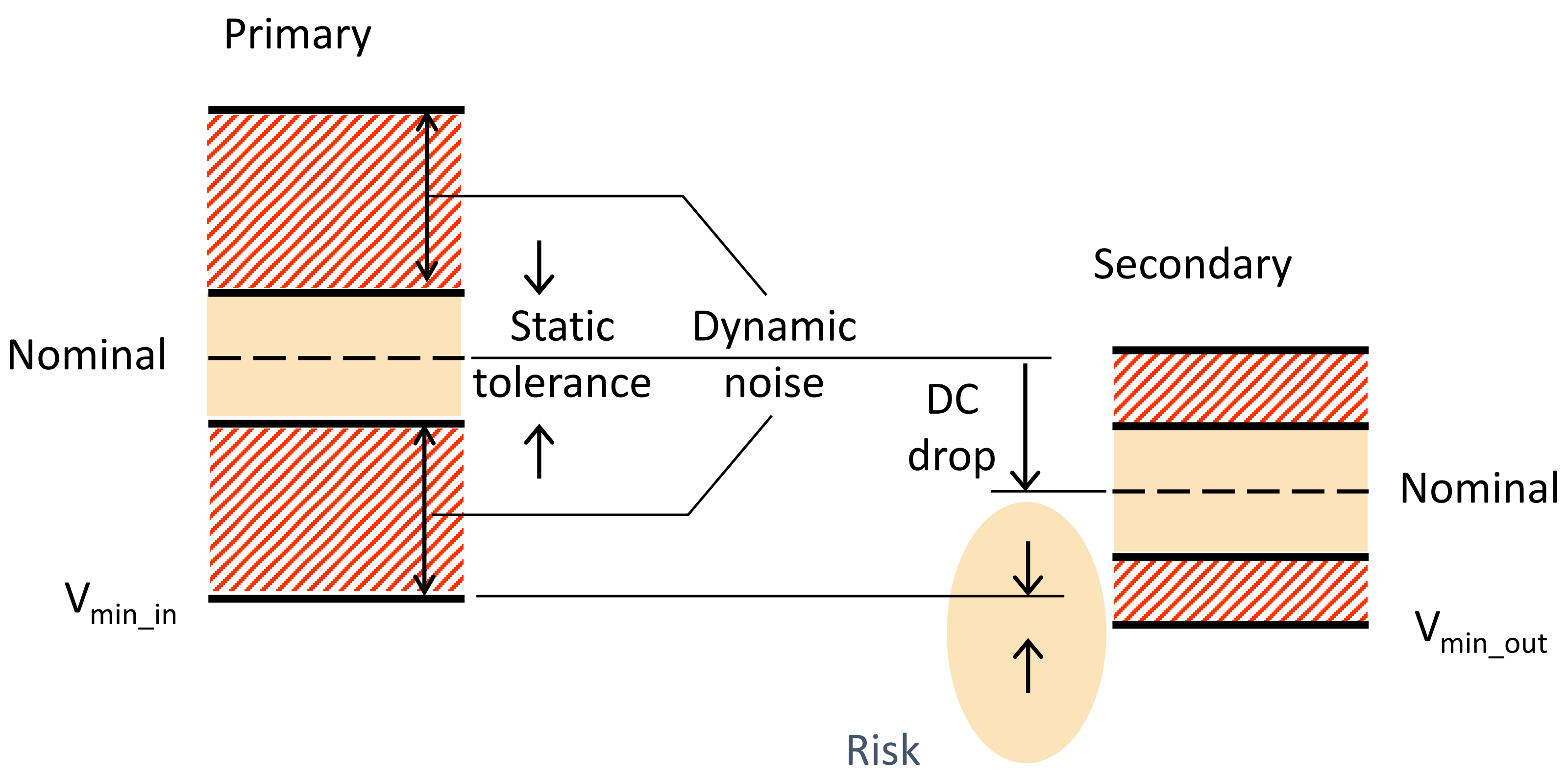
Passive filters may be physically symmetrical

Relevant transfer functions are mostly not symmetric

Watch DC voltage drops closely

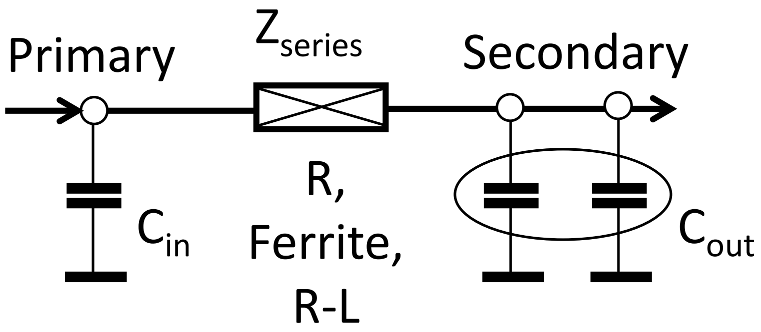
Analog Supply Noise Filter (3)

Static and dynamic budget

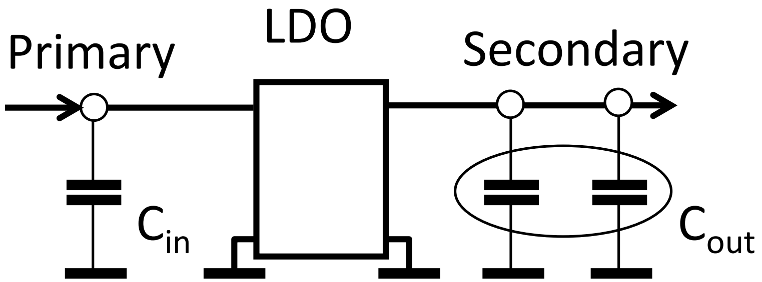


Analog Supply Noise Filter (4)

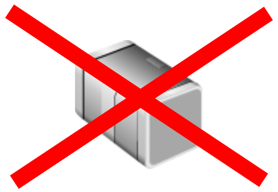
* Use low-Q inductors or ferrites, or

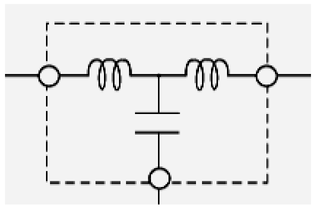


* Low Dropout Regulators



* DO NOT use Hi-Q filters

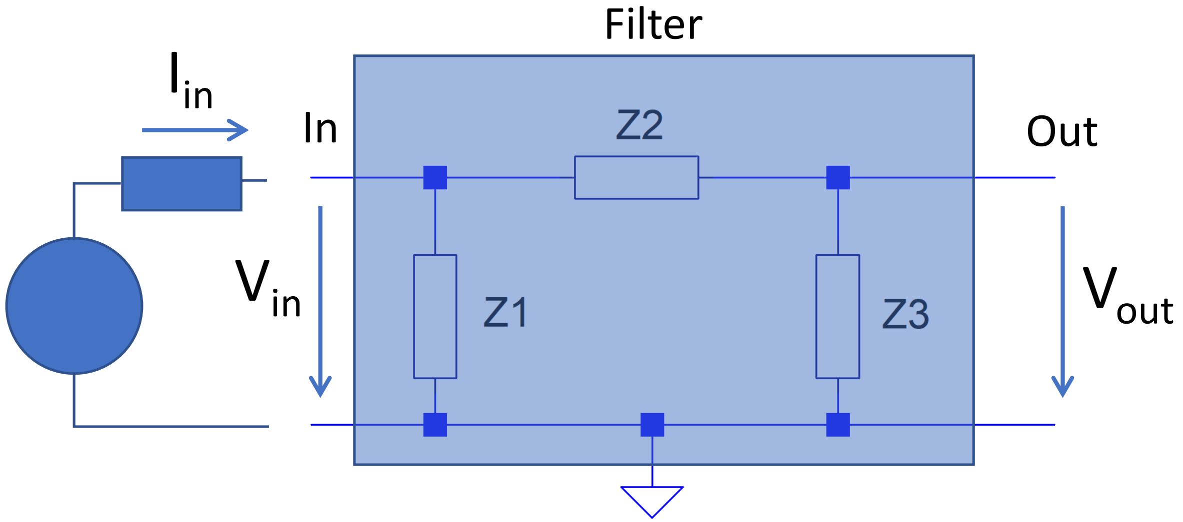


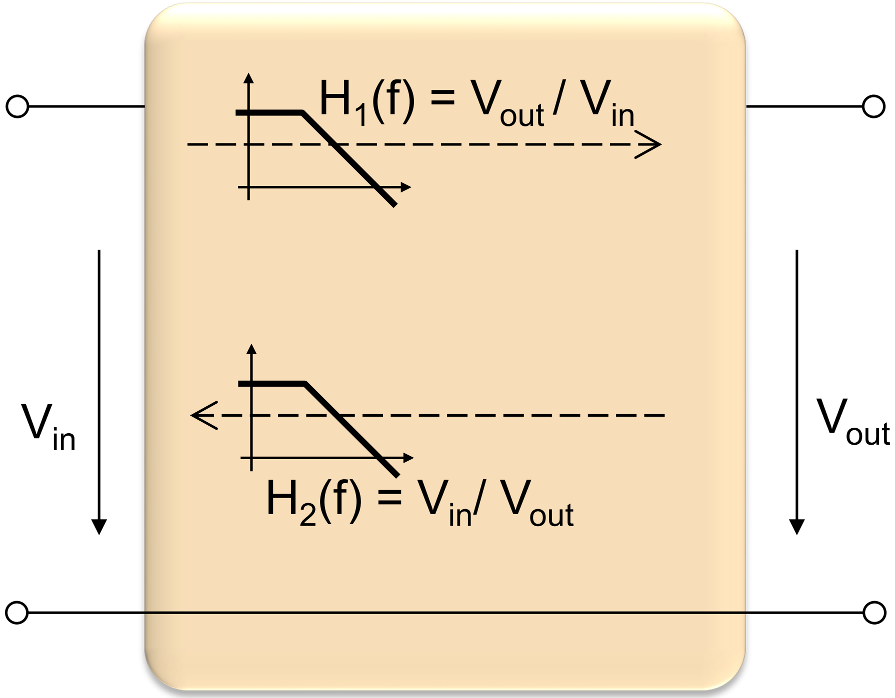


Transfer Functions

What transfer function matters?

* Z_{21} or S_{21}?
* Something else?



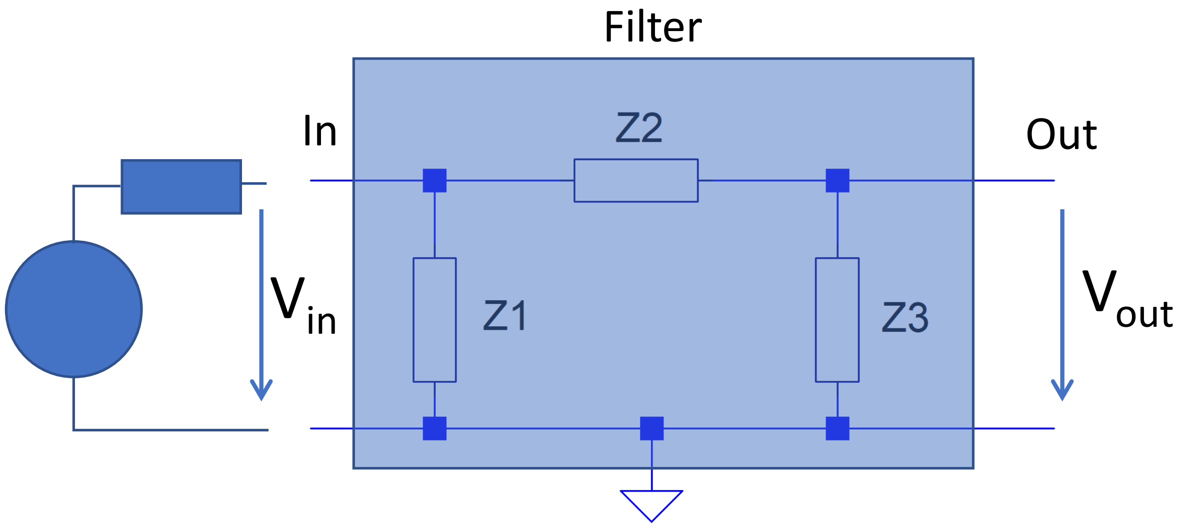


$$Z_{21} = V_{out}/I_{in}$$

$$S_{21} = wave_{out}/wave_{in}$$

Transfer Functions

For filters from a high-current to a low-current rail we need the *unloaded voltage transfer function: V_{out}/V_{in}*

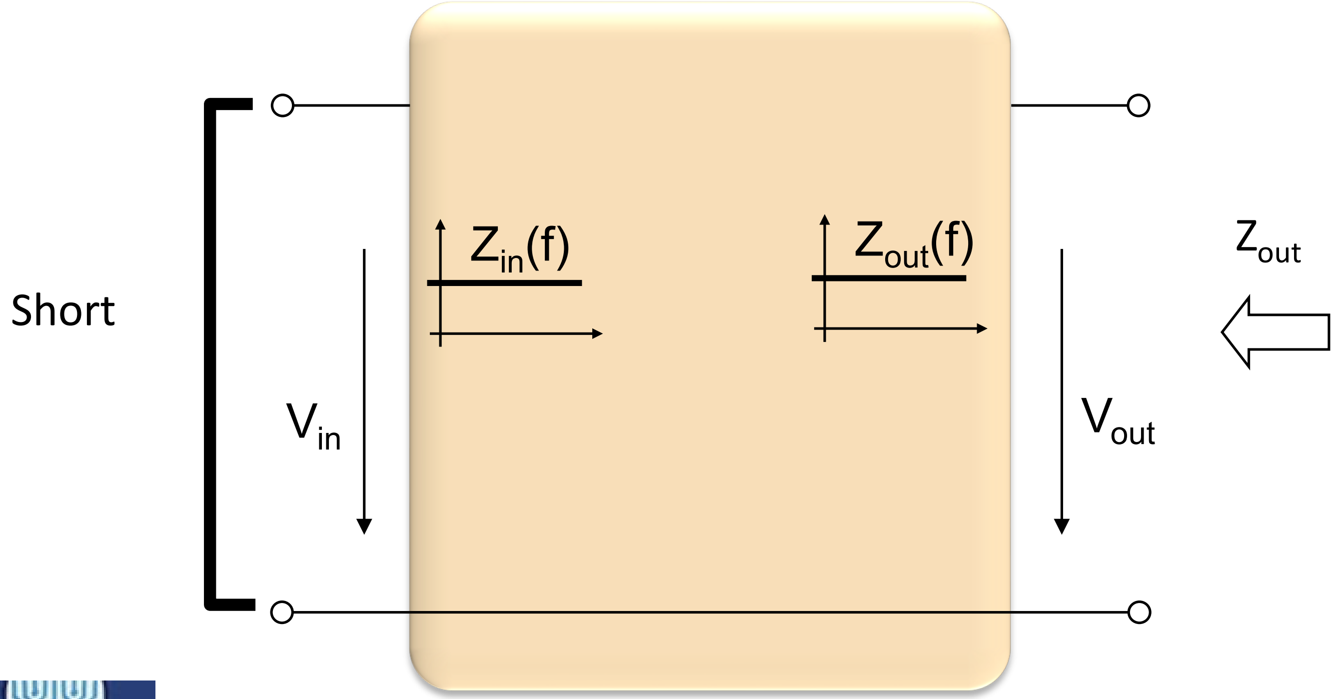


Impedances

What filter impedance function matters?

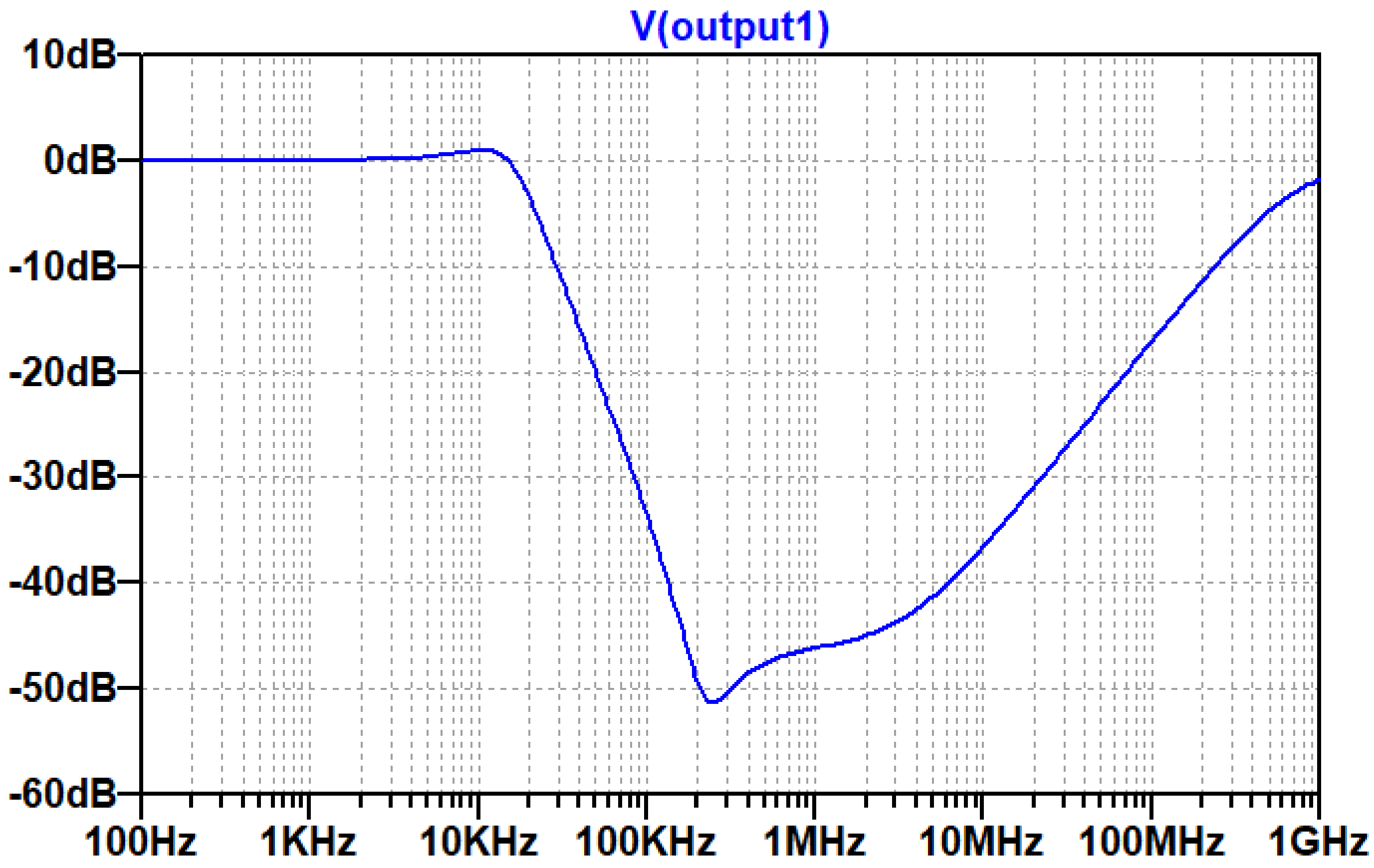
- Z_{11}, or Z_{22}?
- Something else?

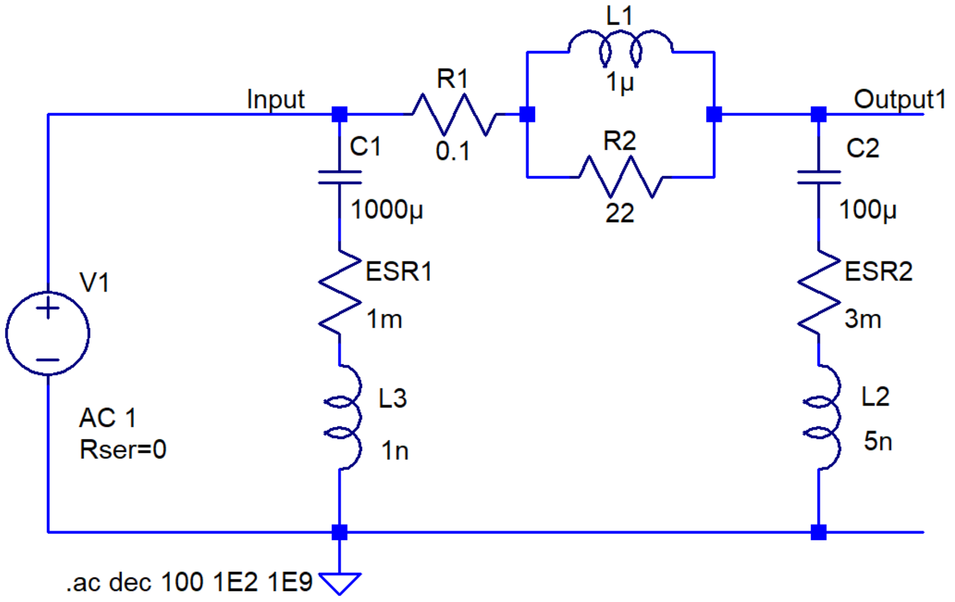
For filters from a high-current to a low-current rail: *Output impedance with shorted input and input impedance with open output*



Filter Illustration

The good



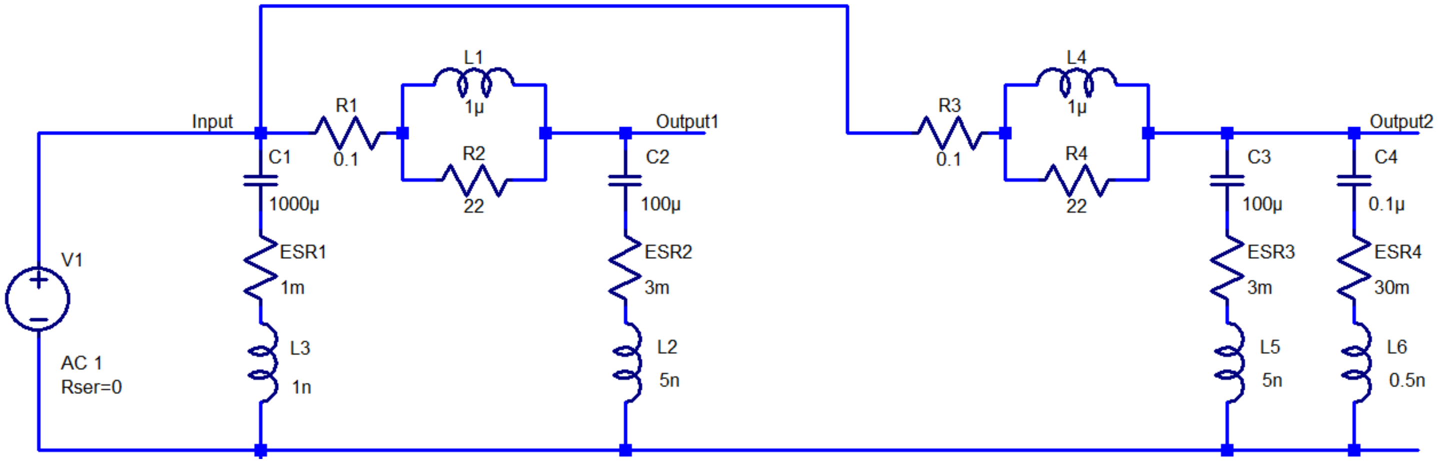


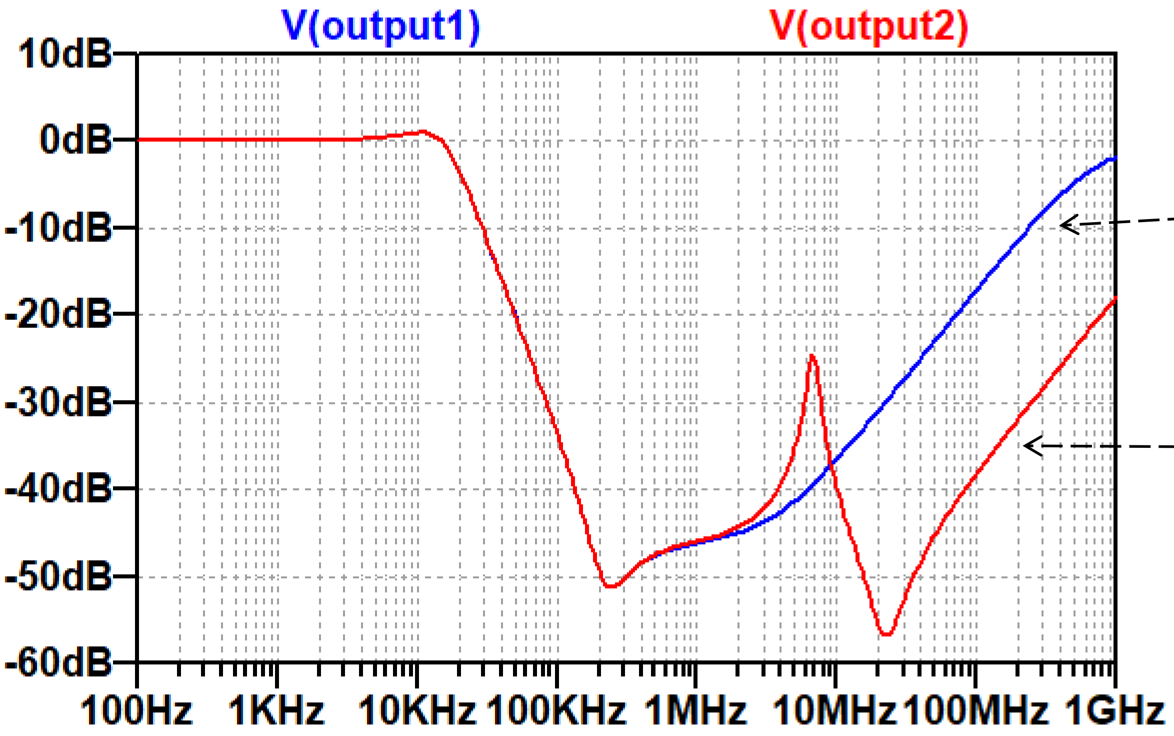
C_{out}=C2

100 µF 0.003 ohm 5 nH

Filter Illustration

When more is less





Case 1 C_{out}

100 µF 0.003 ohm 5 nH

Case 2 C_{out}

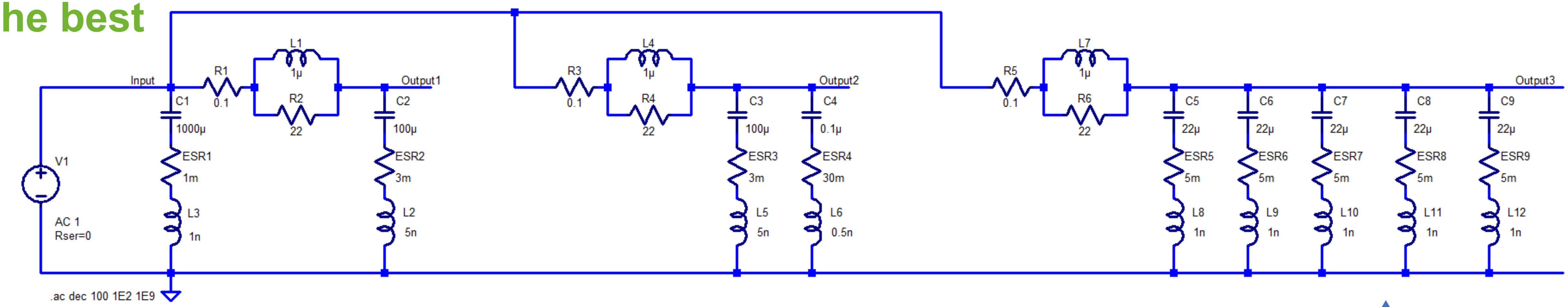
100 µF 0.003 ohm 5 nH

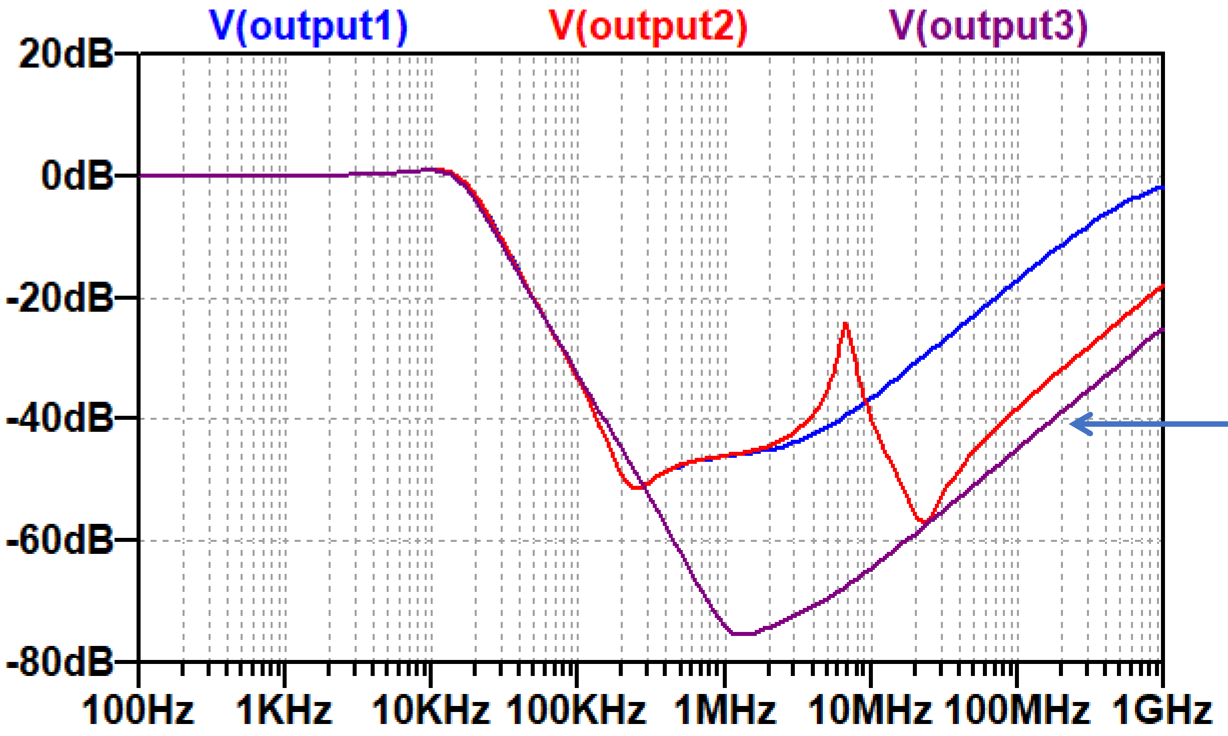
0.1 µF 0.03 ohm 0.5 nH

Better at high frequencies, but we got a peak

Filter Illustration

The best





Identical capacitors in parallel

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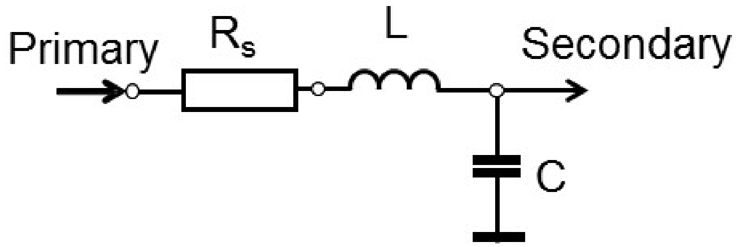
The Filter Design Process

Collect input requirements

- Offending frequency components (frequency, magnitude) to filter
- Necessary attenuation
- Set design parameters:
- Filter cutoff frequency f_c and Q

Design the inductance and bulk capacitance based on:



$$f_c = \frac{1}{2\pi\sqrt{LC}}, \quad Q = \frac{\sqrt{\frac{L}{C}}}{R_S}$$

Or use a circuit simulator to quickly iterate component values…

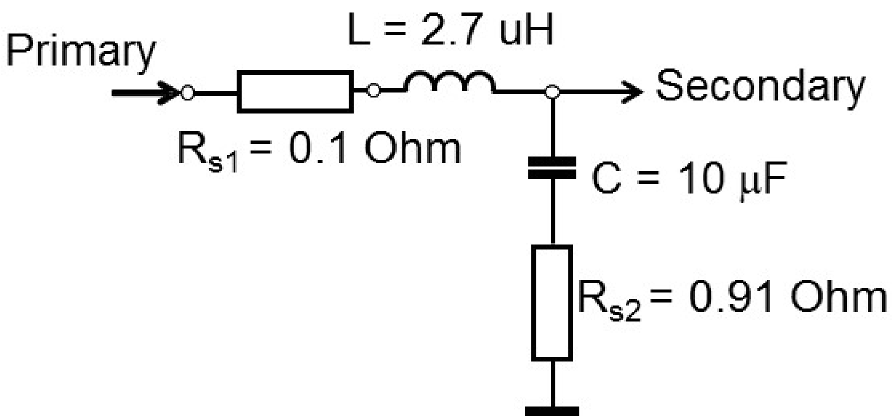
Low-Current Filter Example (1)

Design requirements for low-current filter

- Cutoff frequency f_c = 100 kHz (DC-DC converter running at 1MHz)
- Q = 0.5

Assume R_s = 1 Ohm

$$f_c = \frac{1}{2\pi\sqrt{LC}}, \quad Q = \frac{\sqrt{\frac{L}{C}}}{R_S}$$



Calculated values:

- L = 2.7 µH
- C = 10 uF

Select:

- L = 2.7 µH 0.1 Ohm
- C = 10 µF + 0.91 Ohm

Low-Current Filter Example (2)

Transfer functions of PDN filter with ferrite-bead model

C1	C2	C3	Rdc	Lf1	C4	C5	C6
1.00E+03	1.00E-03	1.00E-05	1.00E-01	2.70E-06	1.00E-05	1.00E-07	1.00E-09
R1	R2	R3	Cb	Rf1	R4	R5	R6
1.00E-03	5.00E-02	1.00E-02	5.00E-13	1.00E+06	9.10E-01	1.00E+06	1.00E+06
L1	L2	L3	Rb	Lf2	L4	L5	L6
5.00E-07	5.00E-09	1.00E-09	1.00E+01	1.00E-12	1.00E-09	1.00E-09	1.00E-10
N1	N2	N3		Rf2	N4	N5	N6
1	1	1		1.00E-03	1	1	1

Fmin
1.00E+02
Fmax
1.00E+08

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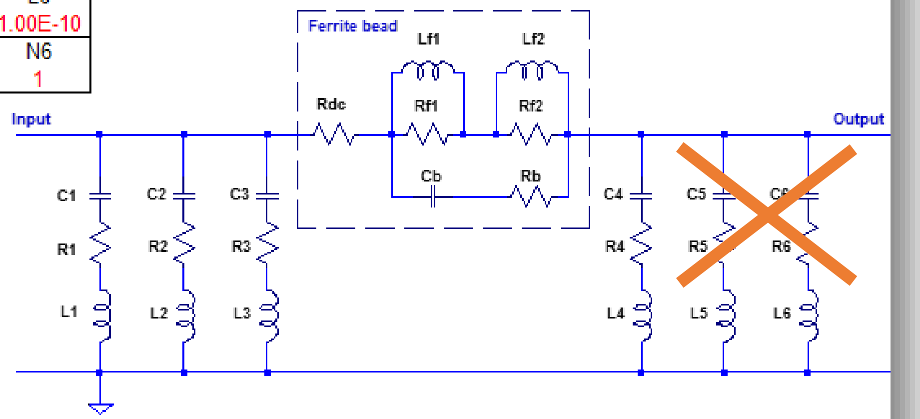
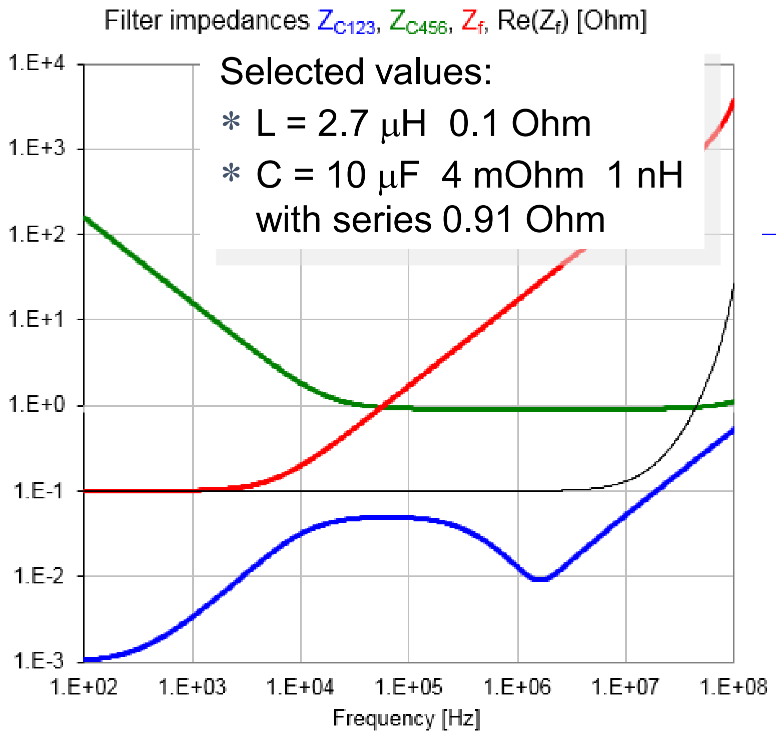
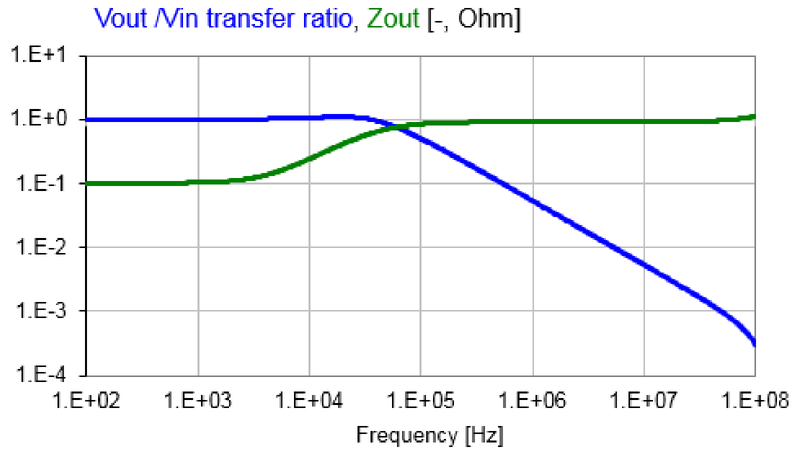


Selected values:

* L = 2.7 μH 0.1 Ohm
* C = 10 μF 4 mOhm 1 nH with series 0.91 Ohm

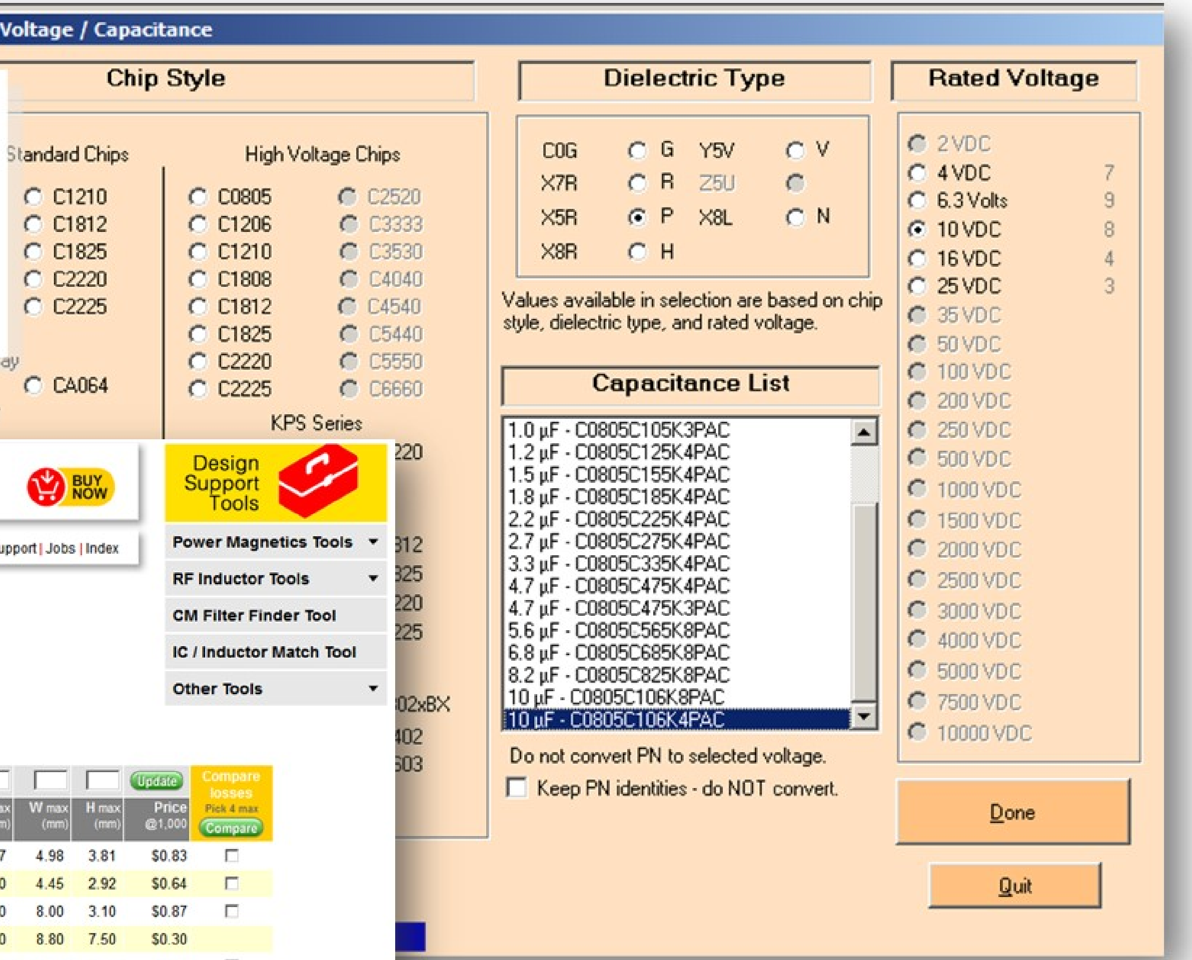


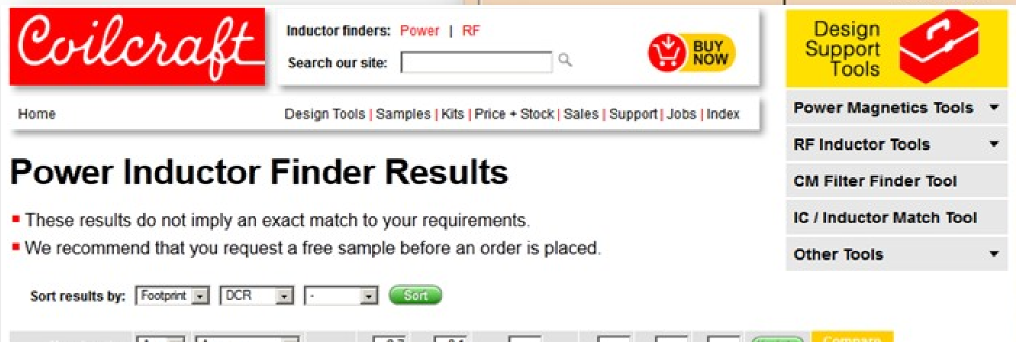


Low-Current Filter Example (3)

Selected components:

- Coilcraft 181PS-272 L = 2.7 µH 0.08 Ohm
- Kemet C0805C106K4PAC C = 10 µF 4 mOhm 1 nH





Power Inductor Finder Results

- These results do not imply an exact match to your requirements.
- We recommend that you request a free sample before an order is placed.

Sort results by: Footprint DCR - Sort

Part number	Mount	Core material	Other*	L (µH)	DCR (Ω)	I sat (A)	I rms (A)	L max (mm)	W max (mm)	H max (mm)	Price @1,000	Compare
Your inputs:	Any	Any core		2.7	0.1							
1812PS-272	SM	Ferrite	S	2.7	0.0800	1.4	2.3	5.87	4.98	3.81	$0.83	
DO1608C-272	SM	Ferrite		2.7	0.0800	2.1	2.45	6.60	4.45	2.92	$0.64	
XAL7030-272	SM	Composite	S	2.7	0.0173	12.8	11.4	8.00	8.00	3.10	$0.87	
RFB0807-2R7	Leaded	Ferrite		2.7	0.0140	5.5	6.54	8.80	8.80	7.50	$0.30	
MSS1038T-252	SM	Ferrite	S	2.5	0.0100	9.26	6.65	10.50	10.20	4.00	$0.55	

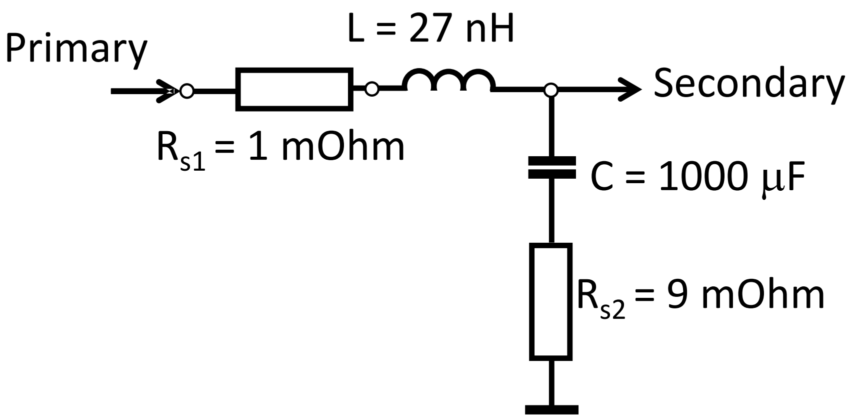
High-Current Filter Example (1)

Design requirements for high-current filter

- Cutoff frequency f_c = 30 kHz (DC-DC converter running at 300 kHz)
- Q = 0.5

Assume R_s = 10 mOhm

$$f_c = \frac{1}{2\pi\sqrt{LC}}, \quad Q = \frac{\sqrt{\frac{L}{C}}}{R_S}$$



Calculated values:

- L = 27 nH
- C = 1000 μF

Select:

- L = 27 nH 1 mOhm
- C = 1000 μF 9 mOhm

High-Current Filter Example (2)

Transfer functions of PDN filter with ferrite-bead model

C1	C2	C3	Rdc	Lf1	C4	C5	C6
1.00E+03	1.00E-03	1.00E-05	1.00E-03	2.70E-08	1.00E-03	1.00E-07	1.00E-09
R1	R2	R3	Cb	Rf1	R4	R5	R6
1.00E-03	5.00E-02	1.00E-02	5.00E-13	1.00E+06	9.00E-03	1.00E+06	1.00E+06
L1	L2	L3	Rb	Lf2	L4	L5	L6
5.00E-07	5.00E-09	1.00E-09	1.00E+01	1.00E-12	5.00E-09	1.00E-09	1.00E-10
N1	N2	N3		Rf2	N4	N5	N6
1	1	1		1.00E-03	1	1	1

Fmin
1.00E+02
Fmax
1.00E+09

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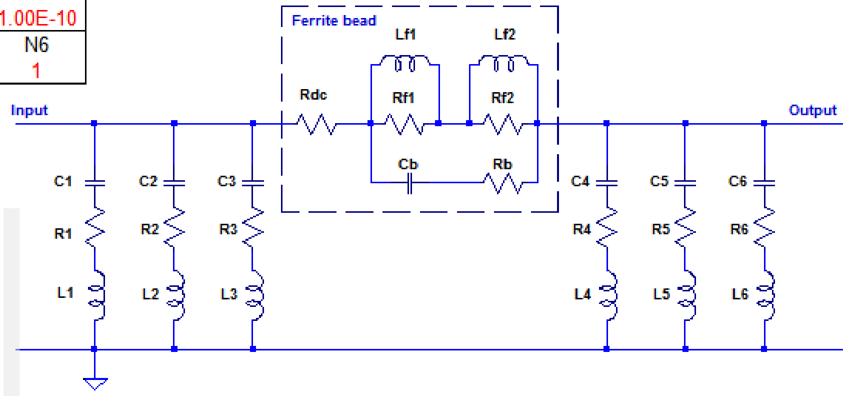
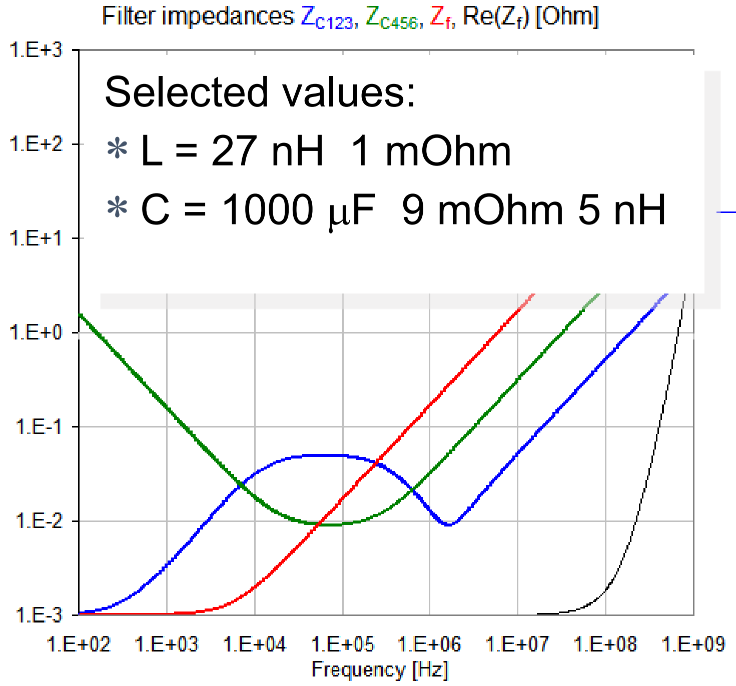
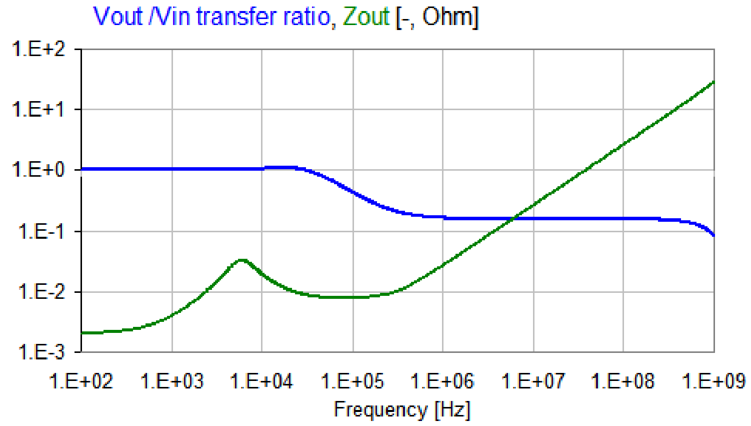




Selected values:

* L = 27 nH 1 mOhm
* C = 1000 μF 9 mOhm 5 nH



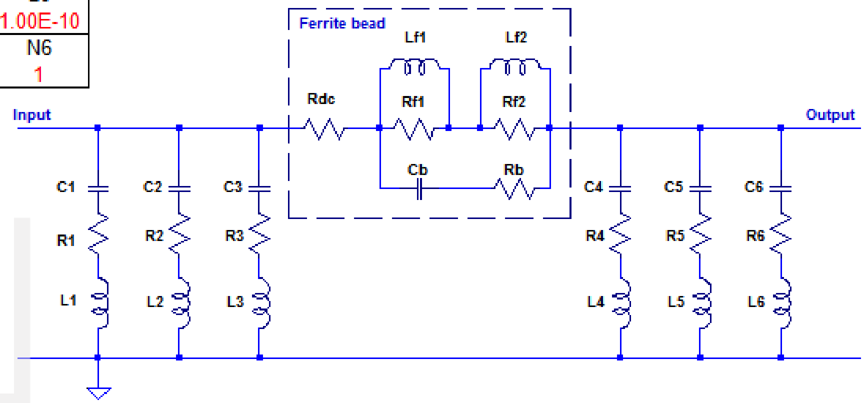
High-Current Filter Example (3)

Transfer functions of PDN filter with ferrite-bead model

C1	C2	C3	Rdc	Lf1	C4	C5	C6
1.00E+03	1.00E-03	1.00E-05	1.00E-03	2.70E-08	4.70E-04	1.00E-07	1.00E-09
R1	R2	R3	Cb	Rf1	R4	R5	R6
1.00E-03	5.00E-02	1.00E-02	5.00E-13	1.00E+06	1.80E-02	1.00E+06	1.00E+06
L1	L2	L3	Rb	Lf2	L4	L5	L6
5.00E-07	5.00E-09	1.00E-09	1.00E+01	1.00E-12	4.00E-09	1.00E-09	1.00E-10
N1	N2	N3		Rf2	N4	N5	N6
1	1	1		1.00E-03	2	1	1

Fmin
1.00E+02
Fmax
1.00E+09

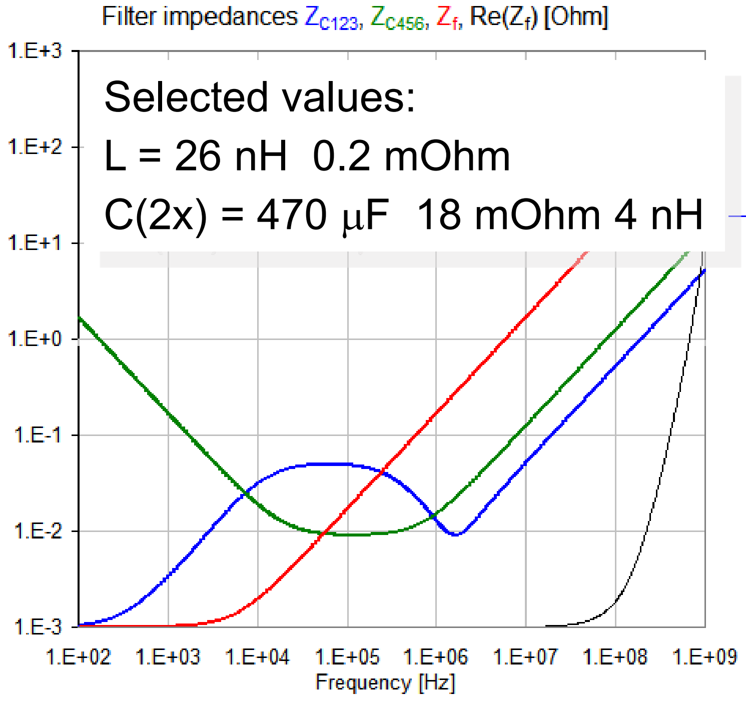
istvan.novak@ieee.org
www.electrical-integrity.com

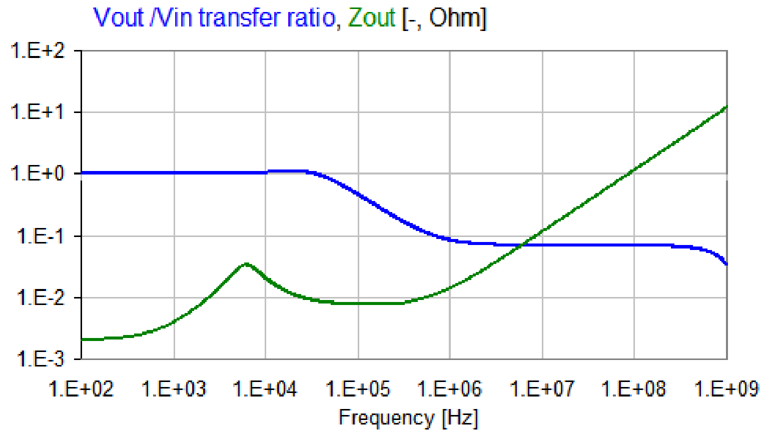


Selected values:

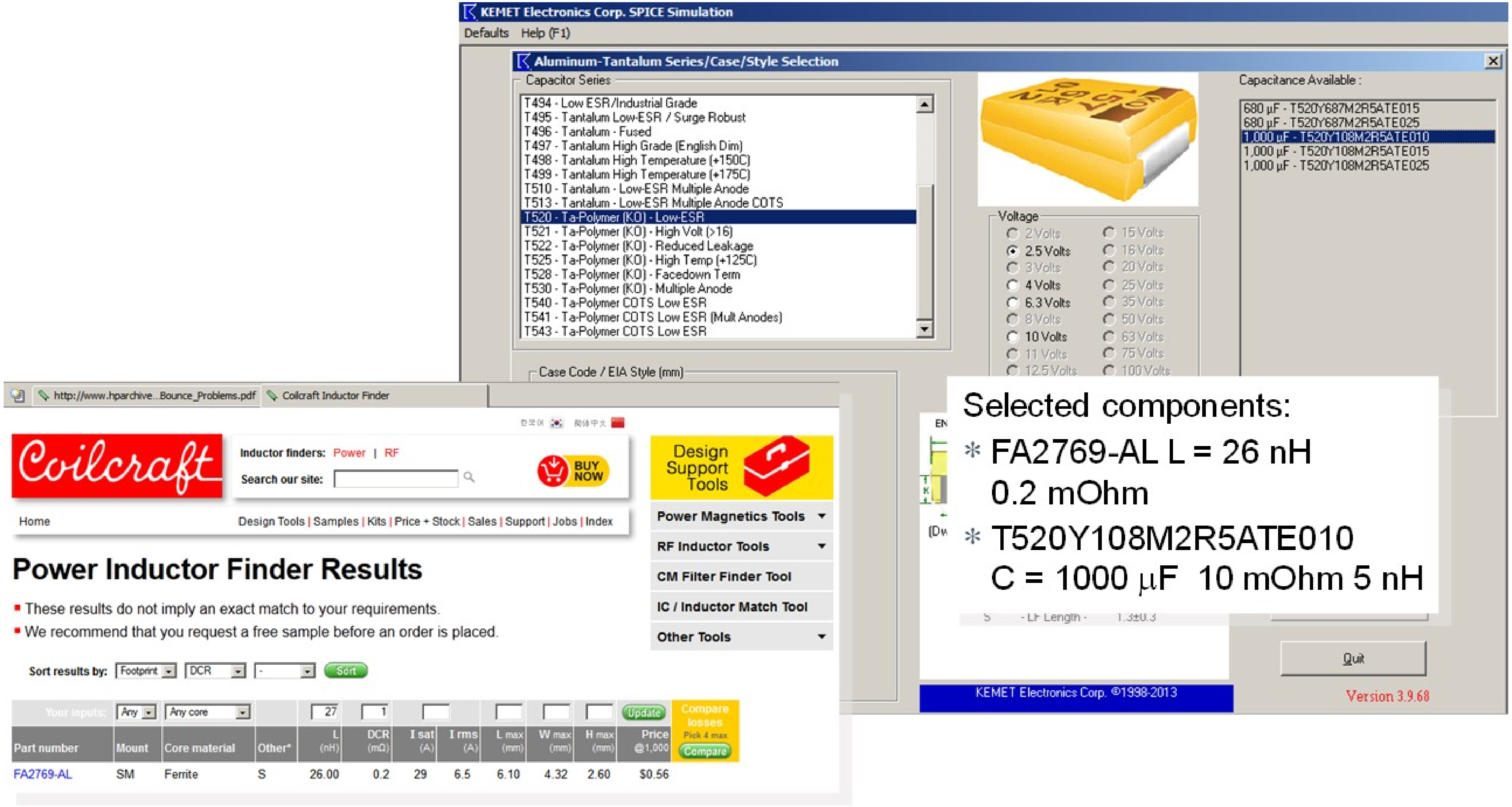
L = 26 nH 0.2 mOhm

C(2x) = 470 µF 18 mOhm 4 nH





High-Current Filter Example (4)



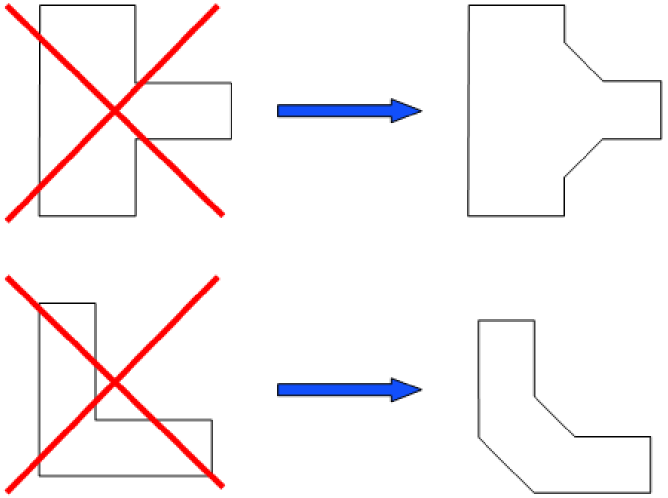
Selected components:

- FA2769-AL L = 26 nH
  0.2 mOhm
- T520Y108M2R5ATE010
  C = 1000 µF 10 mOhm 5 nH

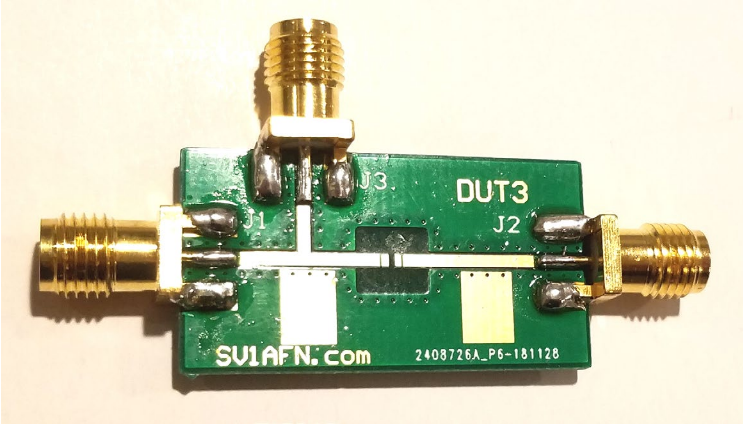
OUTLINE

* Introduction, scope
* Requirements
* Filter design procedure
* What can go wrong
  * Wrong layout
  * Bias dependence
* Simulations and correlations
* Demos

What Can Go Wrong
Layout issues

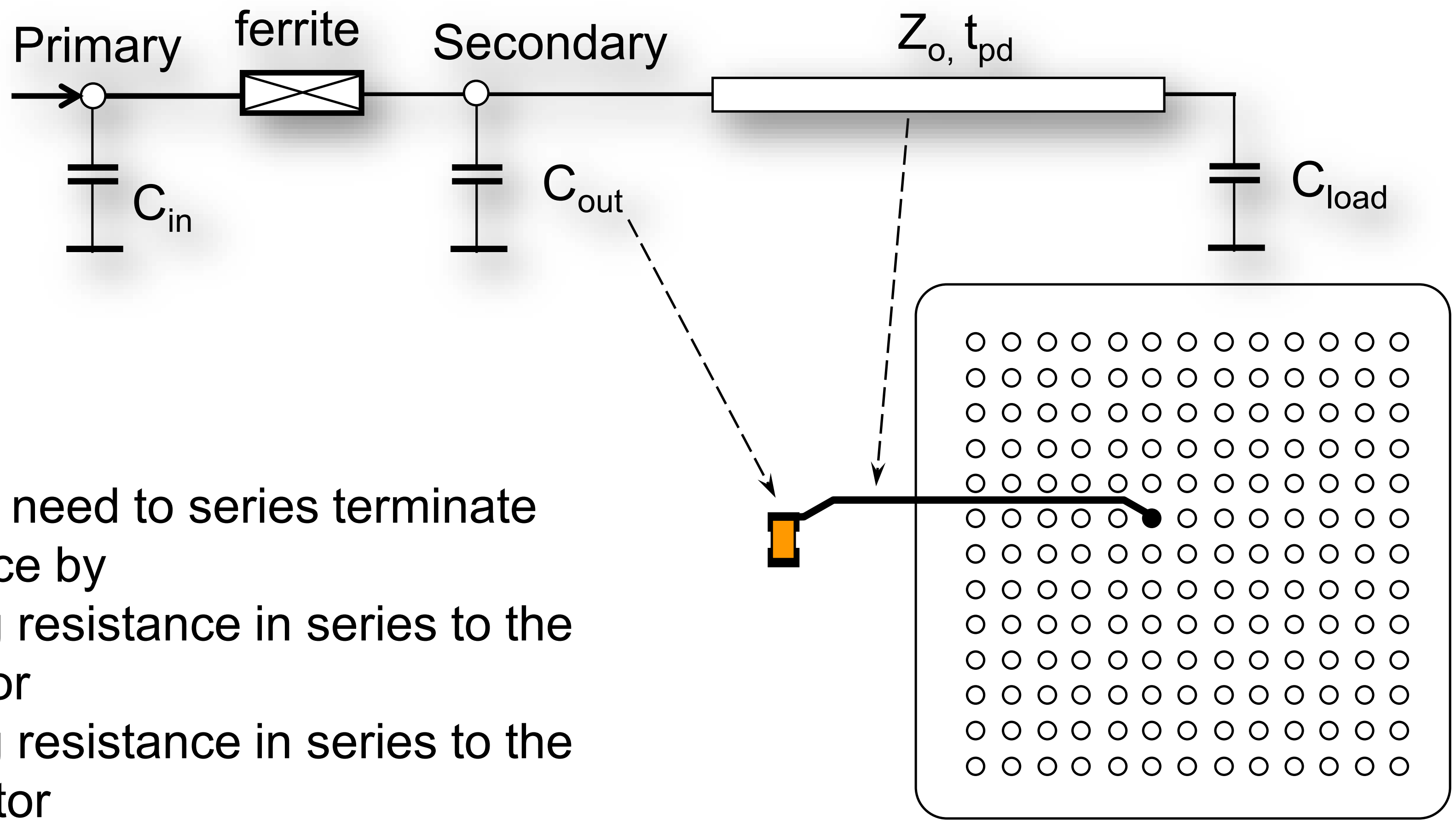


* In high-current filters (voltage drop matters)
  - DC issues around contact resistance
  - resistance increase in corners
  - uneven distribution of currents in via arrays
* In wide-band and high-attenuation filters
  - sneaky path around components
  - Sneaky path on the board
* Too much phase shift if the filter is inside a converter feedback loop (usually in unintentional filters)
* Stub resonance



Filter Geometry
A possible problem

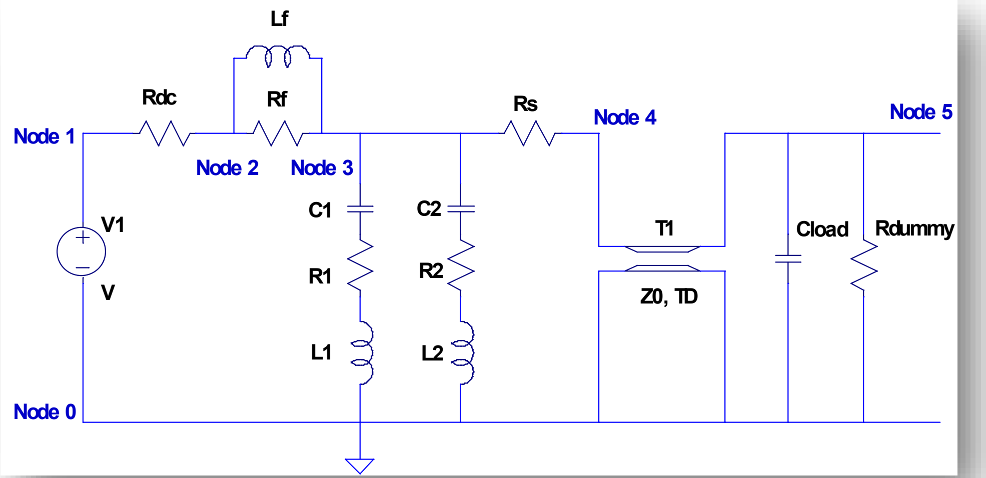
We may not have room for filter capacitors near IC pins. But an extreme terminated trace resonates and amplifies noise.

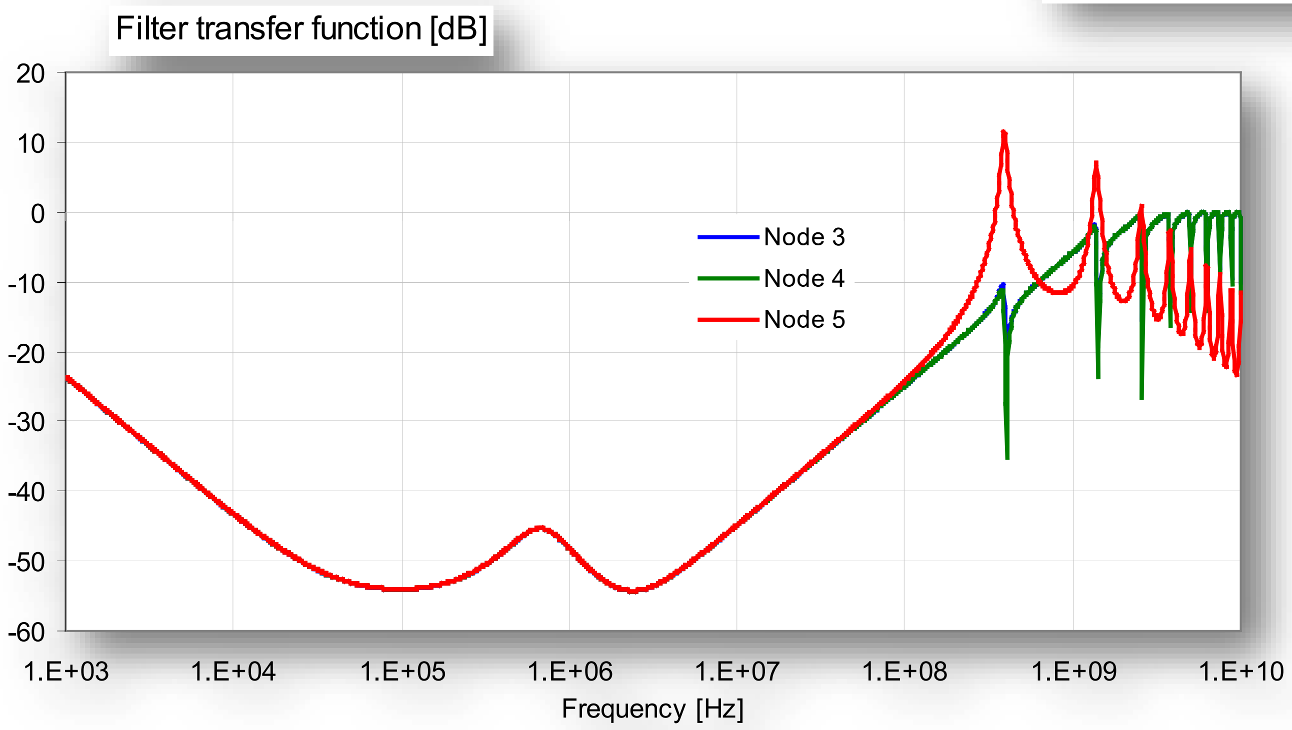


Solution: need to series terminate the trace by

- Adding resistance in series to the trace, or
- Adding resistance in series to the capacitor

Simulated
Before Fix

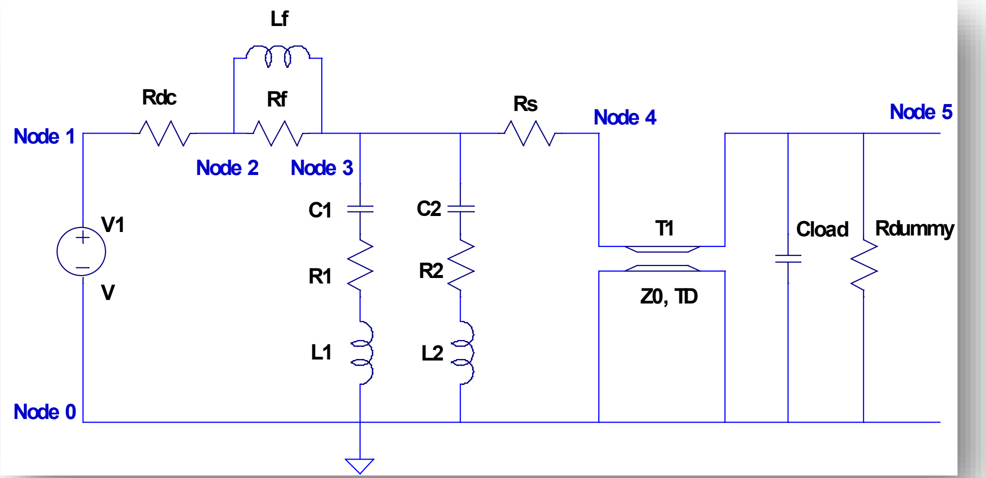


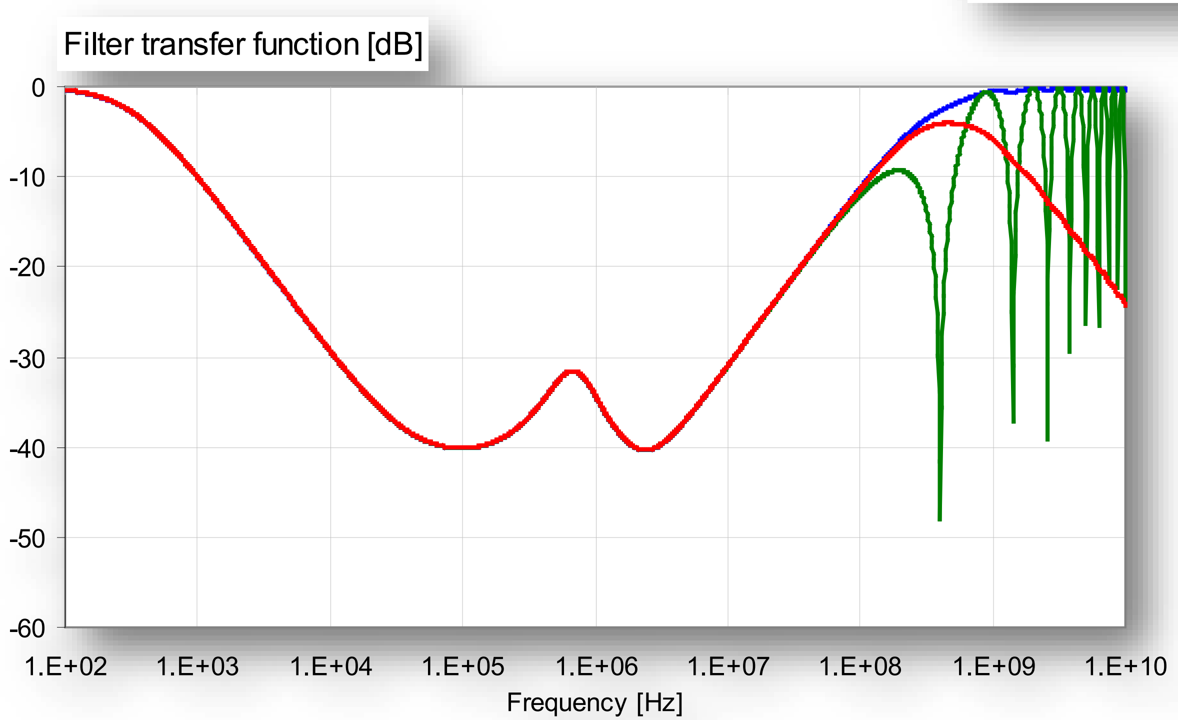


Voltage transfer function of analog PDN filter

Rdc	C1	C2	Fmin
5	4.70E-04	1.00E-05	1.00E+03
Lf	R1	R2	Fmax
1.00E-06	1.00E-02	1.00E-02	1.00E+10
Rf	L1	L2	Fsteps
1.00E-03	5.00E-09	5.00E-10	200
Rs	Zo	tpd	Cl
1.00E+00	2.50E+01	4.00E-10	1.00E-11

Simulated
After Fix





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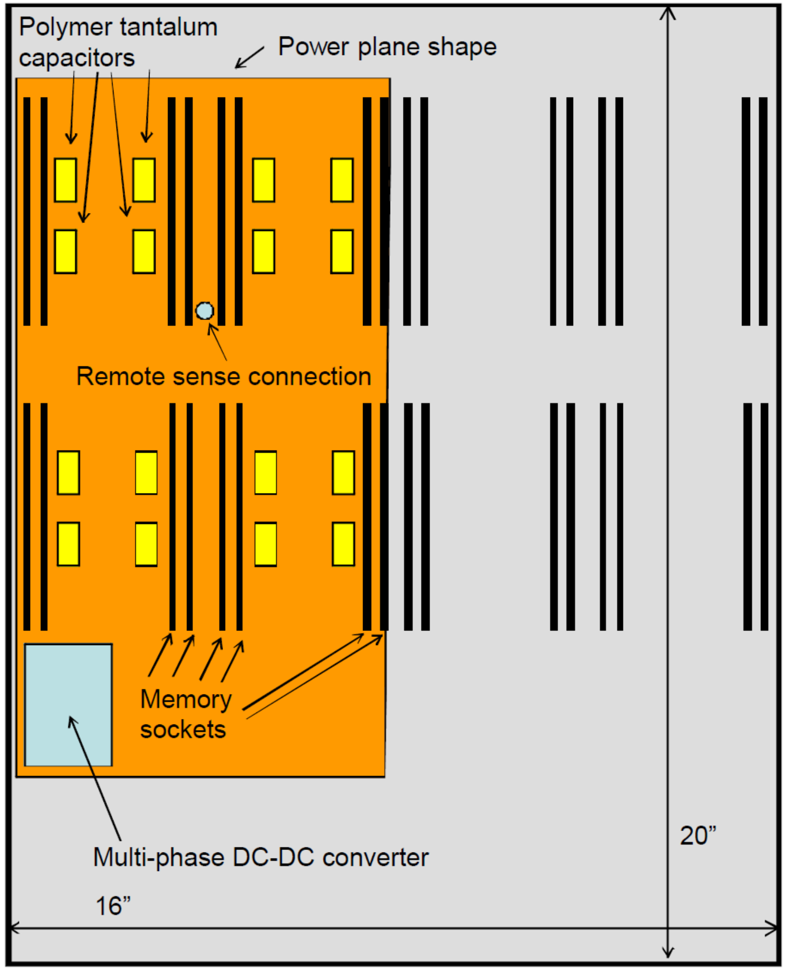
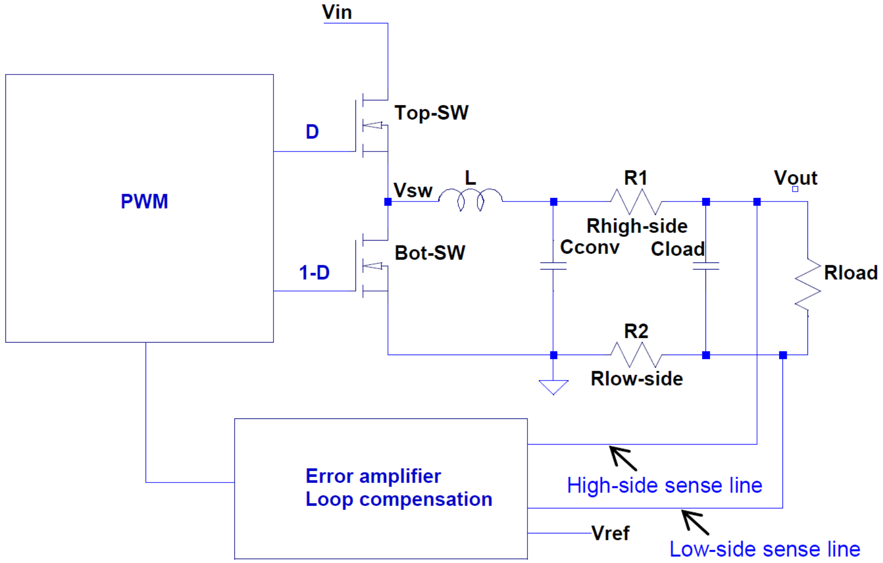
1.00E-03	5.00E-09	5.00E-10	200
Rs	Zo	tpd	Cl
2.50E+01	2.50E+01	4.00E-10	1.00E-11

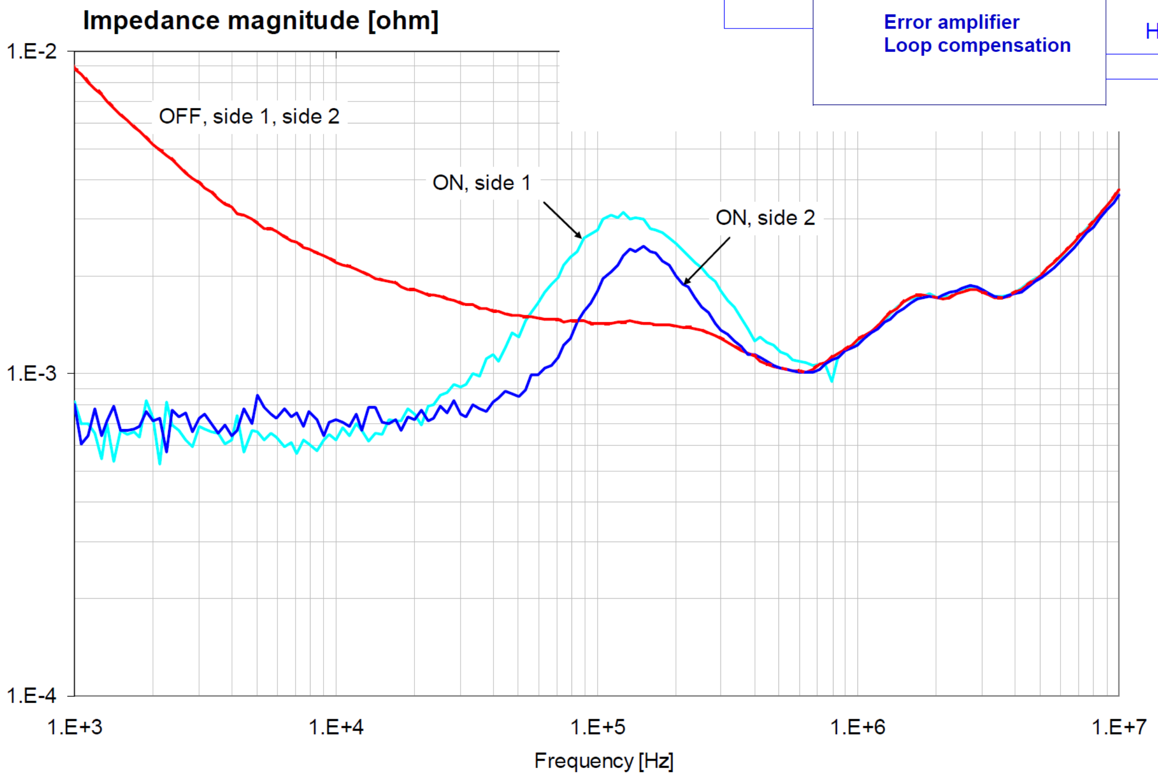
Be Aware

* Sometime parasitic elements create non-negligible filtering
* All filter components may be impacted by bias stress
  - Capacitance loss due to voltage bias
  - Inductance loss due to current bias
* The filter has to pass DC current and therefore very low frequency noise can not be eliminated
  - Sub-harmonic converter ripple
  - Low frequency random noise
* Series resistive loss maintains second-order filtering; resistance in the parallel path approaches first-order filtering
* Check the DC-DC converter operating frequency before you switch to a different converter!

Parasitic Filtering





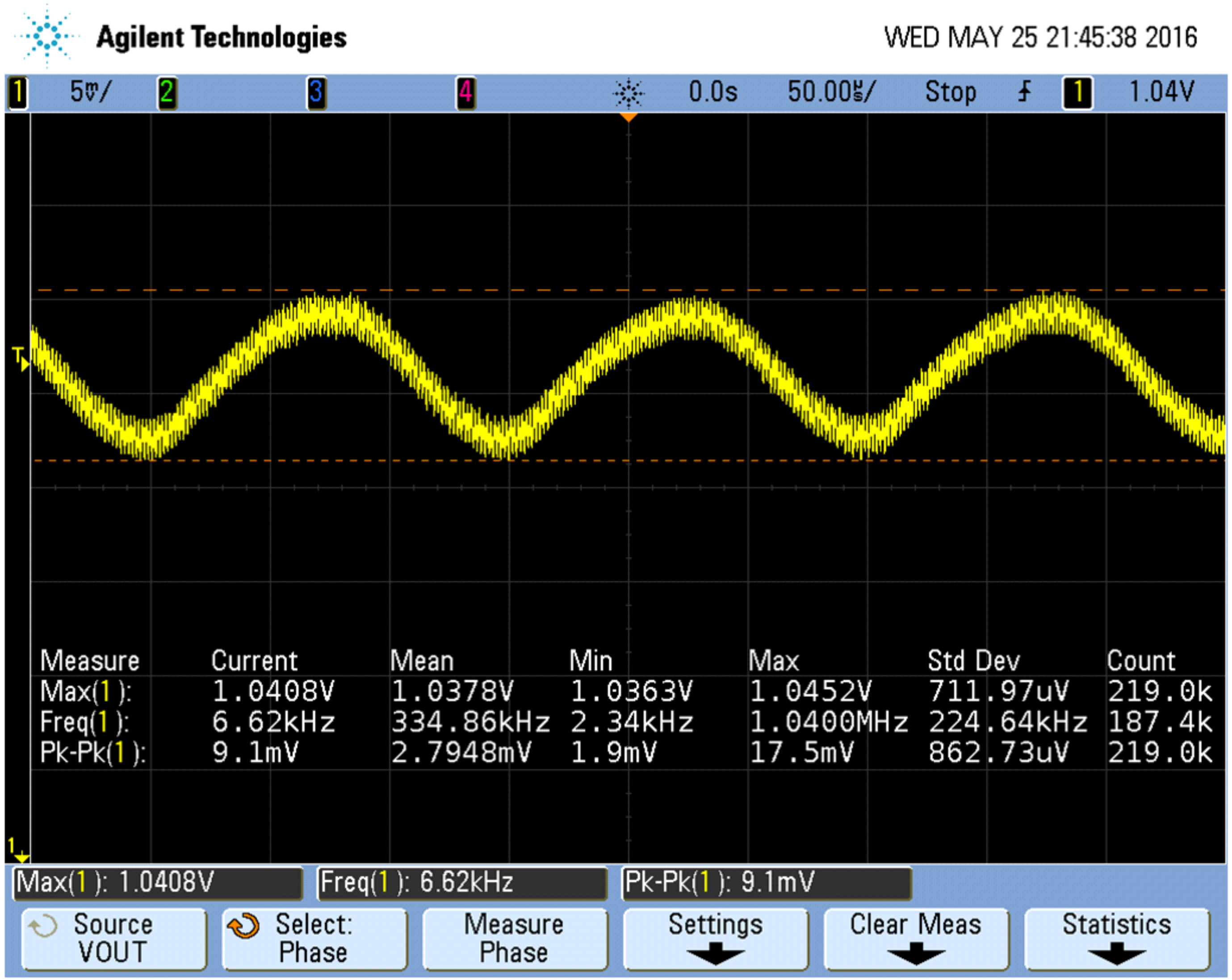


"Impact of Regulator Sense-point Location on PDN Response," Designcon 2015

Be Aware

Measured illustration of a DC-DC converter creating out-of-band low-frequency oscillation

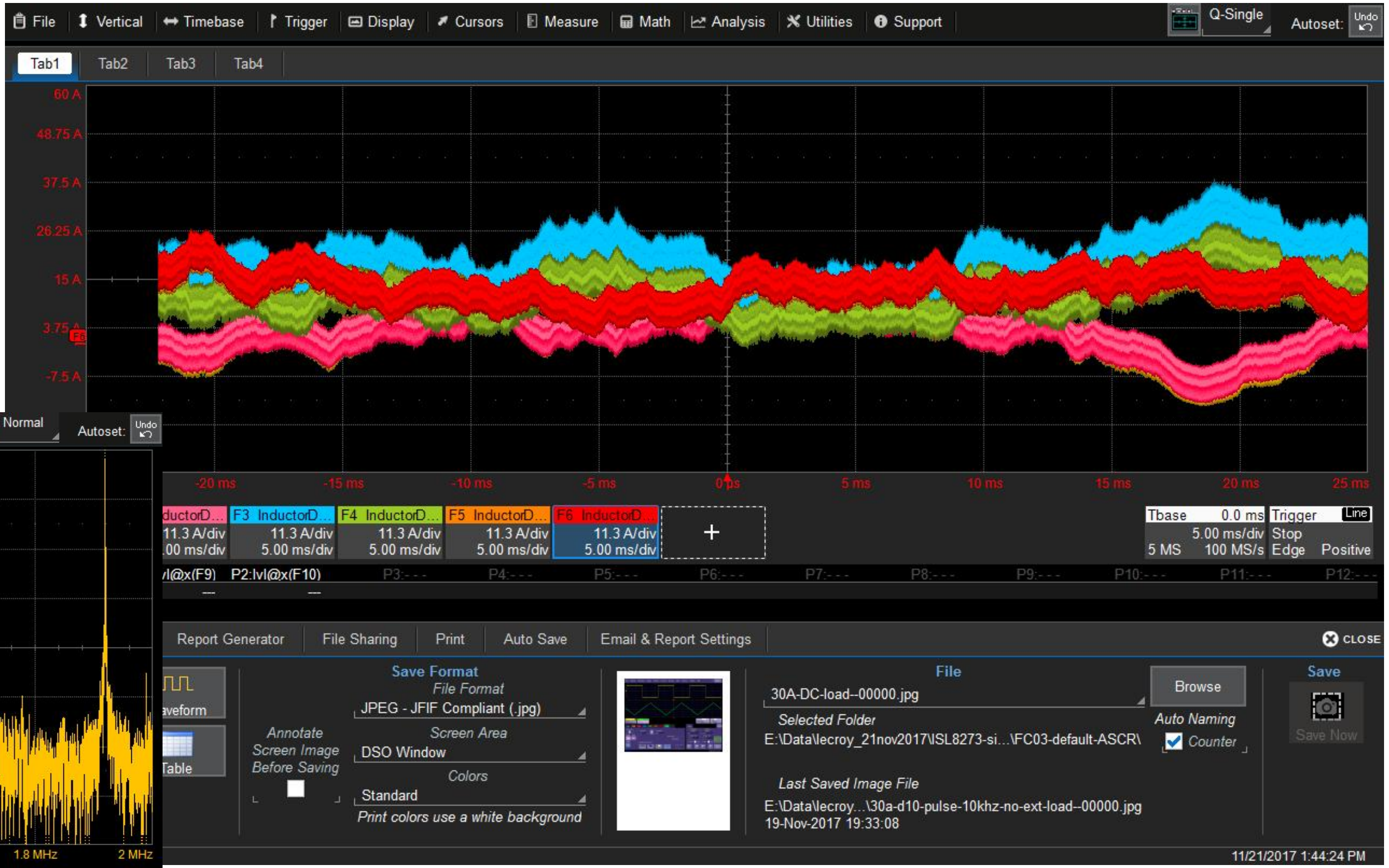
* 6 kHz periodic disturbance in a narrow operating point range
* 500 kHz switching frequency
* Single-phase 12V to 0.9V regulator

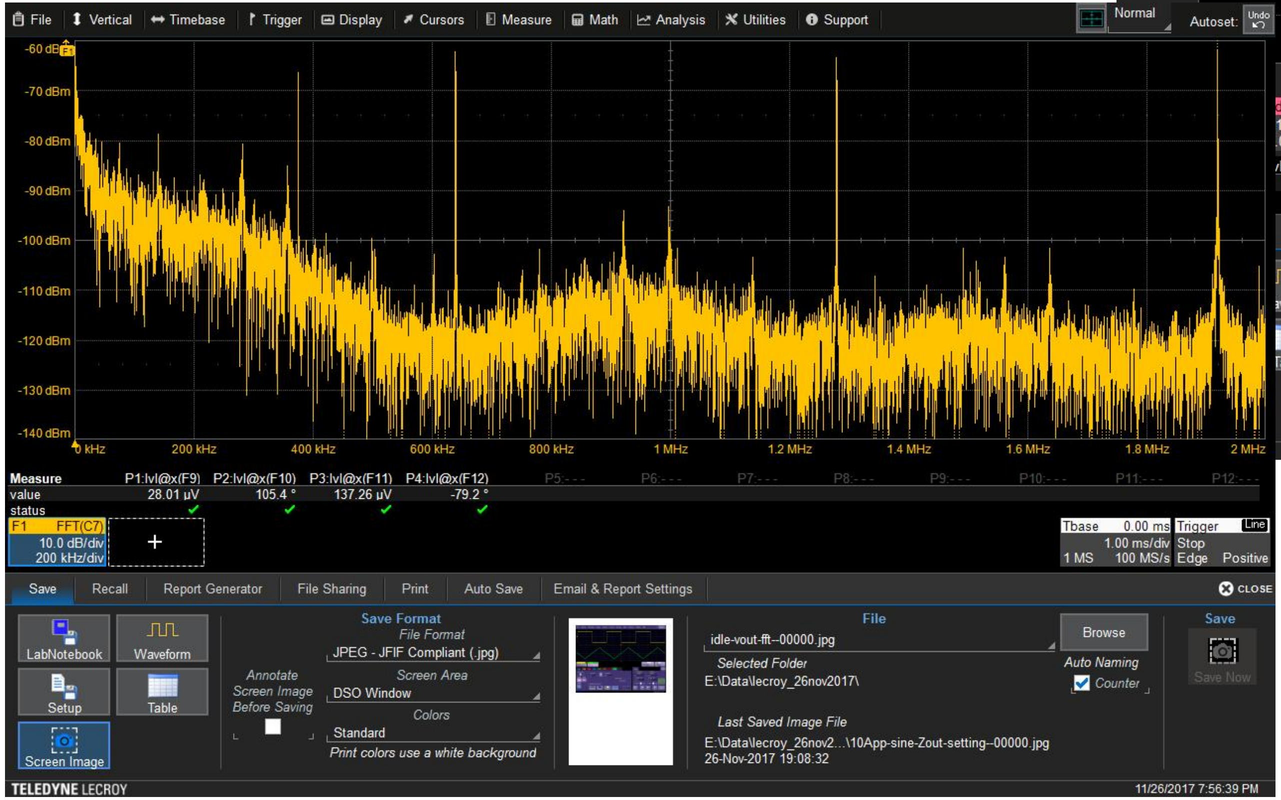


Source: “Overview and Comparison of Power Converter Stability Metrics,” DesignCon 2017

Be Aware

- Random wander of current sharing
- 600 kHz switching frequency
- Six-phase 12V to 0.9V regulator

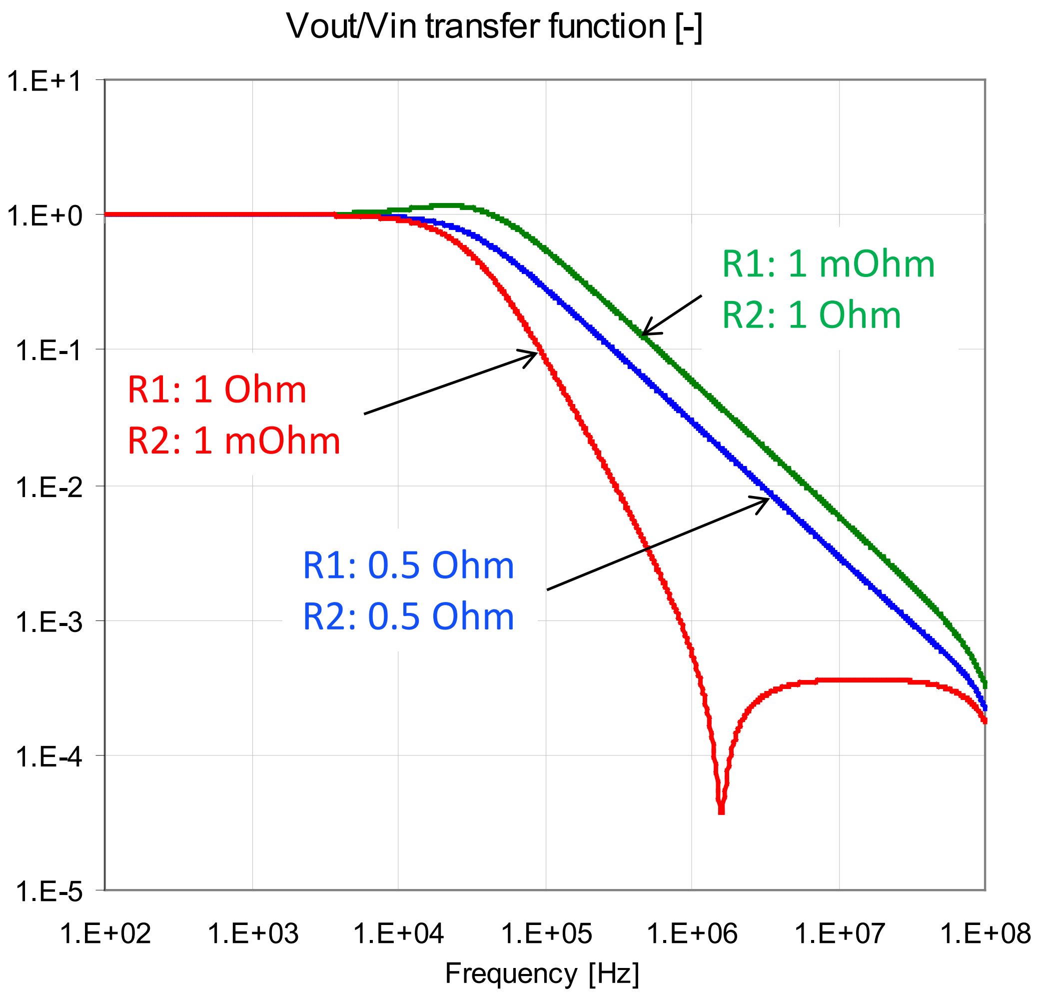


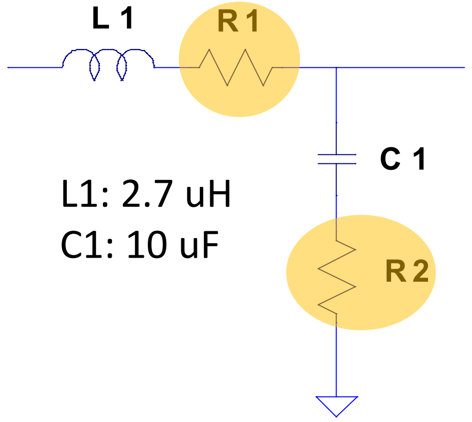


Current sharing among phases in the time domain
Spectrum of output voltage

Source: “Measuring current and current sharing of DC-DC converters,” DesignCon 2018

Be Aware: Distribution of Loss



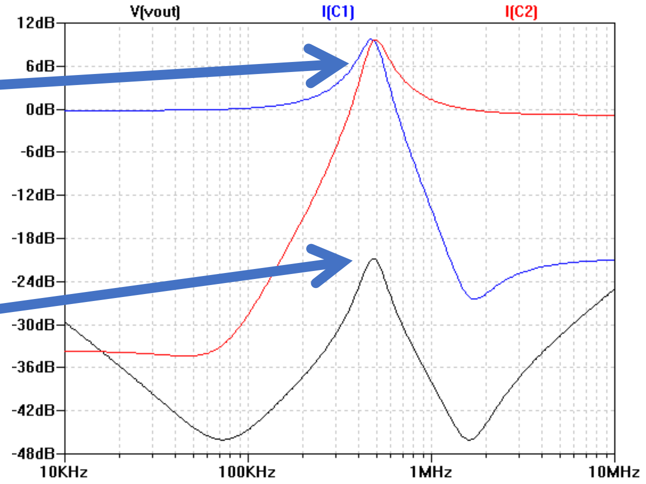


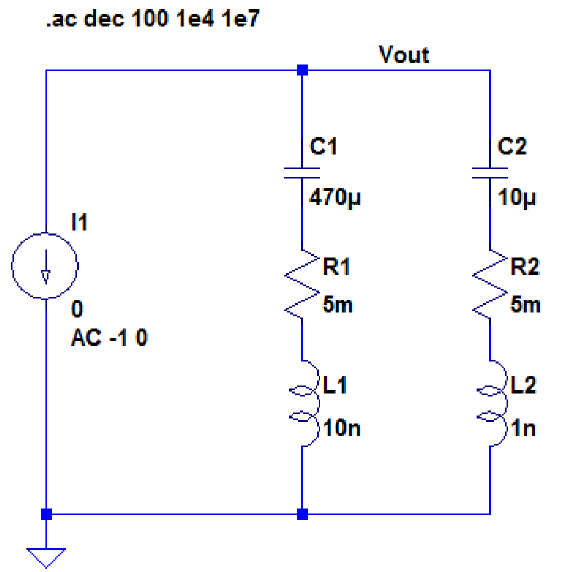
Series resistive loss maintains second-order filtering; resistance in the parallel path approaches first-order filtering

Be Aware: Q Amplification

Q times amplification of current

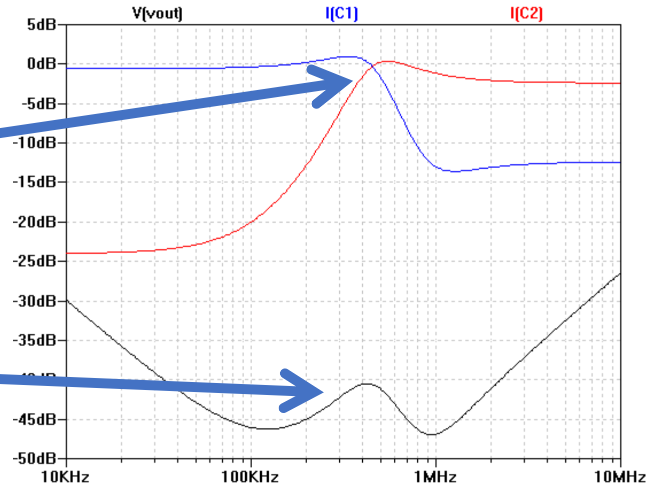
Peaky impedance: Q=3

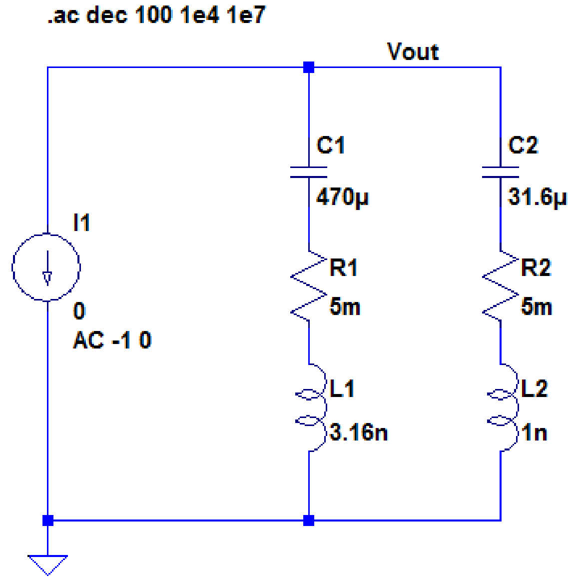




No amplification of current

Q=1

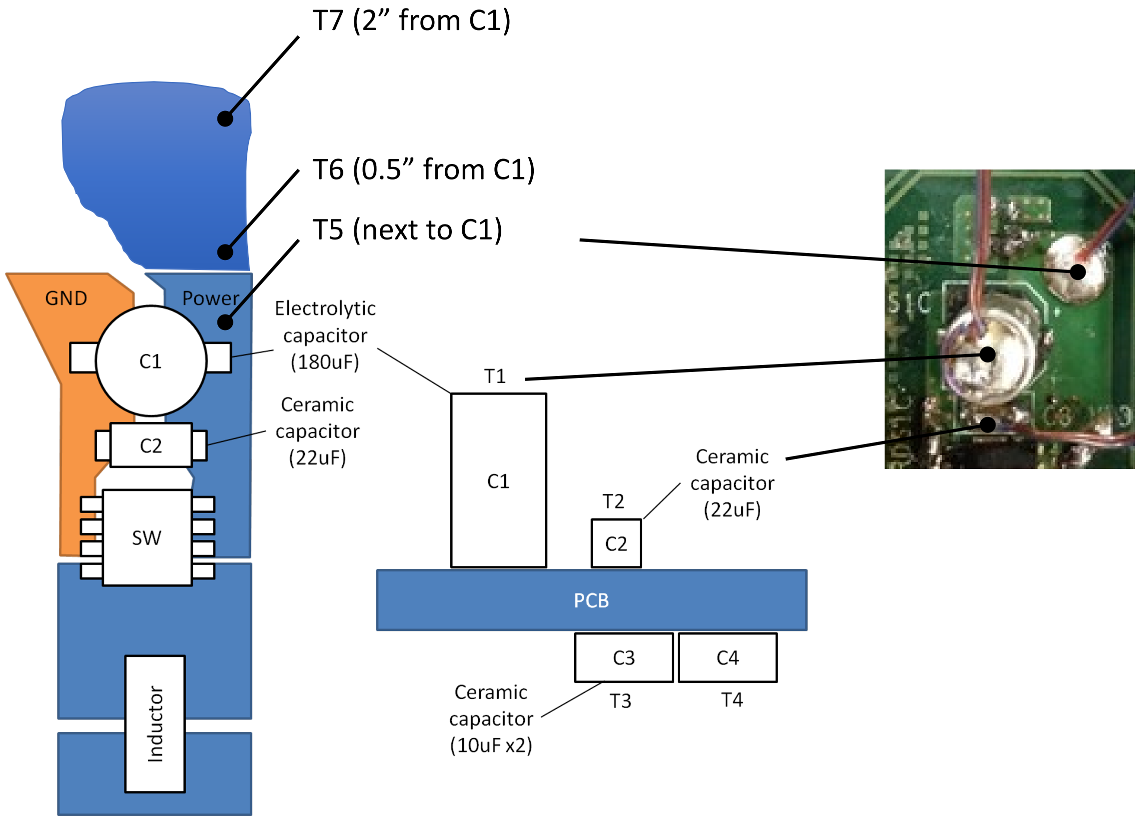


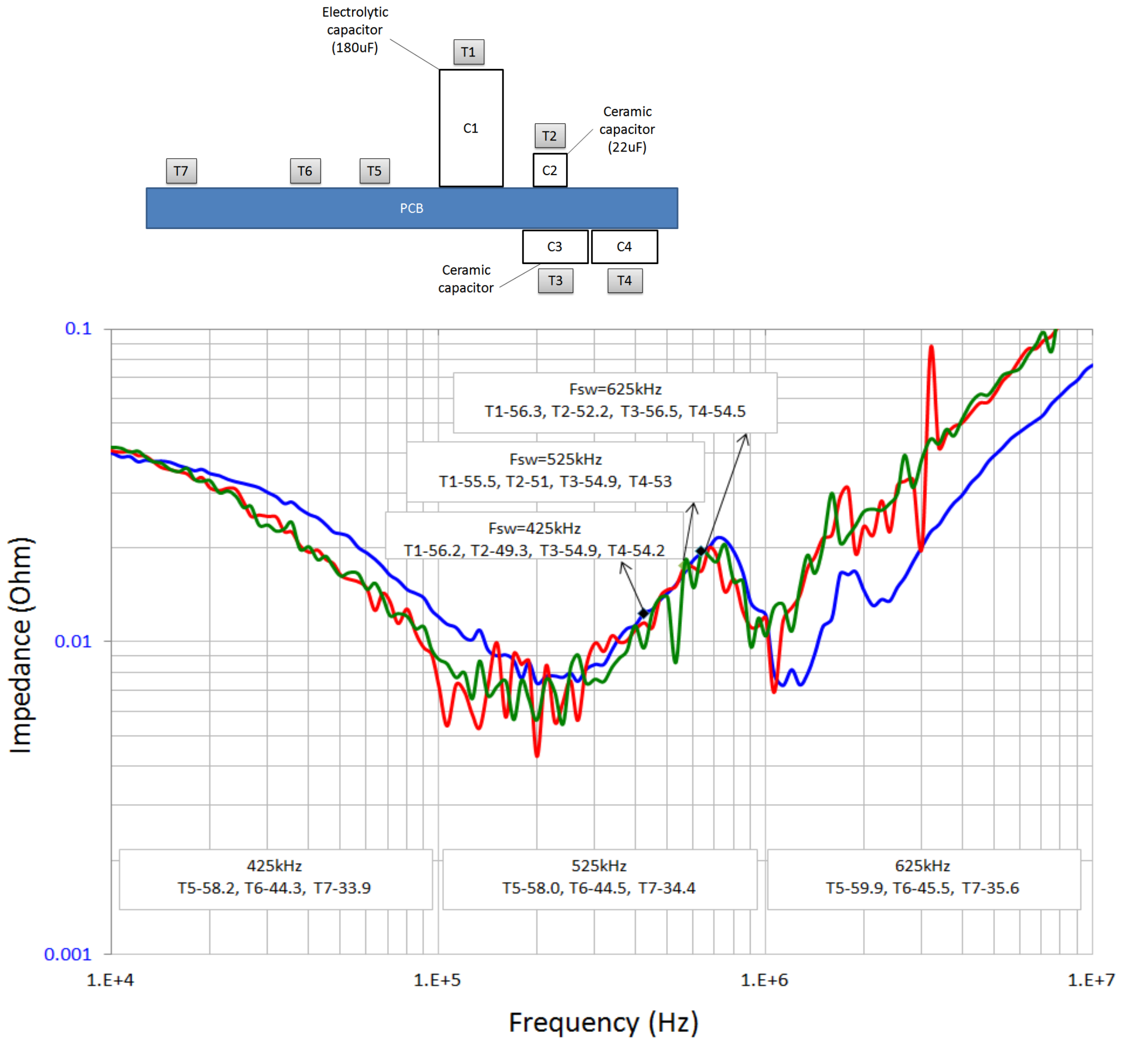


Q Amplification: Thermal Effect

Dissipation in capacitors:

$$I_{rms}^2 * ESR$$

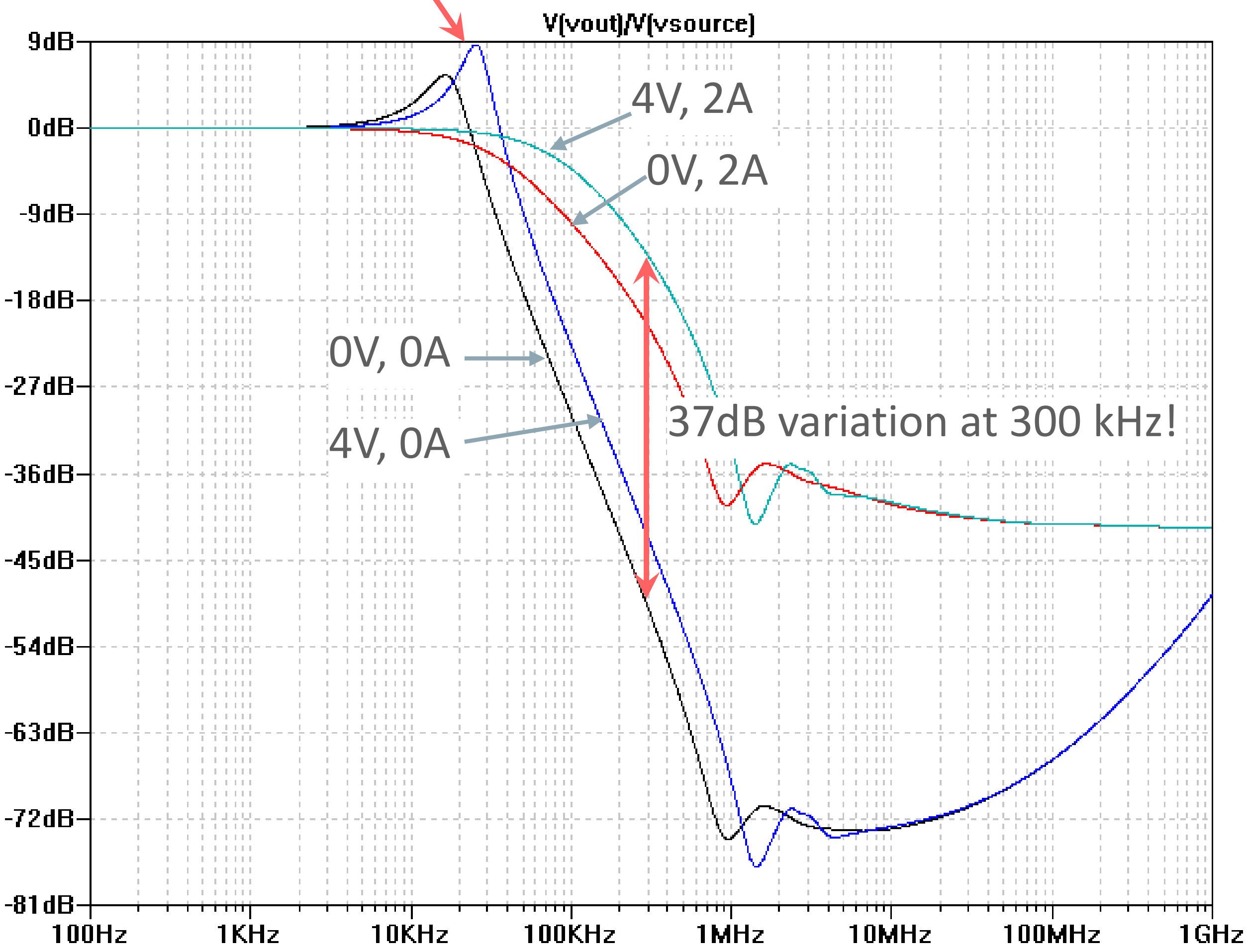


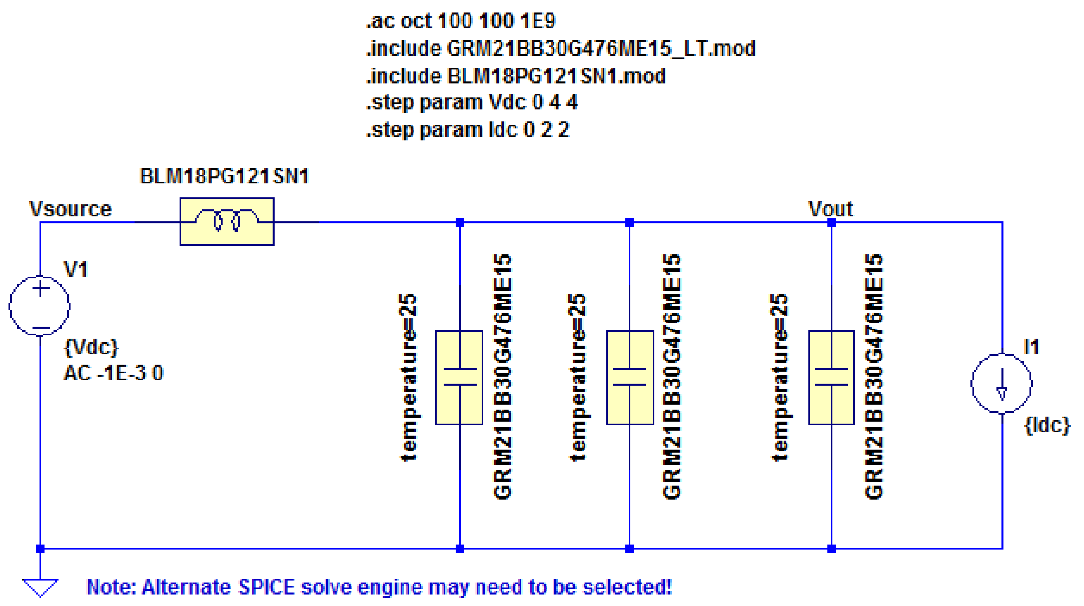


Source: "Electrical and Thermal Consequences of Non-Flat Impedance Profiles," DesignCon 2016

Be Aware: Bias Effect

9dB peaking at 25 kHz!





Loss of Capacitance in MLCCs

	Percentage range [%]	Relative multiplier
Initial tolerance	+-10	0.9 … 1.1
Temperature effect	+-15	0.85 … 1.15
DC bias effect	+0 -70	0.3 … 1
AC bias effect	+0 -30	0.7 … 1
Aging (over 3 years)	+0 -7.5	0.925 … 1

0.15 ***1.27***

* For worst case, have to multiply all multipliers
* High CV ceramic capacitors can lose up to 85% of capacitance
* Highest impact is DC and AC bias voltage

Source: “How Much Capacitance Do We Really Get?,” QuietPower columns, http://www.electrical-integrity.com/Quietpower_files/QuietPower-40.pdf

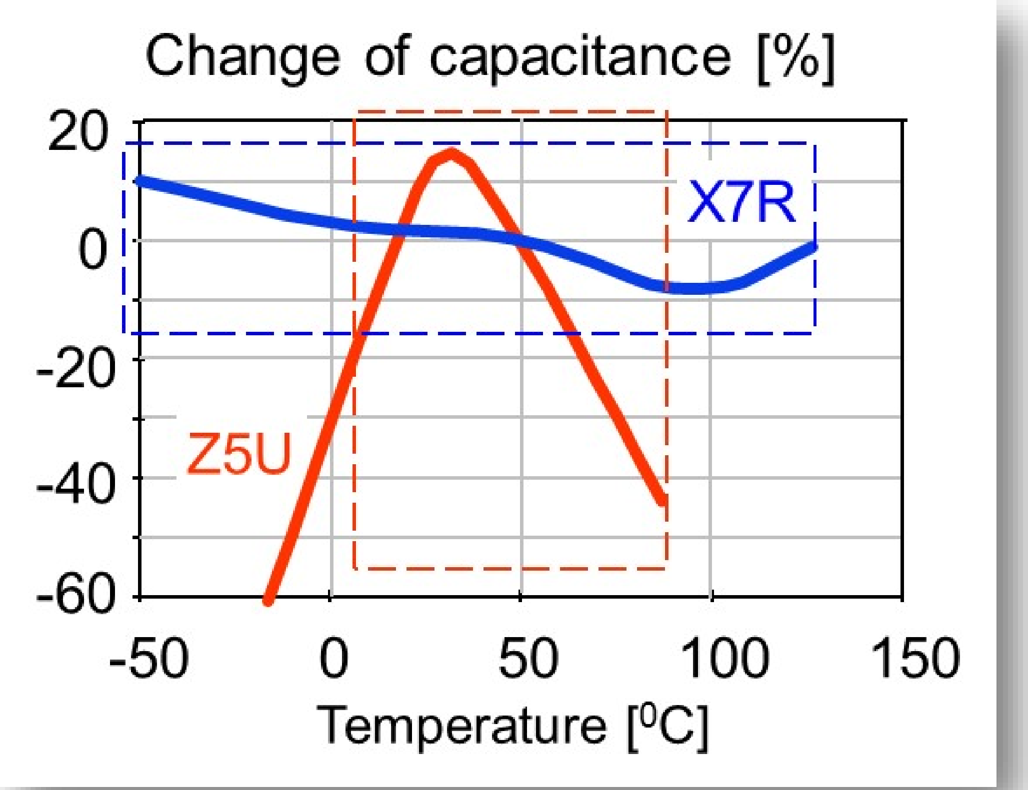
Loss of Capacitance in MLCCs, Temperature

EIA Class II and Class III ceramics

First character:
Z: + 10C
Y: - 30C
X: - 55C

Second character:
2: + 45C
4: + 65C
5: + 85C
6: + 105C
7: + 125C
8: + 150C
9: + 200C

Third character:
F: +- 7.5%
P: +- 10%
R: +- 15%
S: +- 22%
T: + 22 / - 33%
U: + 22 / - 56%
V: + 22 / - 82%

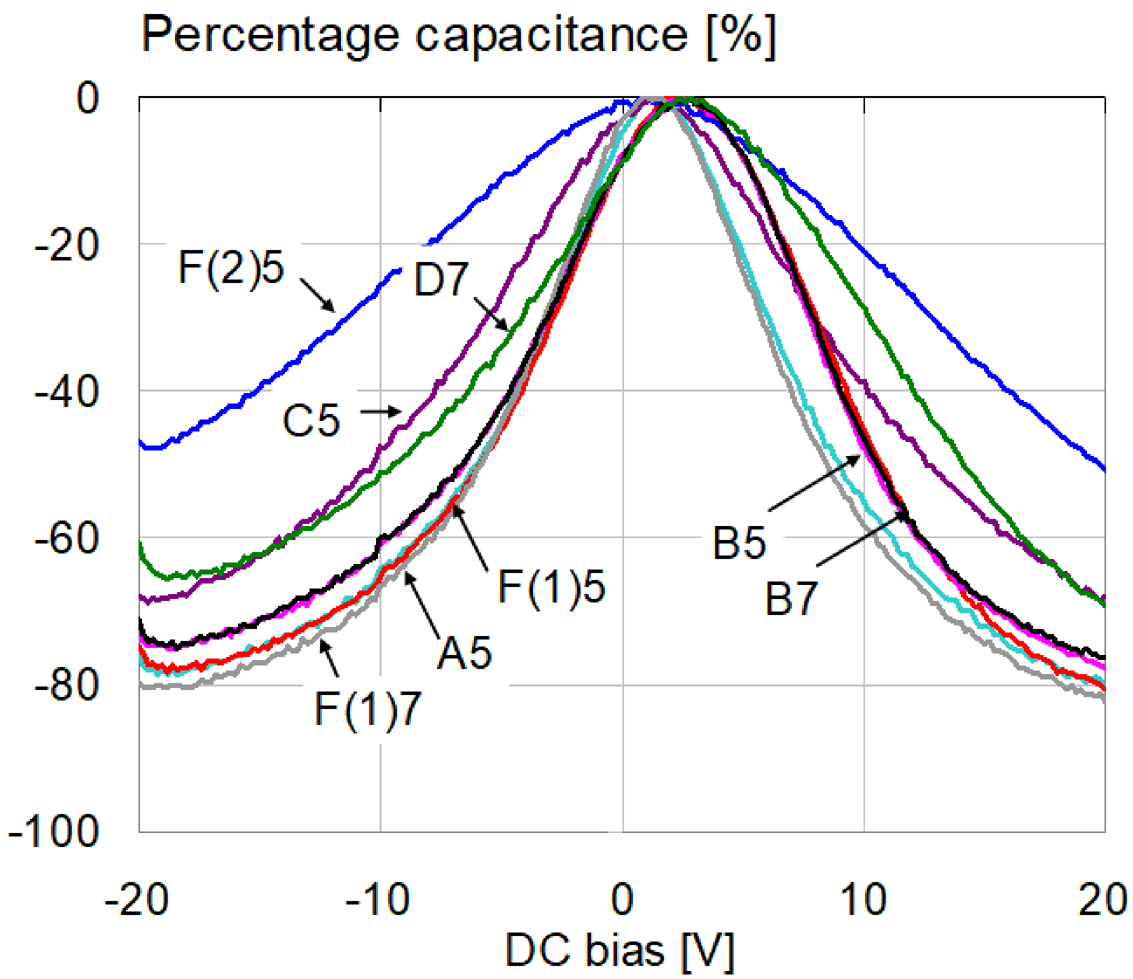


The specification defines the bounding box only, not the shape of the curve

Loss of Capacitance in MLCCs, DC Bias

Old assumptions are not valid any more!

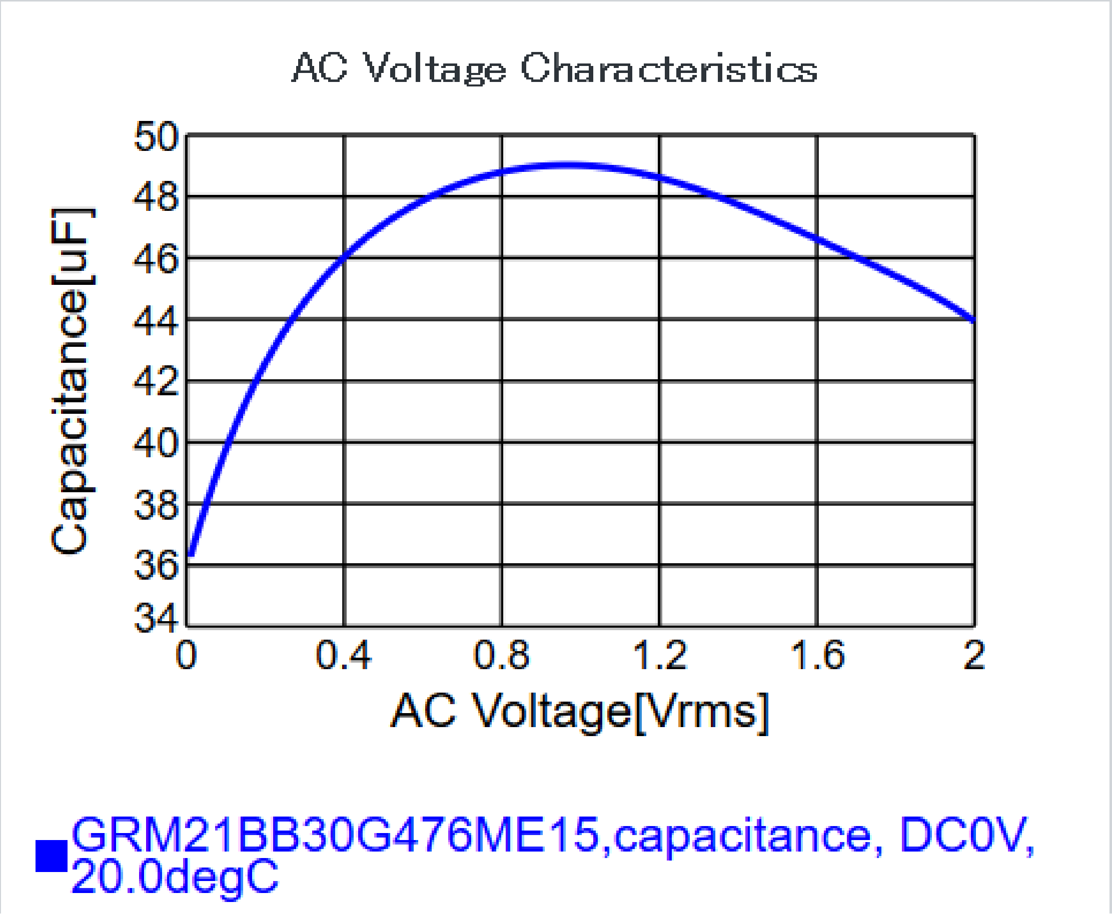
- In the past X7R capacitors were thought to lose less capacitance than X5R capacitors.
- Not true any more
- Last character on plot labels refers to X5R or X7R



Source: "How Much Capacitance Do We Really Get?," QuietPower columns, http://www.electrical-integrity.com/Quietpower_files/QuietPower-40.pdf

Loss of Capacitance in MLCCs, AC Bias

* Vendors test with 0.5 or 1.0Vrms source voltage at 100/120Hz
* Most of the source voltage appears across the DUT
* Bypass applications call for mV or tens of mV noise across the capacitors
* In small signal applications we loose 20-30% capacitance



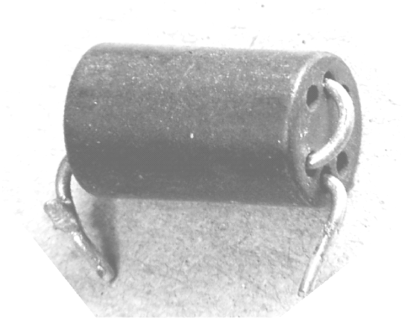
Source: https://psearch.en.murata.com/capacitor/product/GRM21BB30G476ME15%23.html

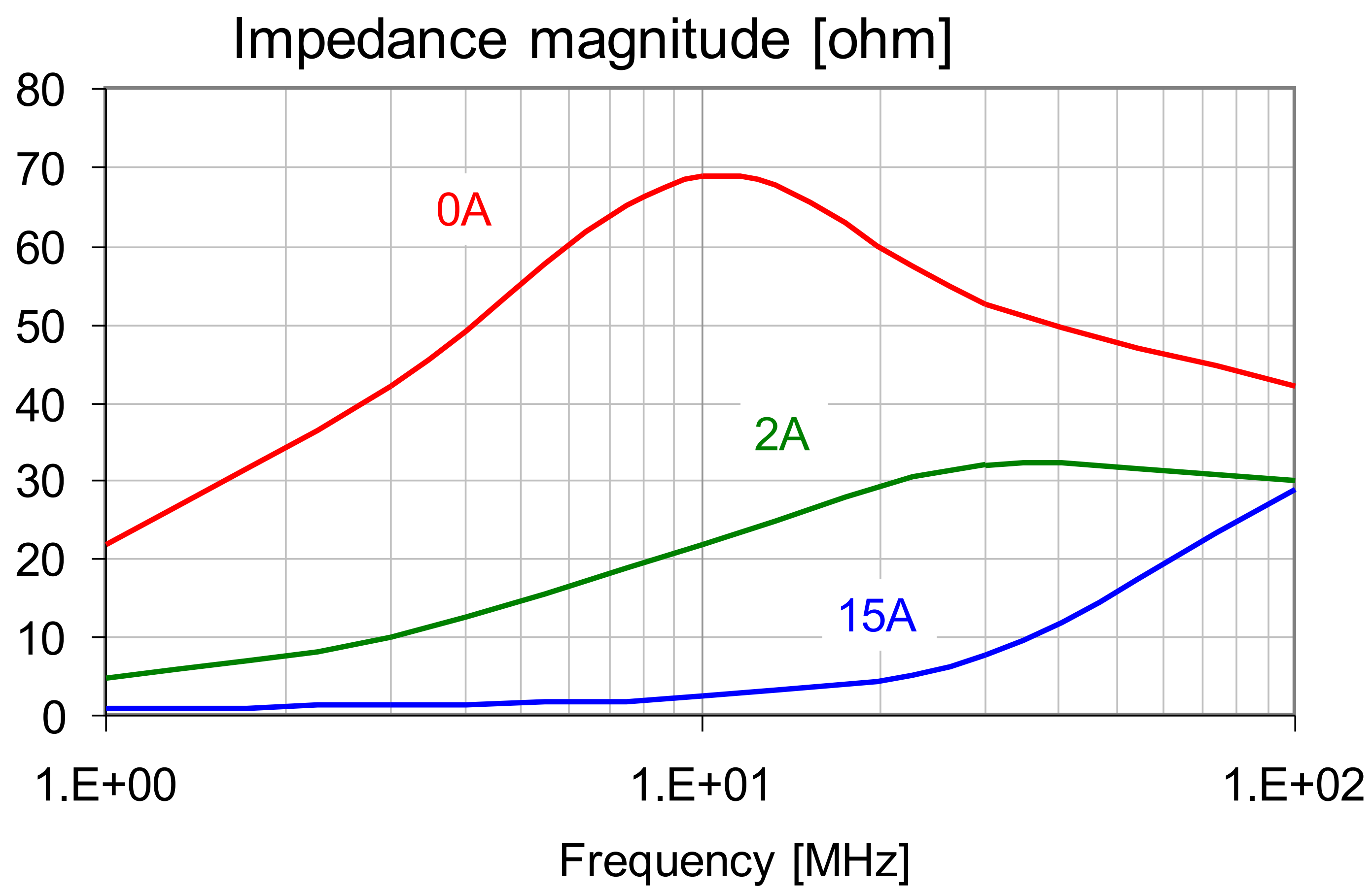
The Good News

Other capacitor types show minimal or no DC or AC bias effect.

Loss of Inductance in Ferrite Beads

* High permeability materials can lose significant inductance
* Highest impact is DC current





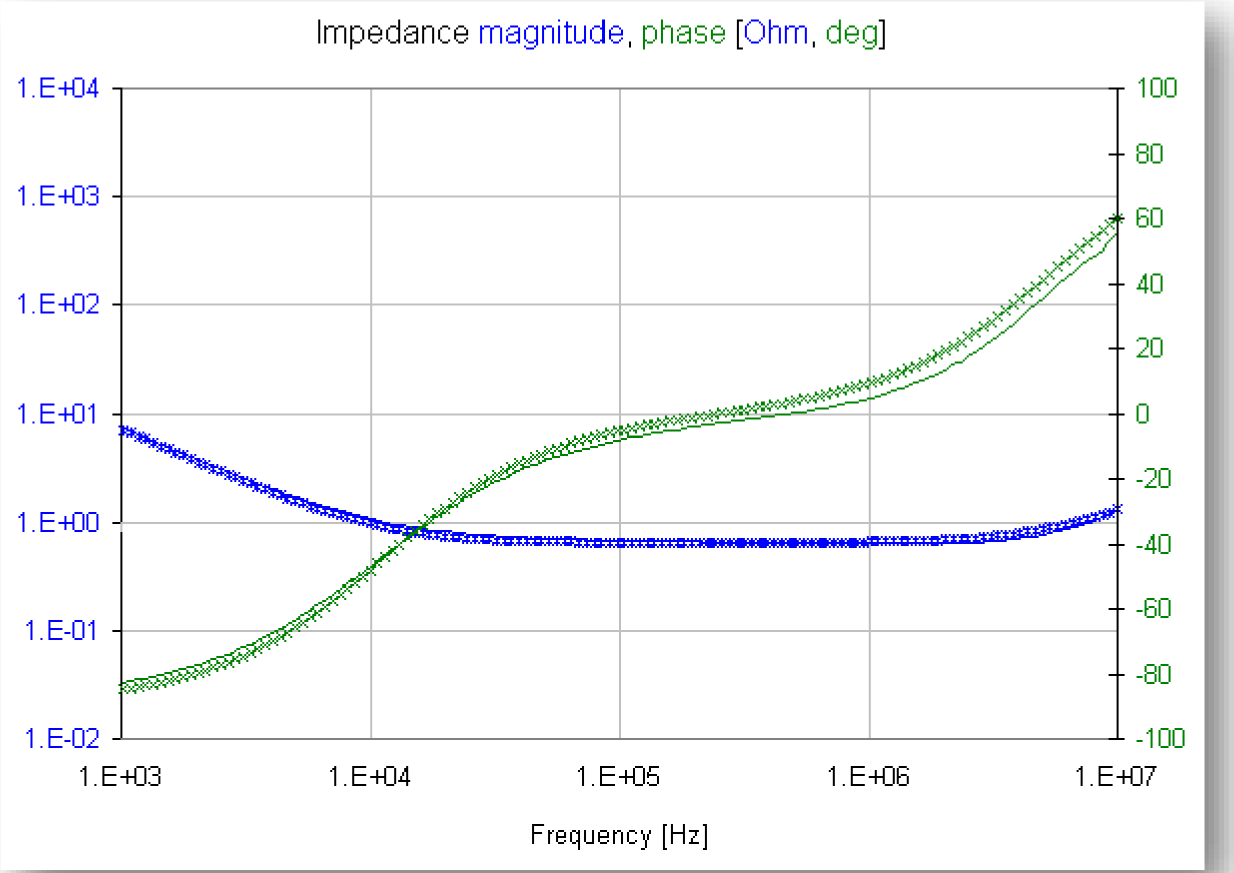
OUTLINE

* Introduction, scope
* Requirements
* Filter design procedure
* What can go wrong
  - Wrong layout
  - Bias dependence
* Simulations and correlations
* Demos

Simulation Models

* Ideal C (default model in some tools)
* C-R, frequency independent (used in DC-DC modeling
* C-R-L, frequency independent (simple SPICE subcircuits)
* C-R-L, frequency dependent fitted models
* S-parameter models, series or parallel
* 2-D RLC grid
* 3-D RLC grid
* Dynamic models

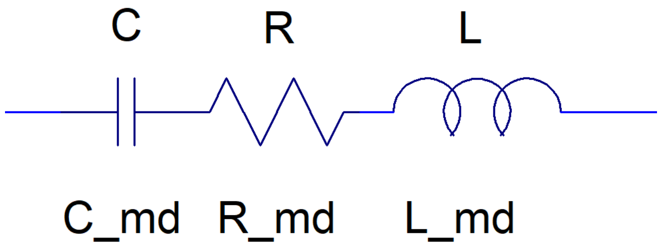
Model Fitted to Measured Data

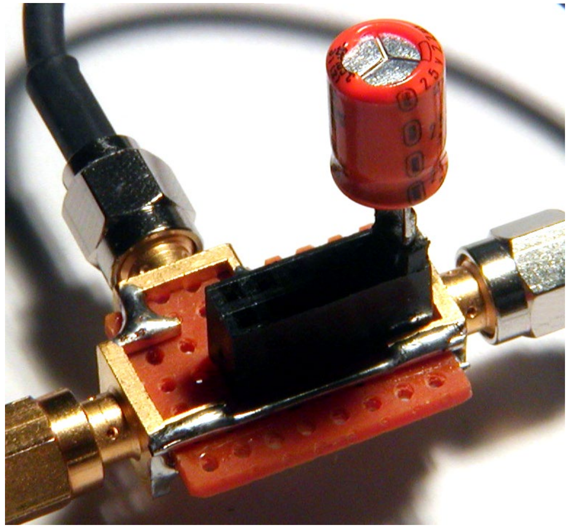


22uF Alu

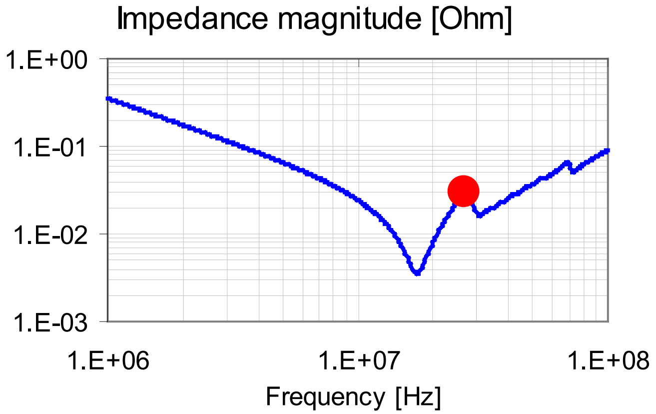
MODEL PARAMETERS:

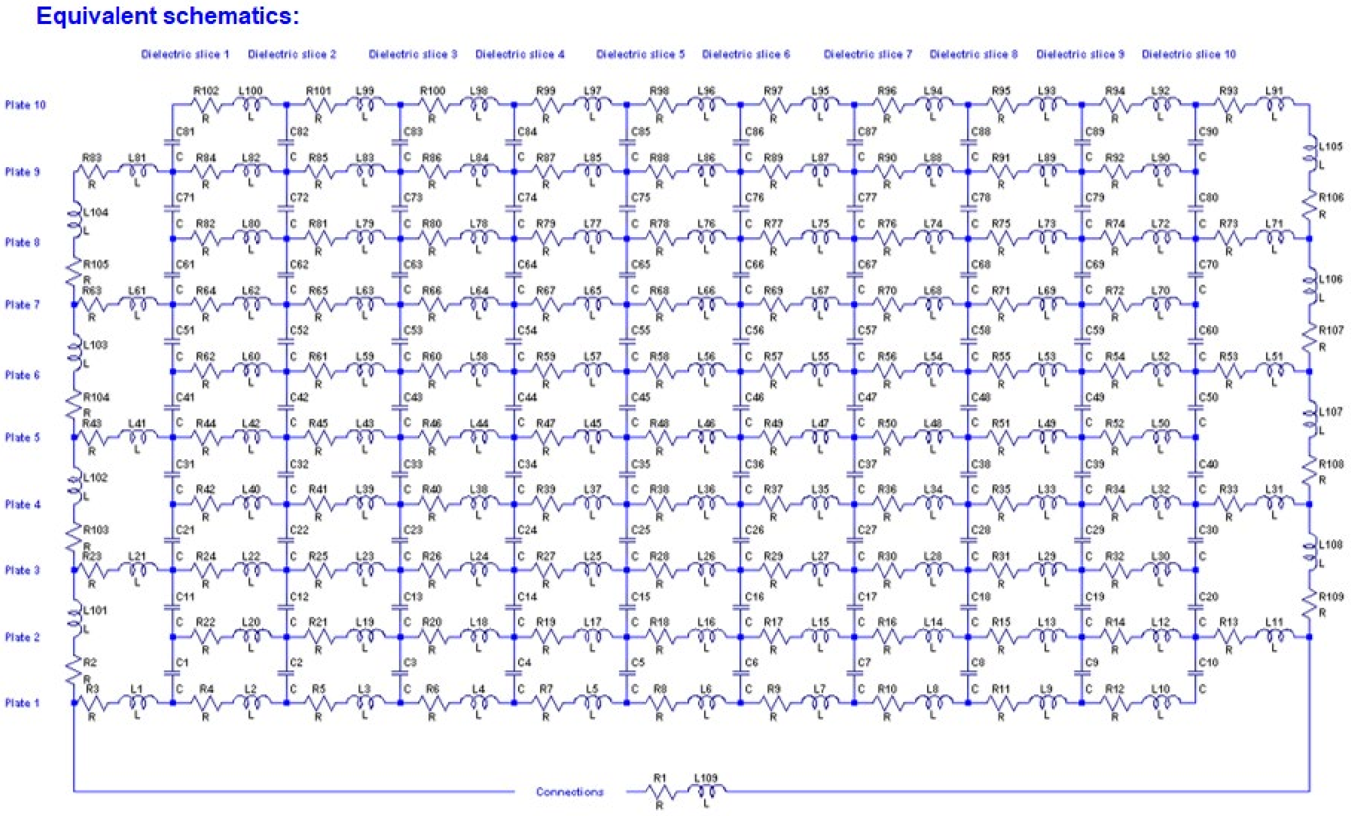
C_md	R_md	L_md
2.20E-05	6.50E-01	1.80E-08



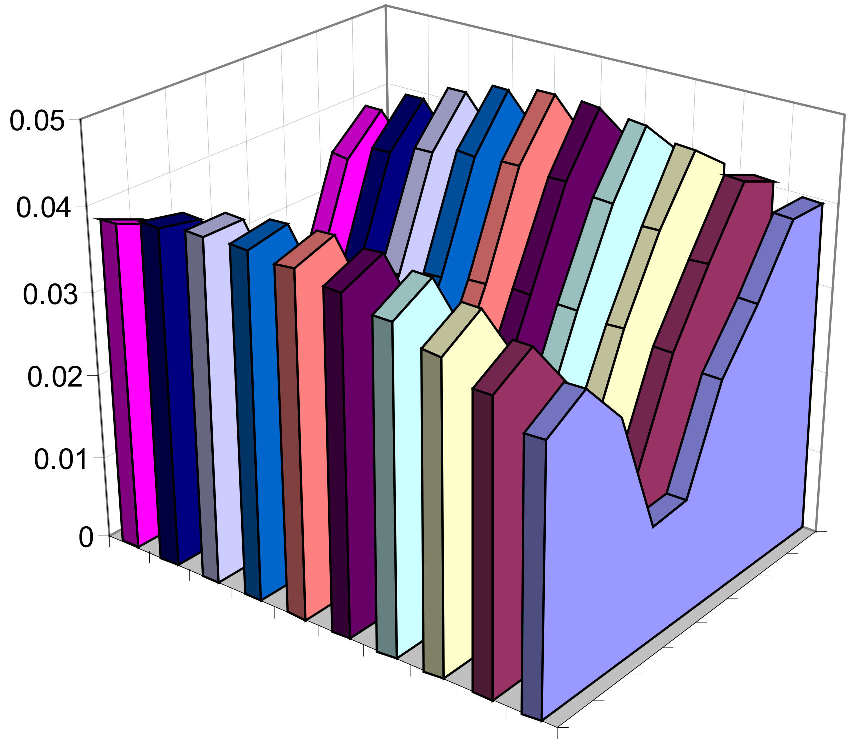


2D Grid MLCC Model

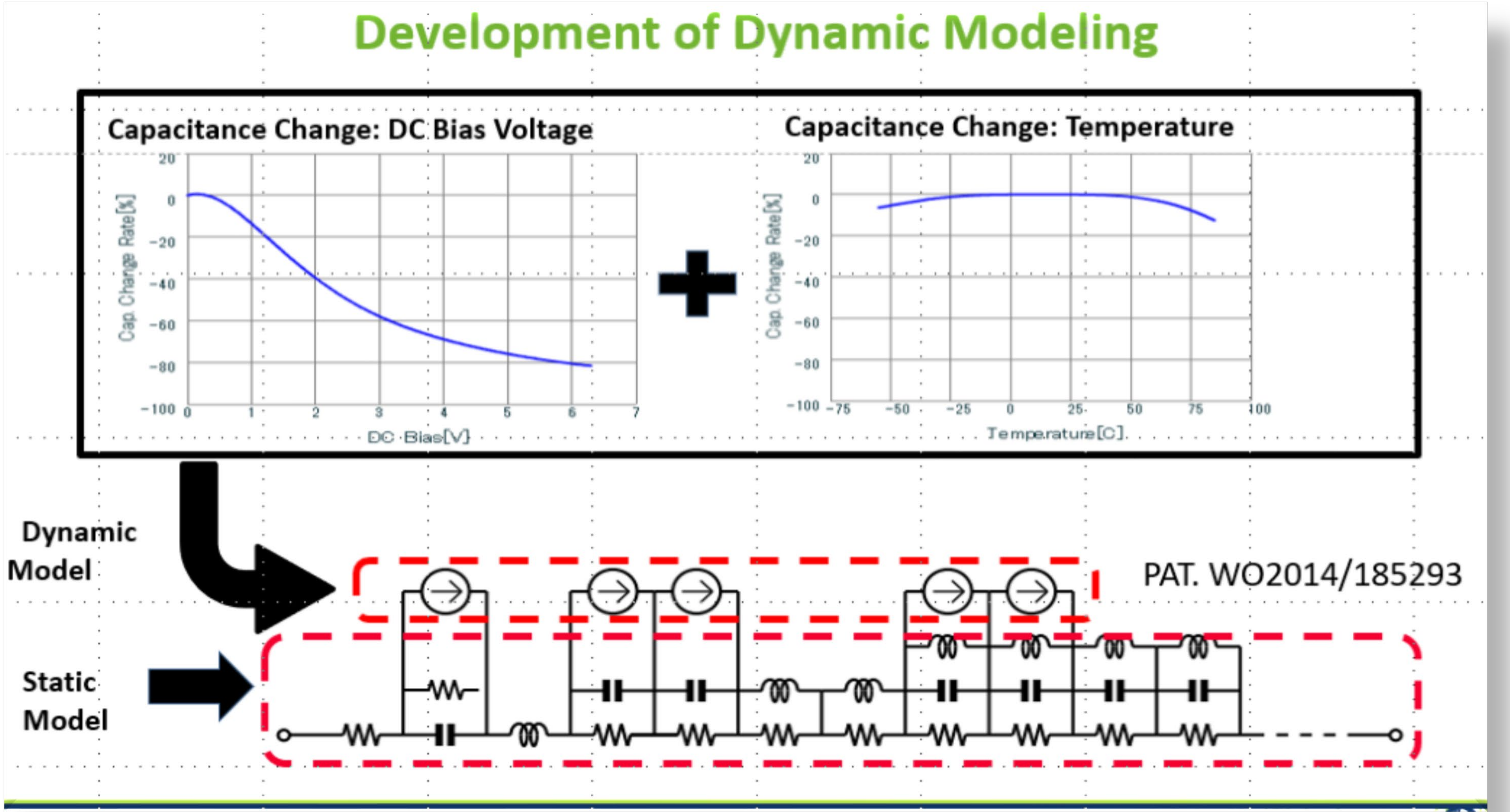




Dielectric current at parallel resonance [A]

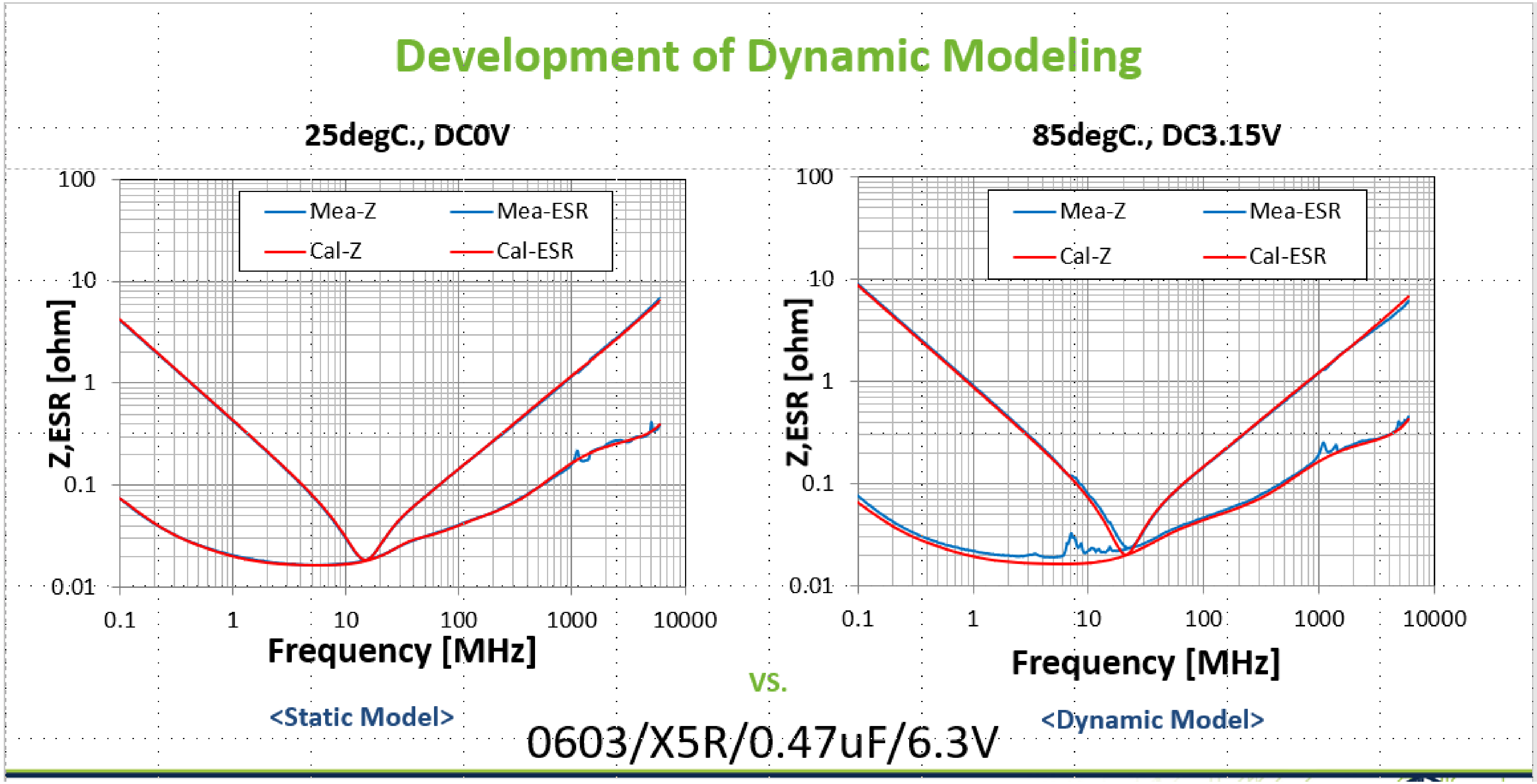


Modeling Capacitance and Inductance Variations



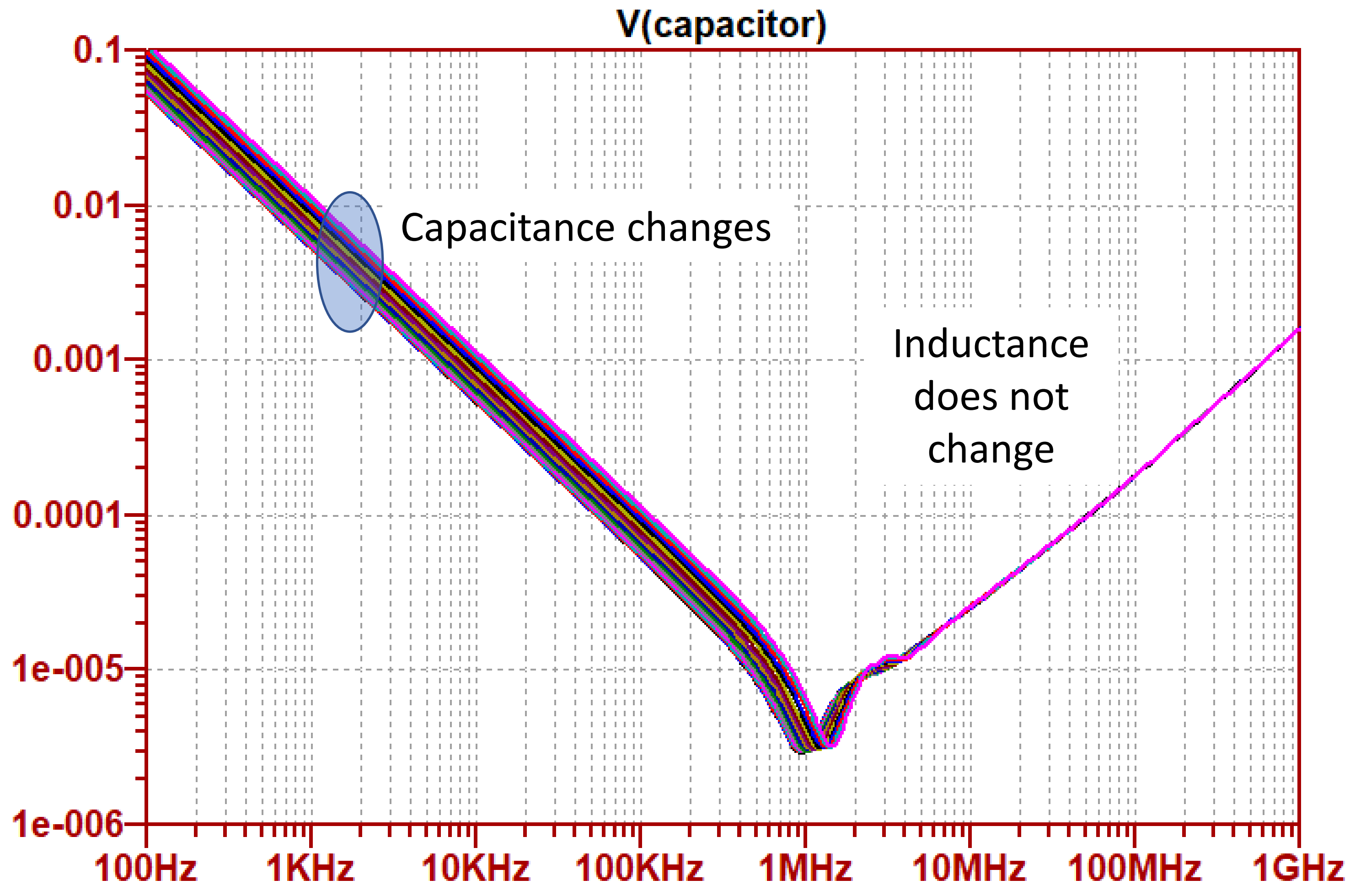
Source: "Needs and Capabilities for Modeling of Capacitor Derating," DesignCon 2016, courtesy of Shoji Tsubota

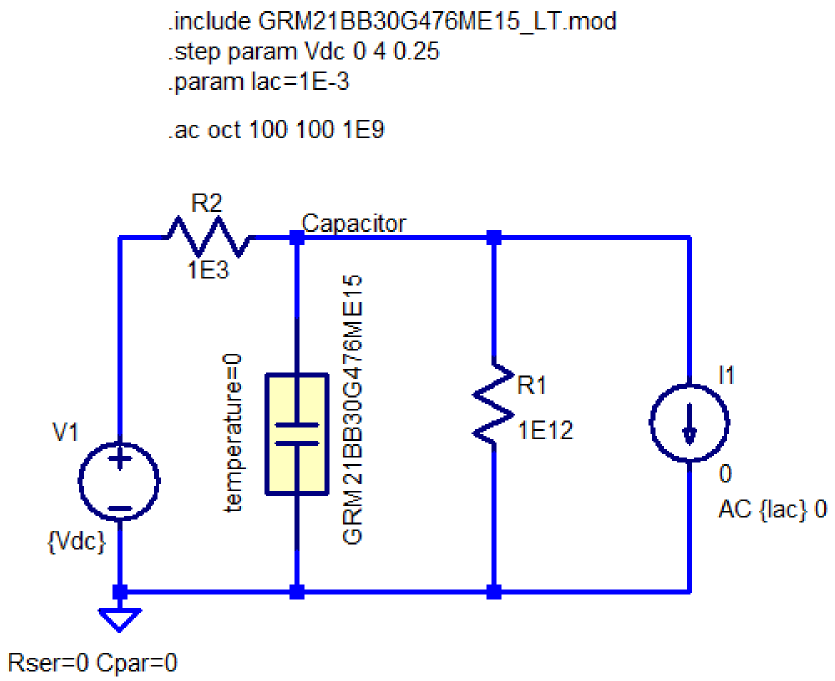
Modeling Capacitance and Inductance Variations



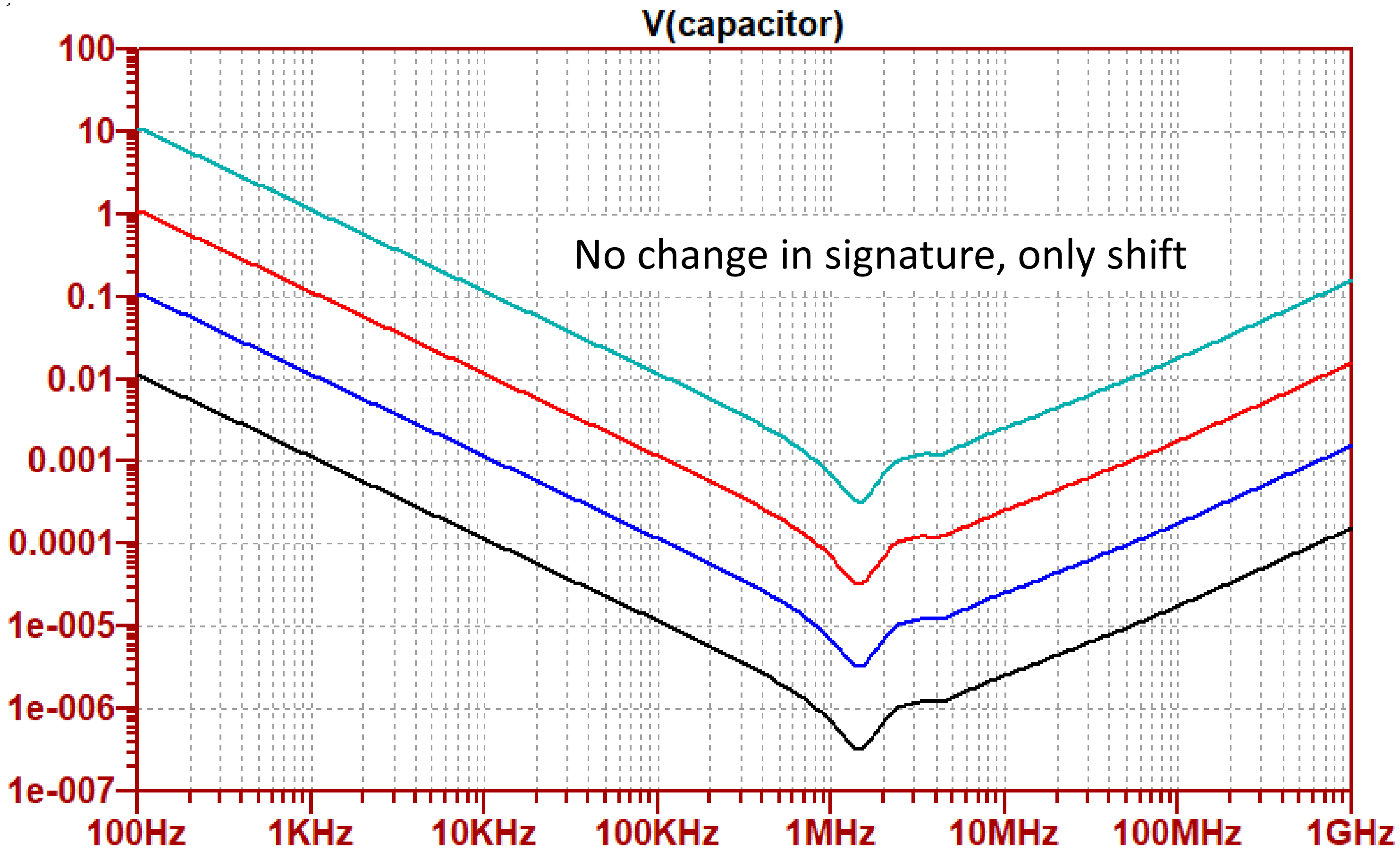
Source: "Needs and Capabilities for Modeling of Capacitor Derating," DesignCon 2016, courtesy of Shoji Tsubota

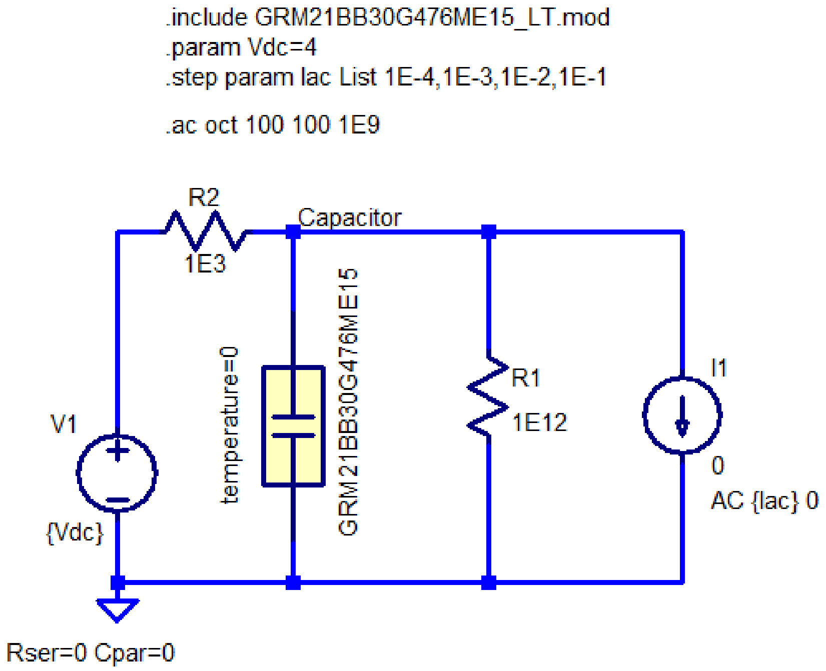
Dynamic Models, Testing Small Signal DC Bias



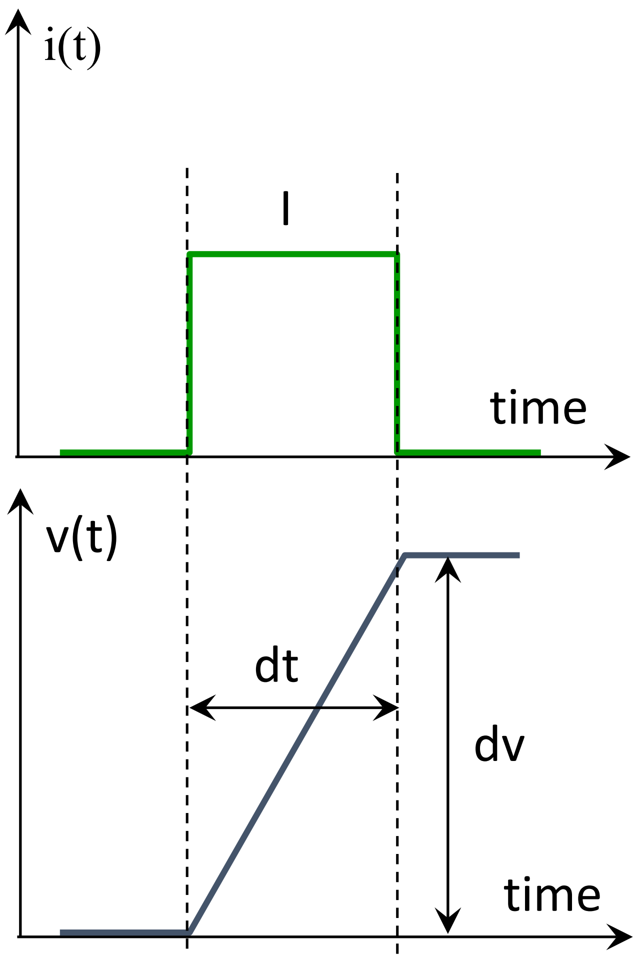


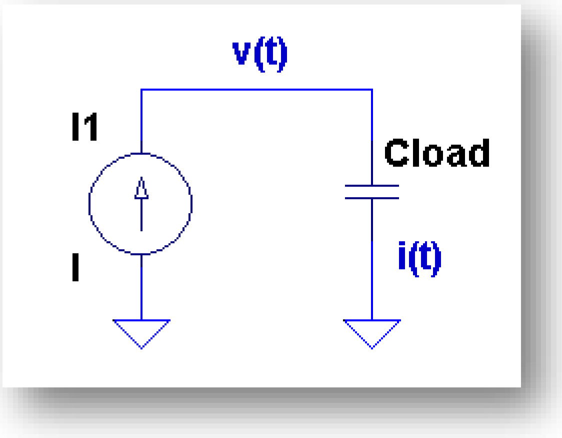
Dynamic Models, Effect of AC Test Current





Dynamic Models, Test Large-signal Nonlinearity



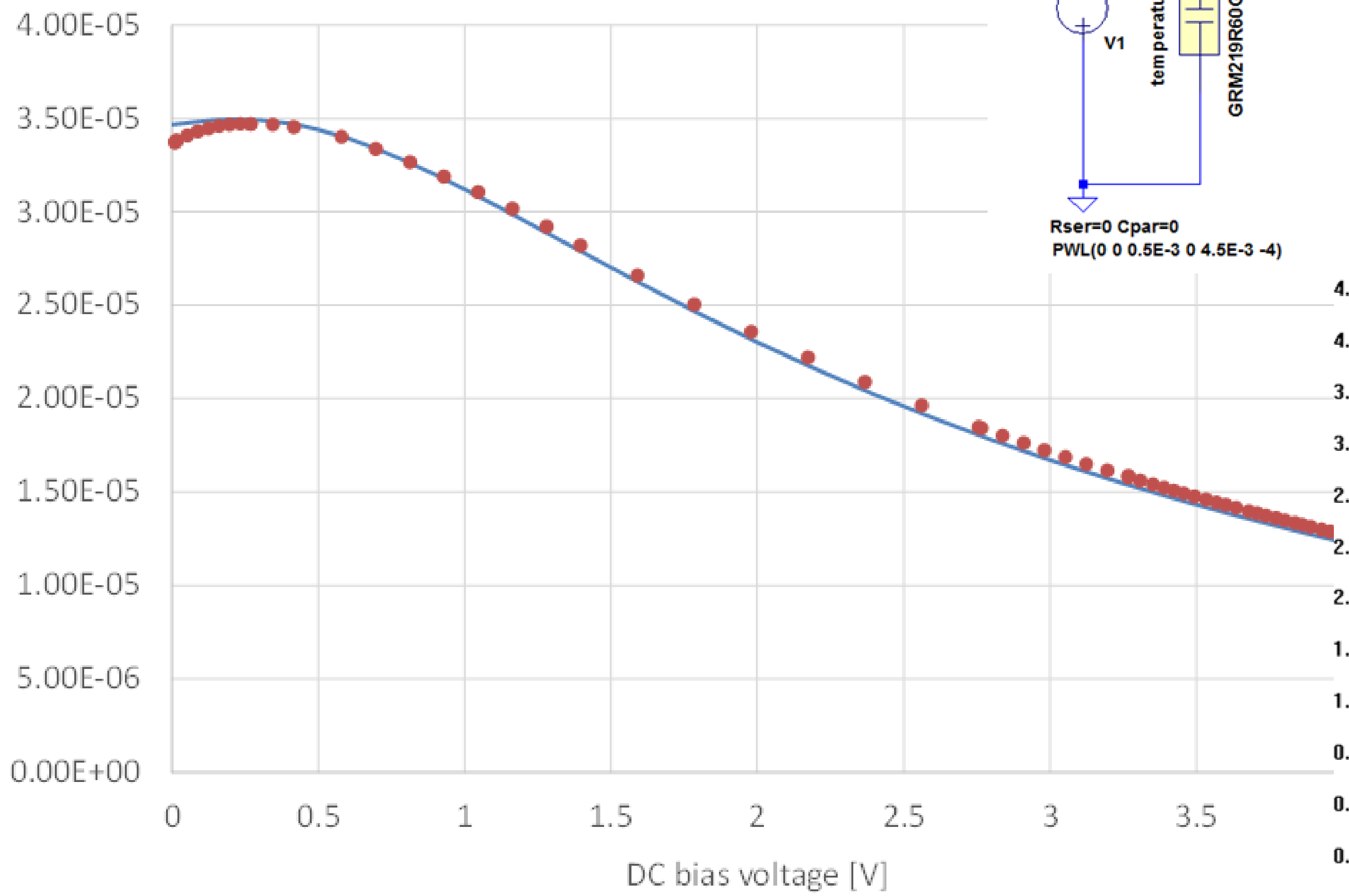


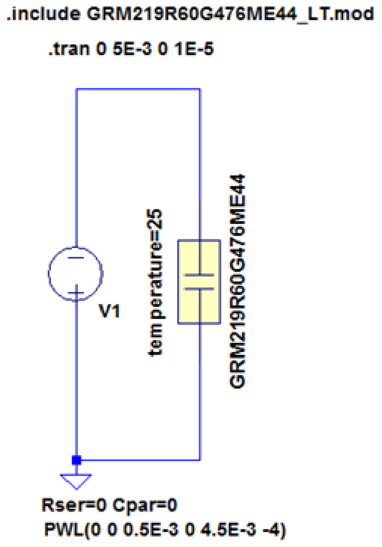
Charge balance:

$$I*dt = C*dv \rightarrow C = I / (dV/dt)$$

Source: "Dynamic Models for Passive Components," QuietPower columns, http://www.electrical-integrity.com/Quietpower_files/QuietPower-36.pdf

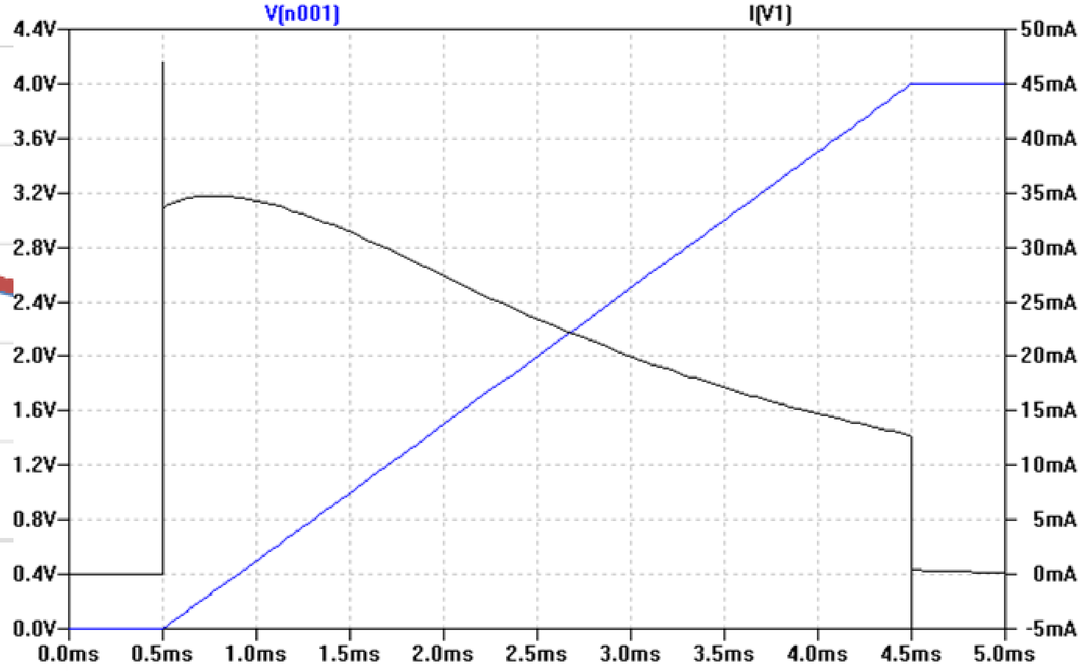
Dynamic Models





Source: “Dynamic Models for Passive Components,” QuietPower columns, http://www.electrical-integrity.com/Quietpower_files/QuietPower-36.pdf

$$BW = 0.35/t_r = 0.35/4ms \sim 100Hz$$



Acknowledgement and Resources

Special thanks to

- Keysight and Picotest for providing demo equipment
  - https://literature.cdn.keysight.com/litweb/pdf/5990-4392EN.pdf
  - https://www.picotest.com/products_BODE100.html
- Murata for assisting with dynamic models and samples
  - https://www.murata.com/en-us/tool
- Simulations were done with Analog Devices' free LTSPICE
- Filter evaluation boards
  - https://www.sv1afn.com/rf-experimenter-s-pcb-panel.html

This presentation is based on the following training course materials

https://www.cei.se/course-056-power-integrity-advanced-design-and-characterization-group.html

https://www.cei.se/course-055-signal-integrity-advanced-high-speed-design-and-characterization-group.html

https://www.conted.ox.ac.uk/courses/making-successful-power-distribution-designs

THANK YOU!

Any Questions?

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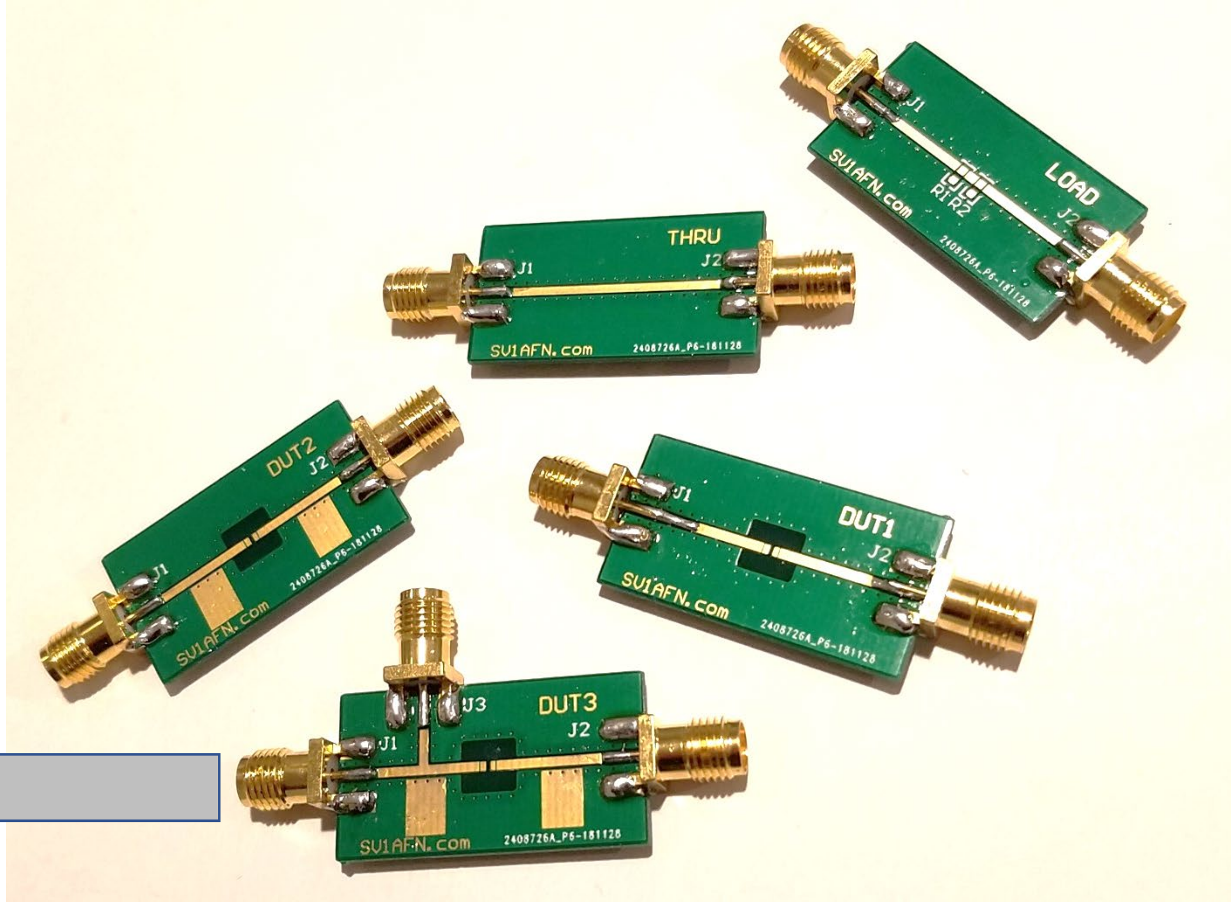
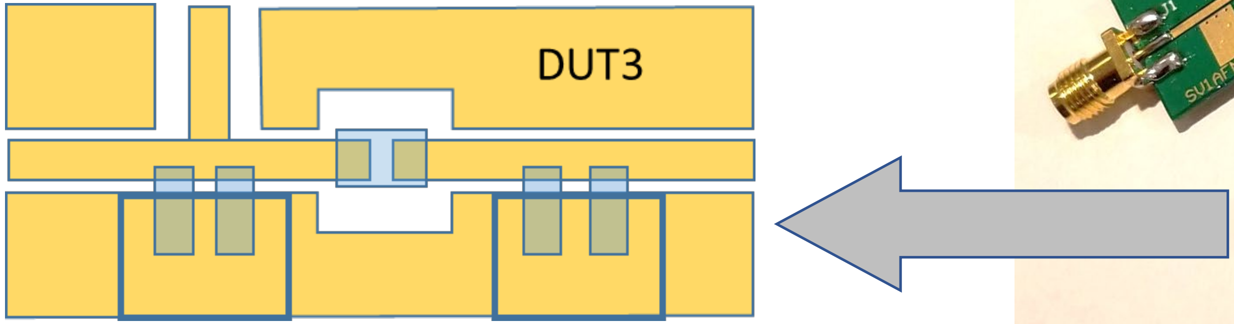
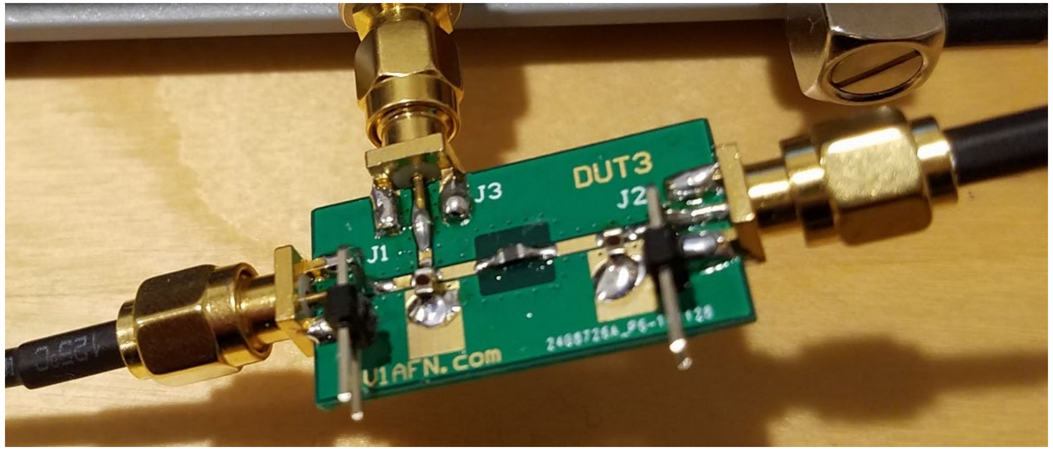
DEMO

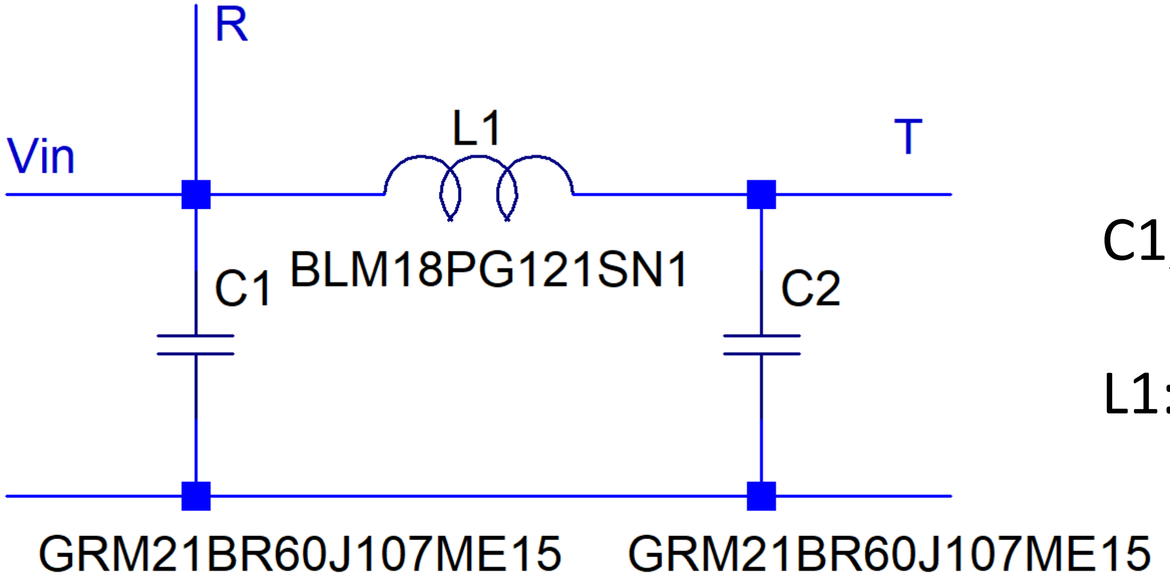
Test Board Construction, Build





DUT Circuit

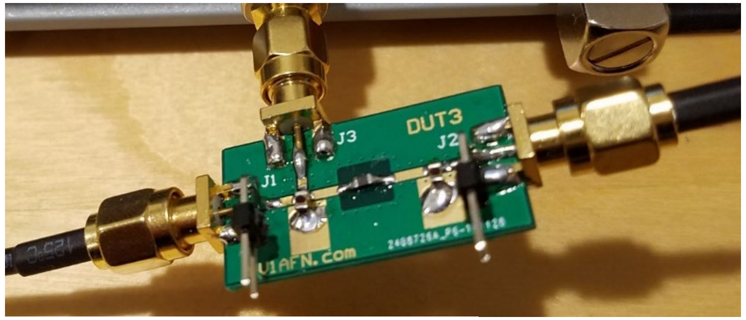




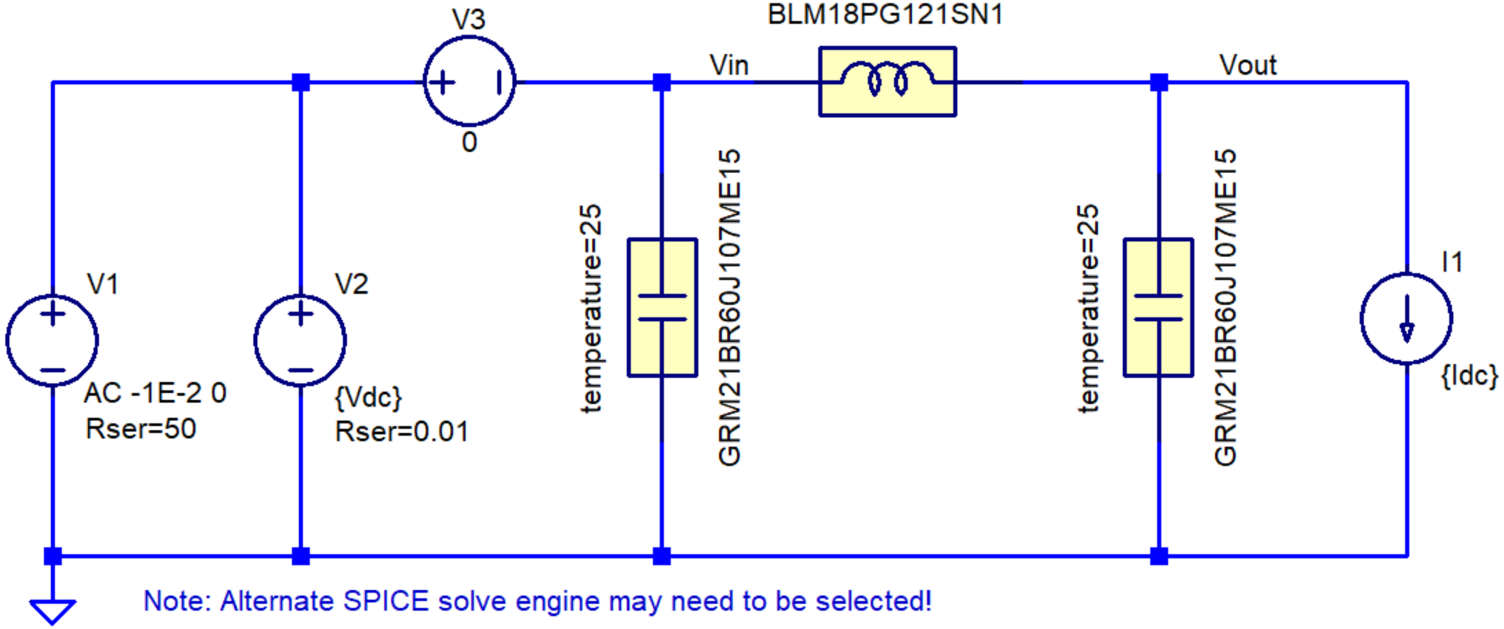
C1, C2: 47uF 4V 0805 X5R MLCC

L1: 120 Ohm @ 100 MHz 0603 2A 50mOhm

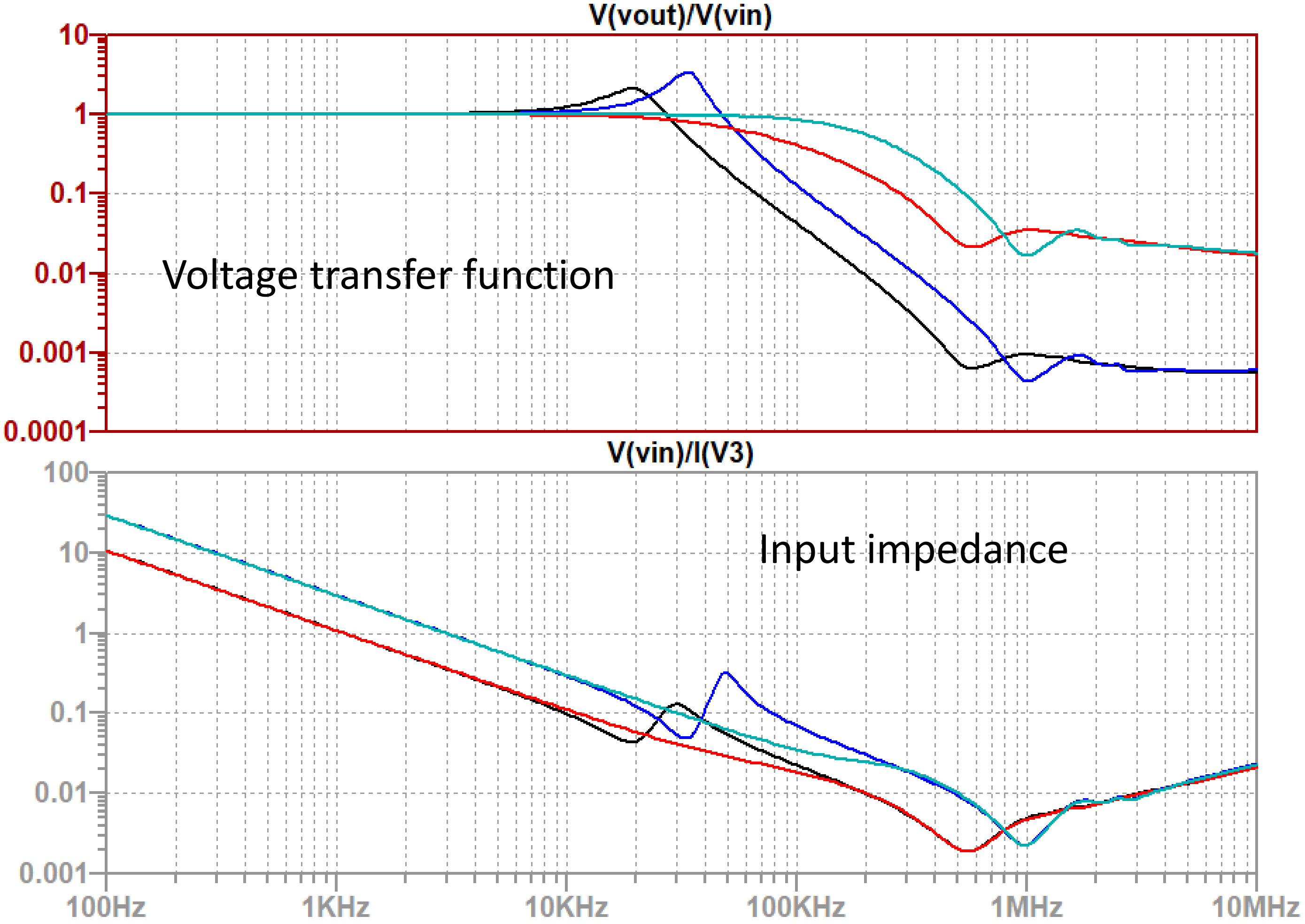
Simulation Setup




```
.ac oct 100 100 1E7
.include GRM21BR60J107ME15_LT.mod
.include BLM18PG121SN1.mod
.step param Vdc List 0,4
.step param Idc List 0,1
```



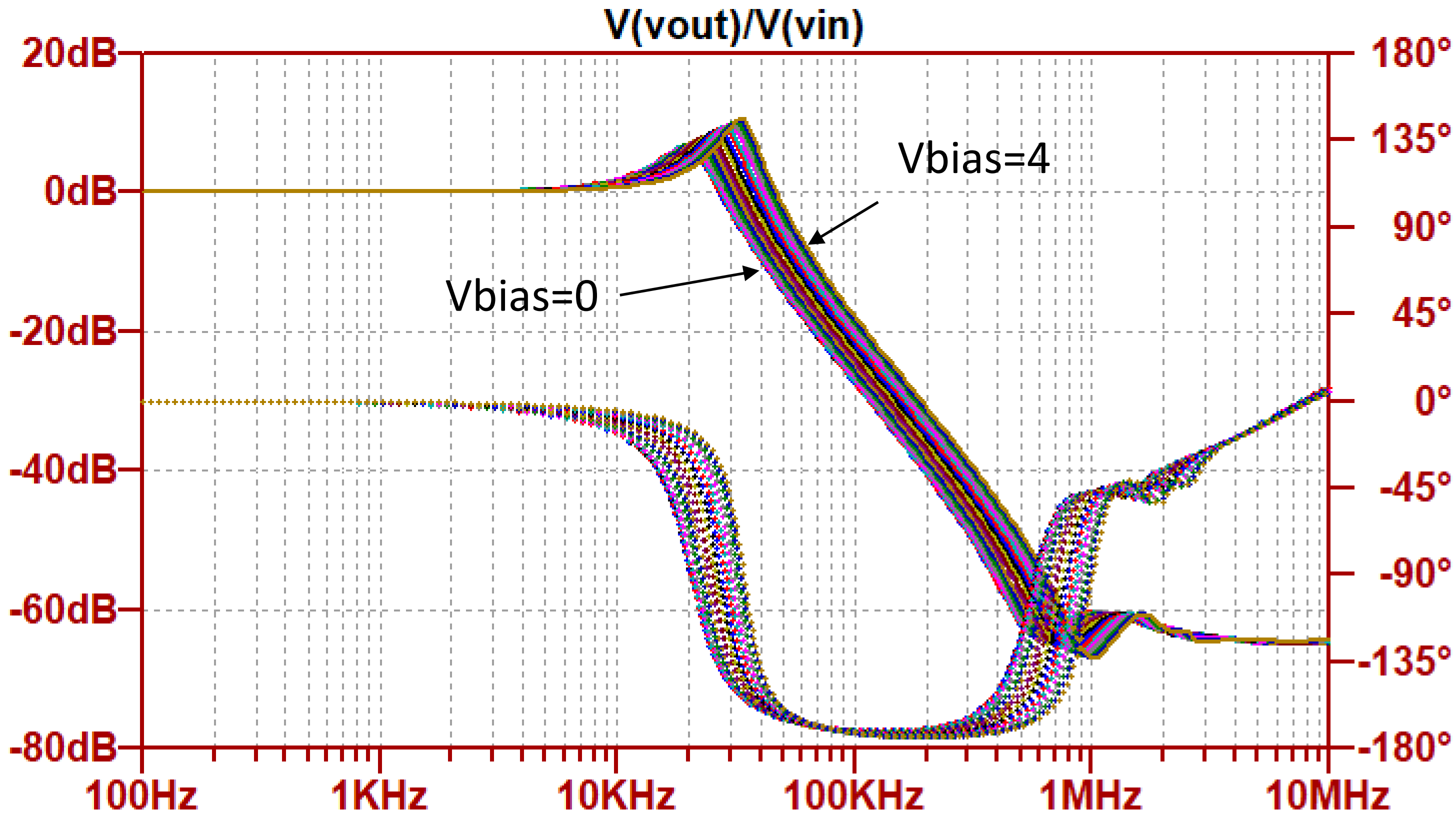
Simulated Corners



Bias:
0V 0A
4V 0A
0V 1A
4V 1A

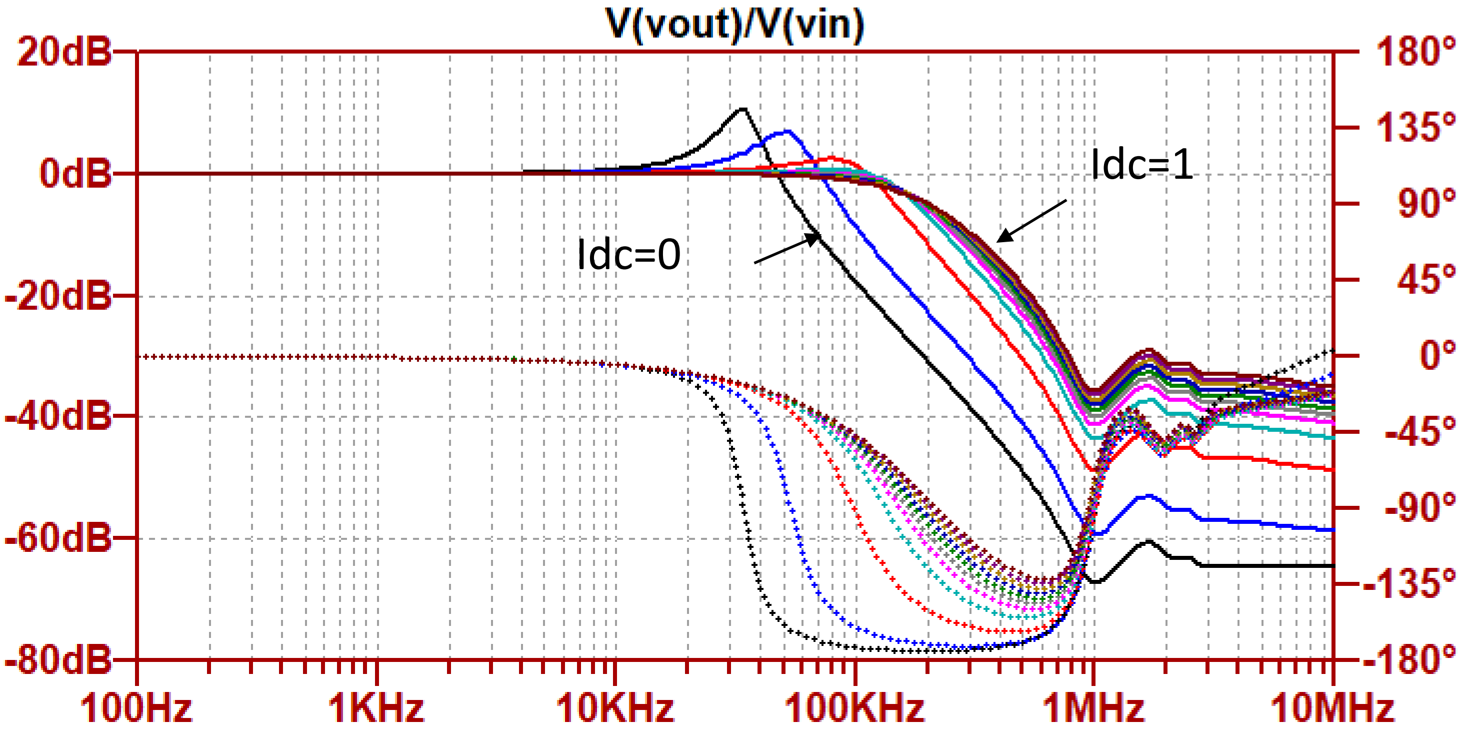
Simulated with LTSPICE and Murata dynamic models.

Simulated Voltage Bias Effect



Simulated with LTSPICE and Murata dynamic models.
Idc = 0A
Vbias = 0…4V

Simulated Current Bias Effect

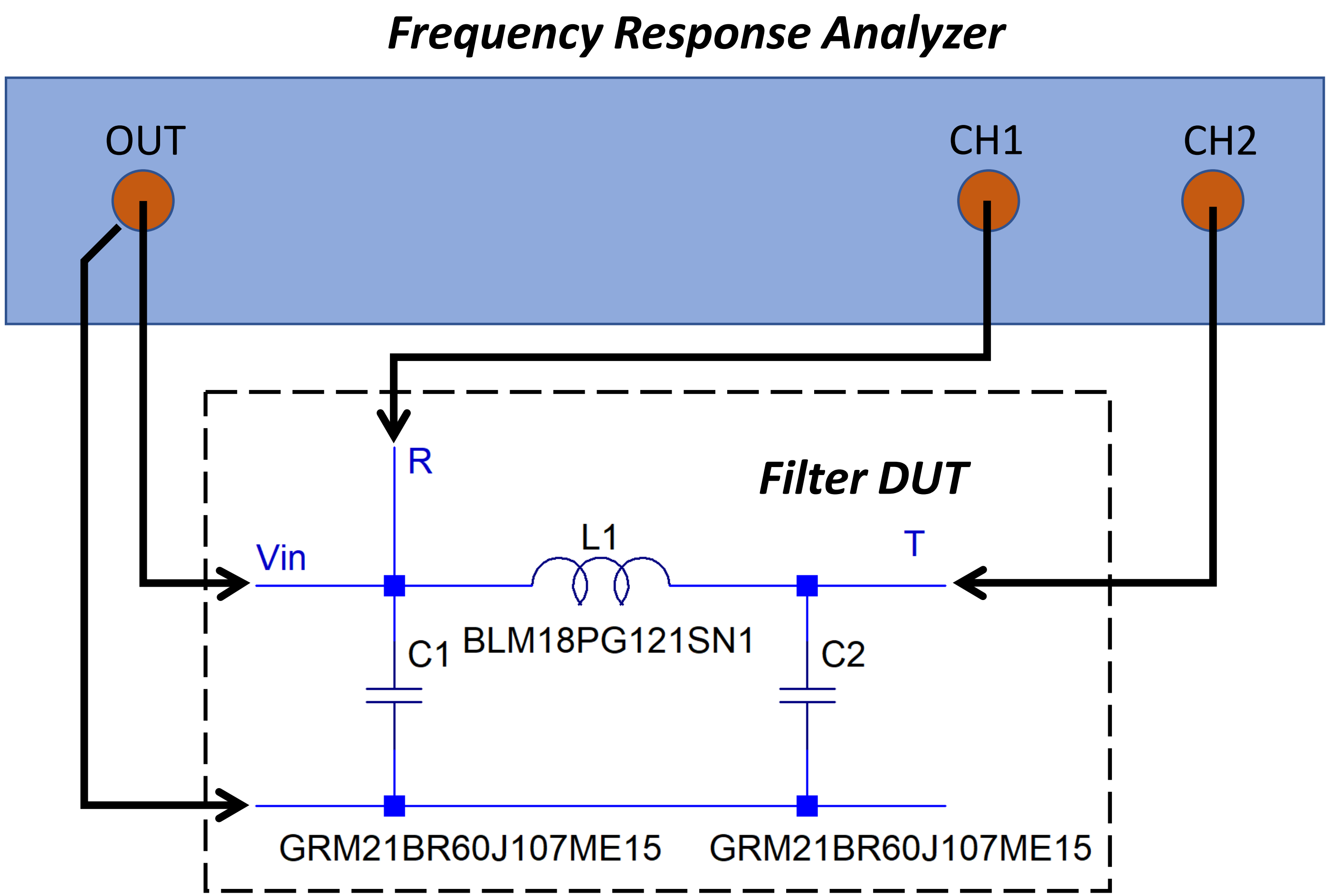


Simulated with LTSPICE and Murata dynamic models.

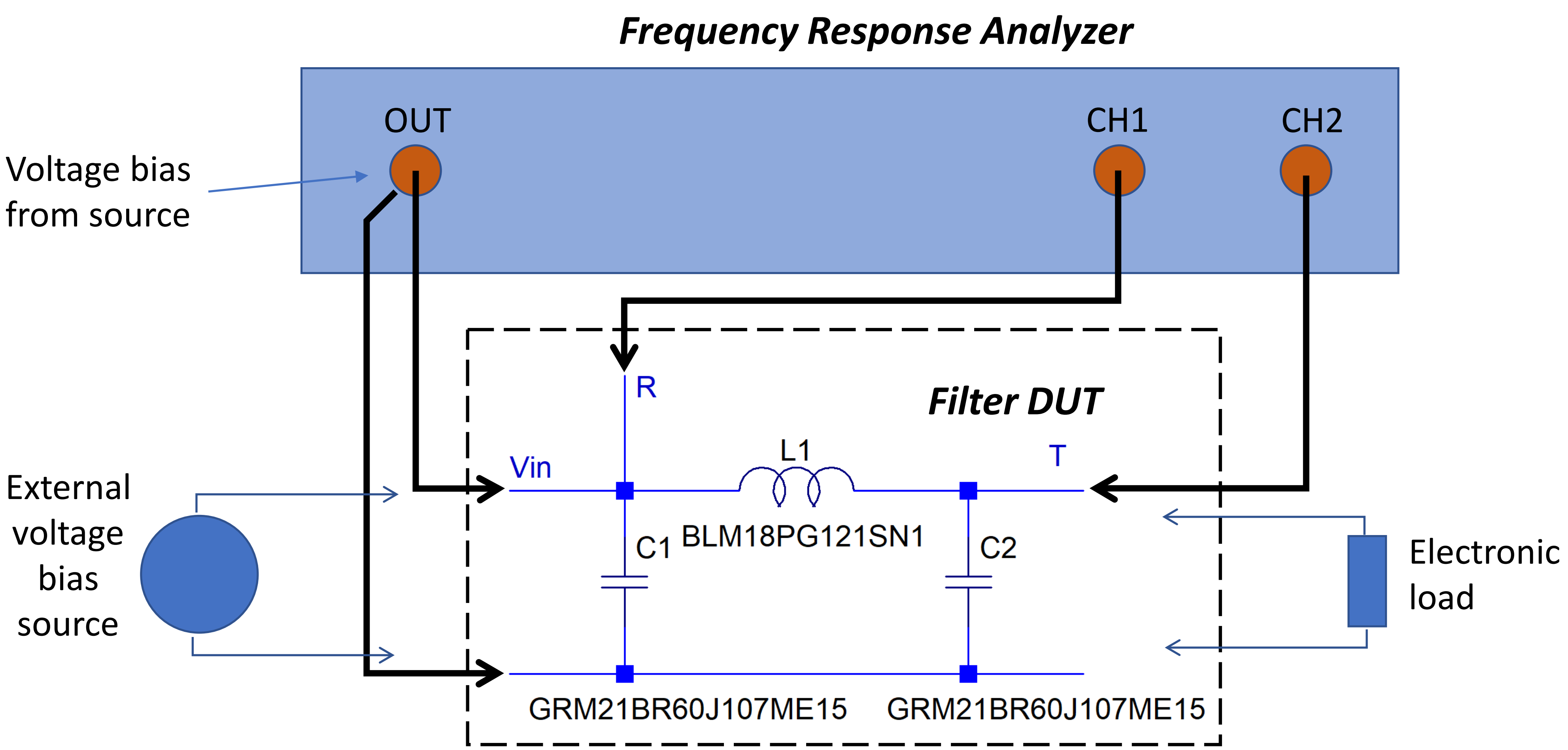
Idc = 0…1A

Vbias =4V

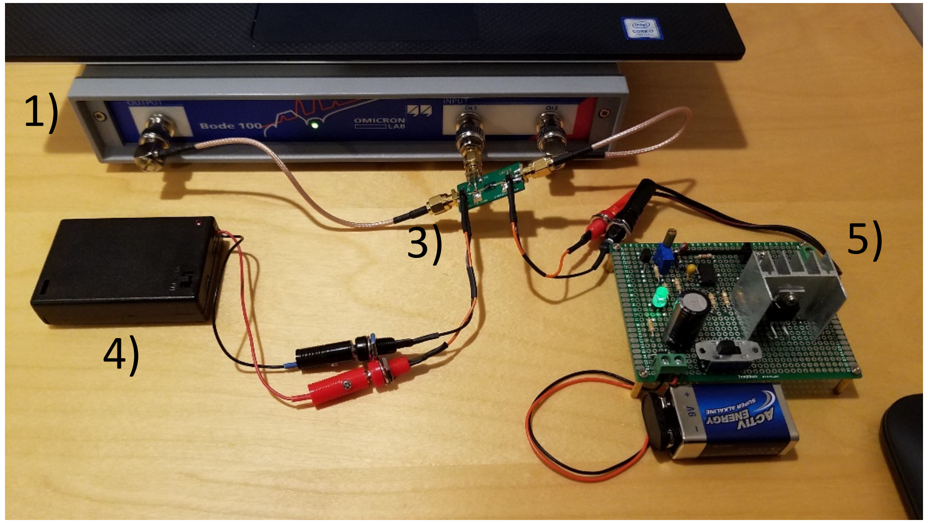
Measurement Setup

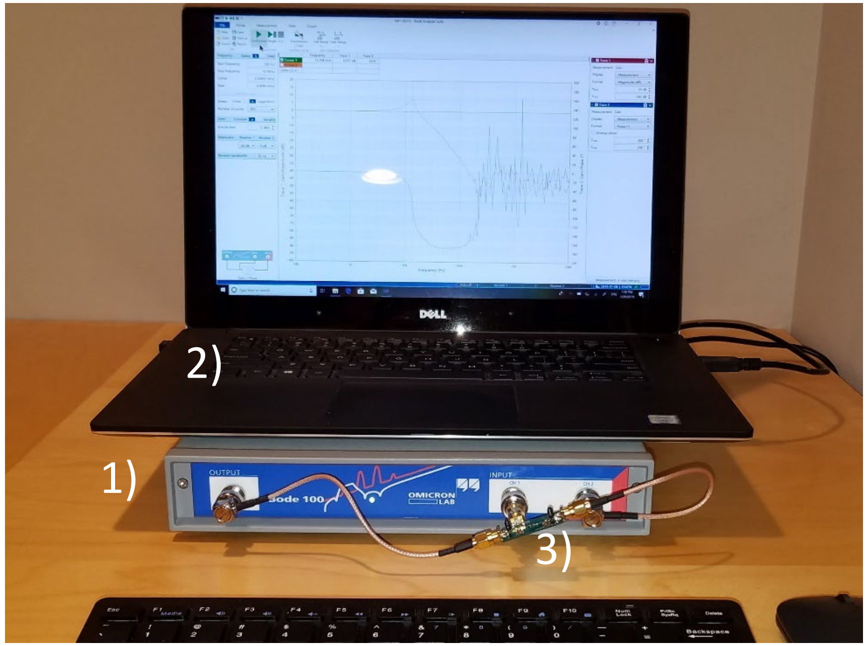


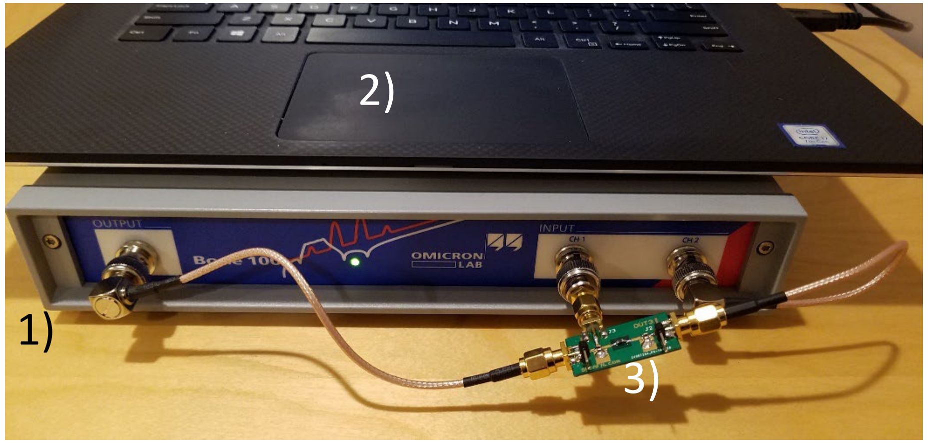
Options for Adding Bias



Bode 100 Setup

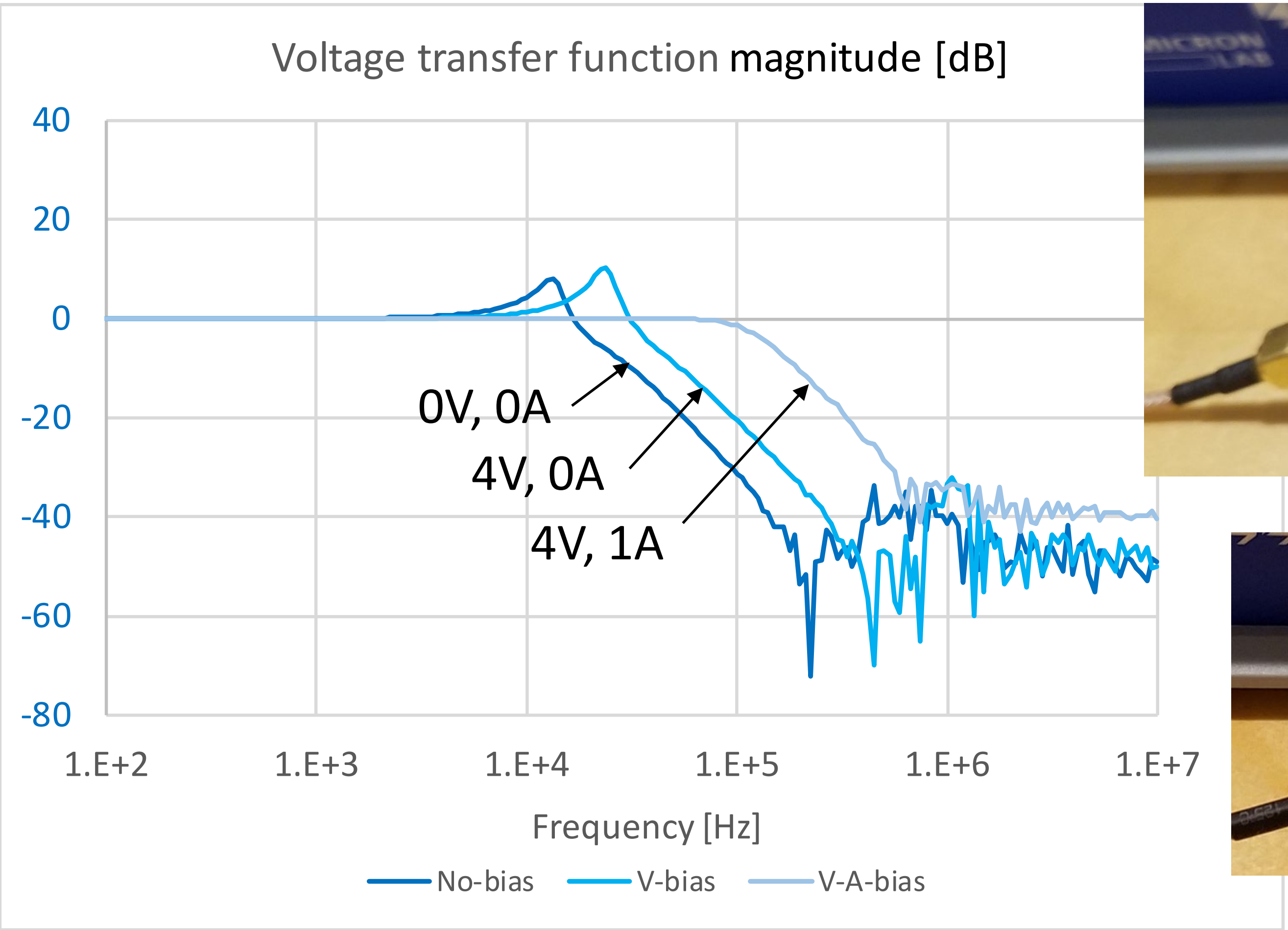


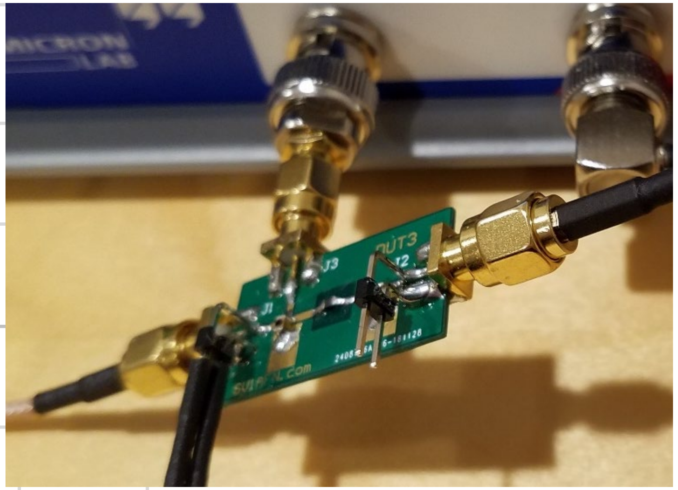


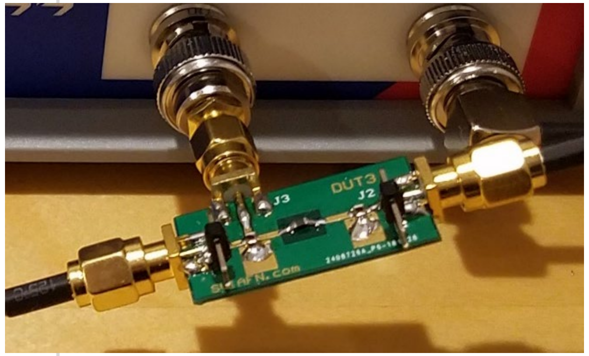


1) Omicron Bode 100
2) Laptop
3) DUT
4) DC voltage bias (battery)
5) DC current bias (electronic load)

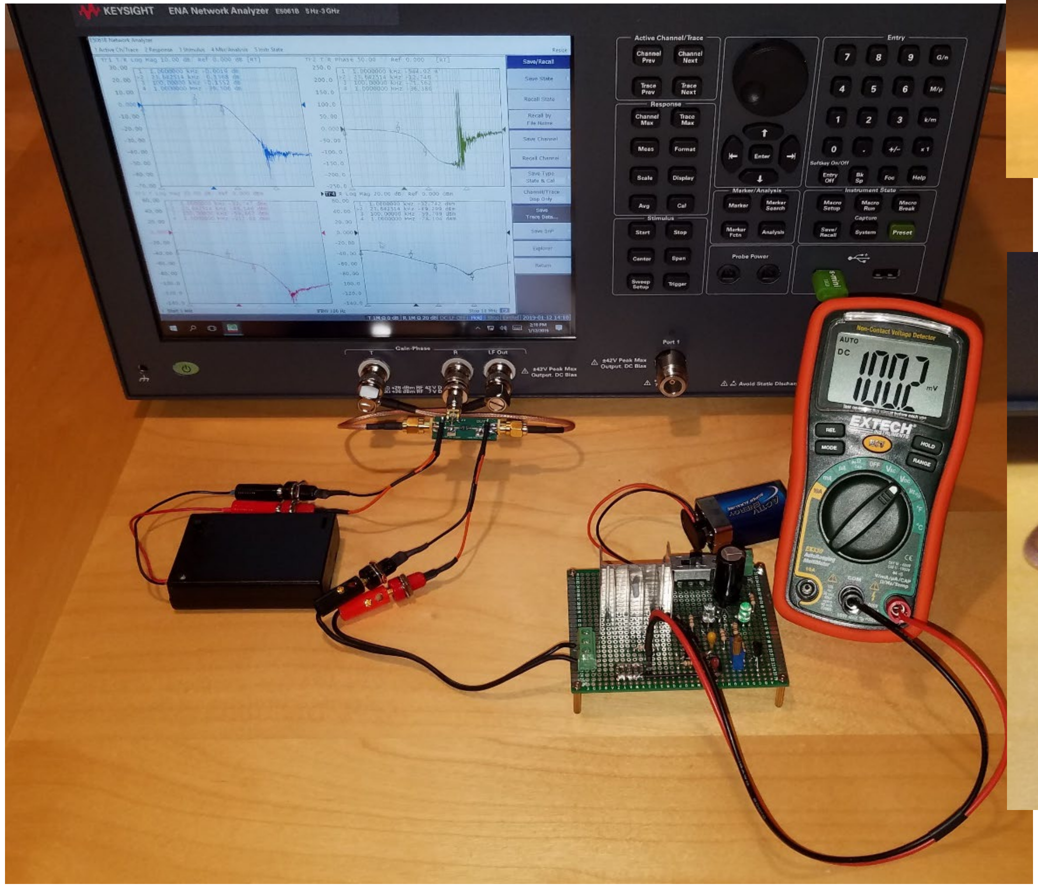
Bode 100 Results

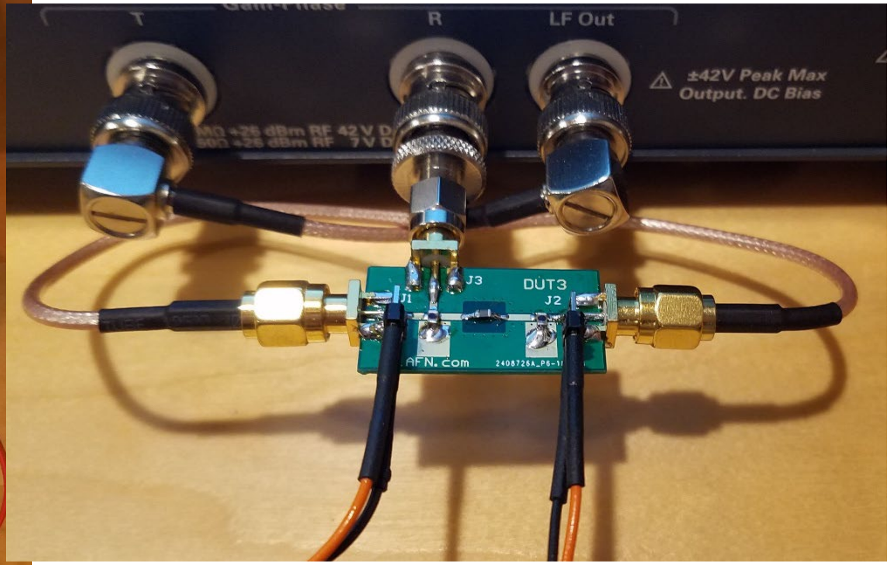




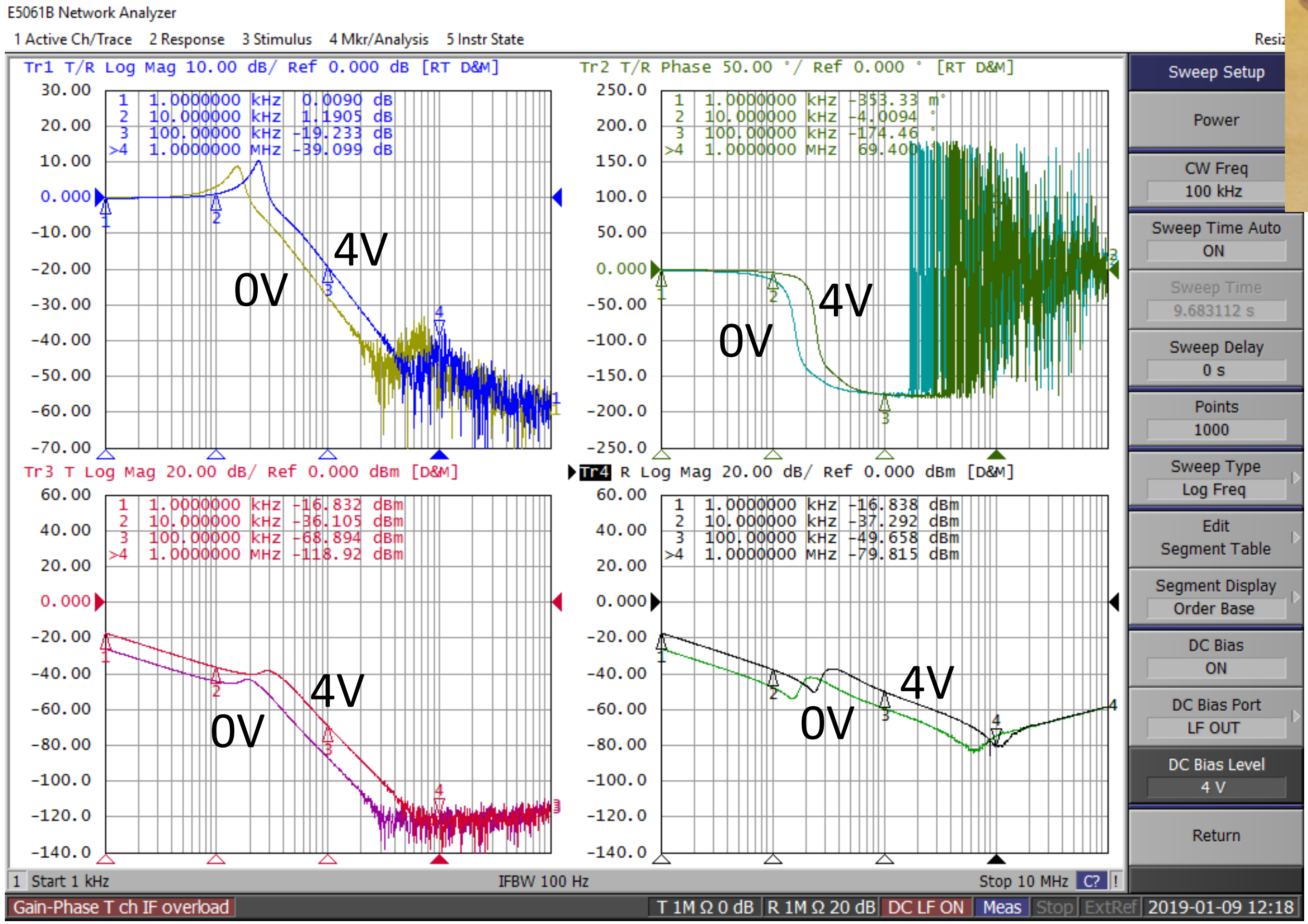


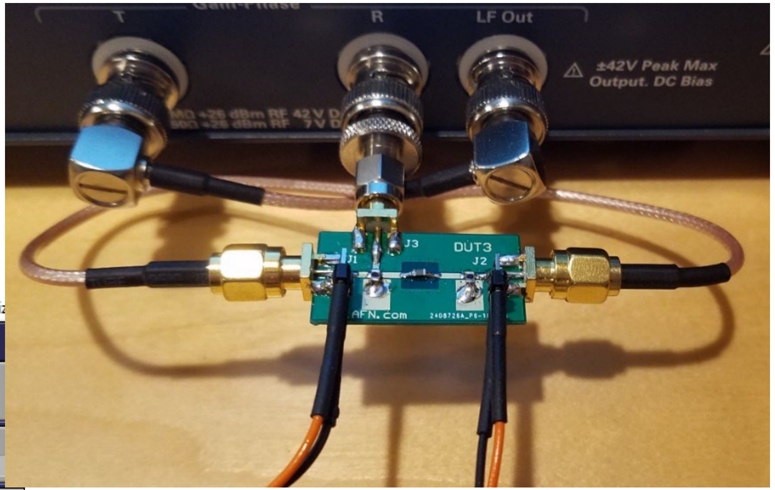
E5061B Gain-Phase Setup





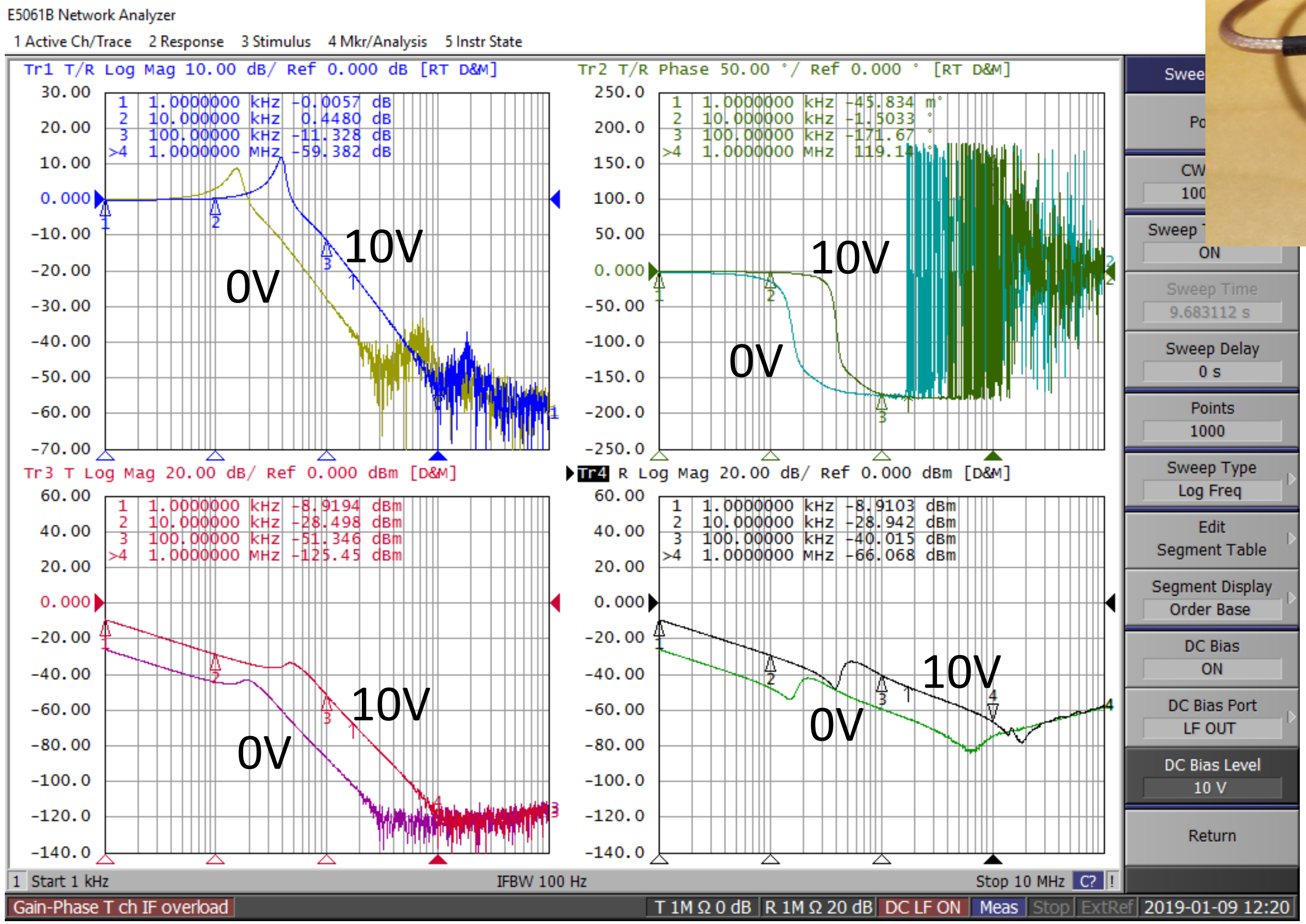
E5061B Gain-Phase Results

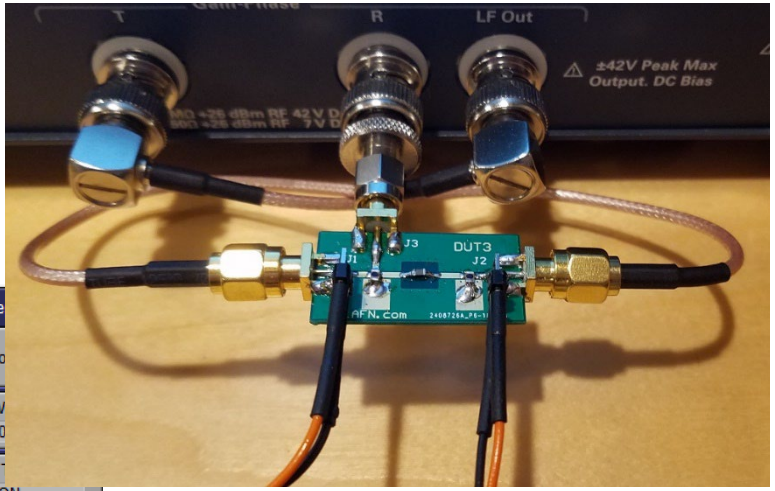




E5061B
0dBm source
0 and 4V DC bias
0A current bias

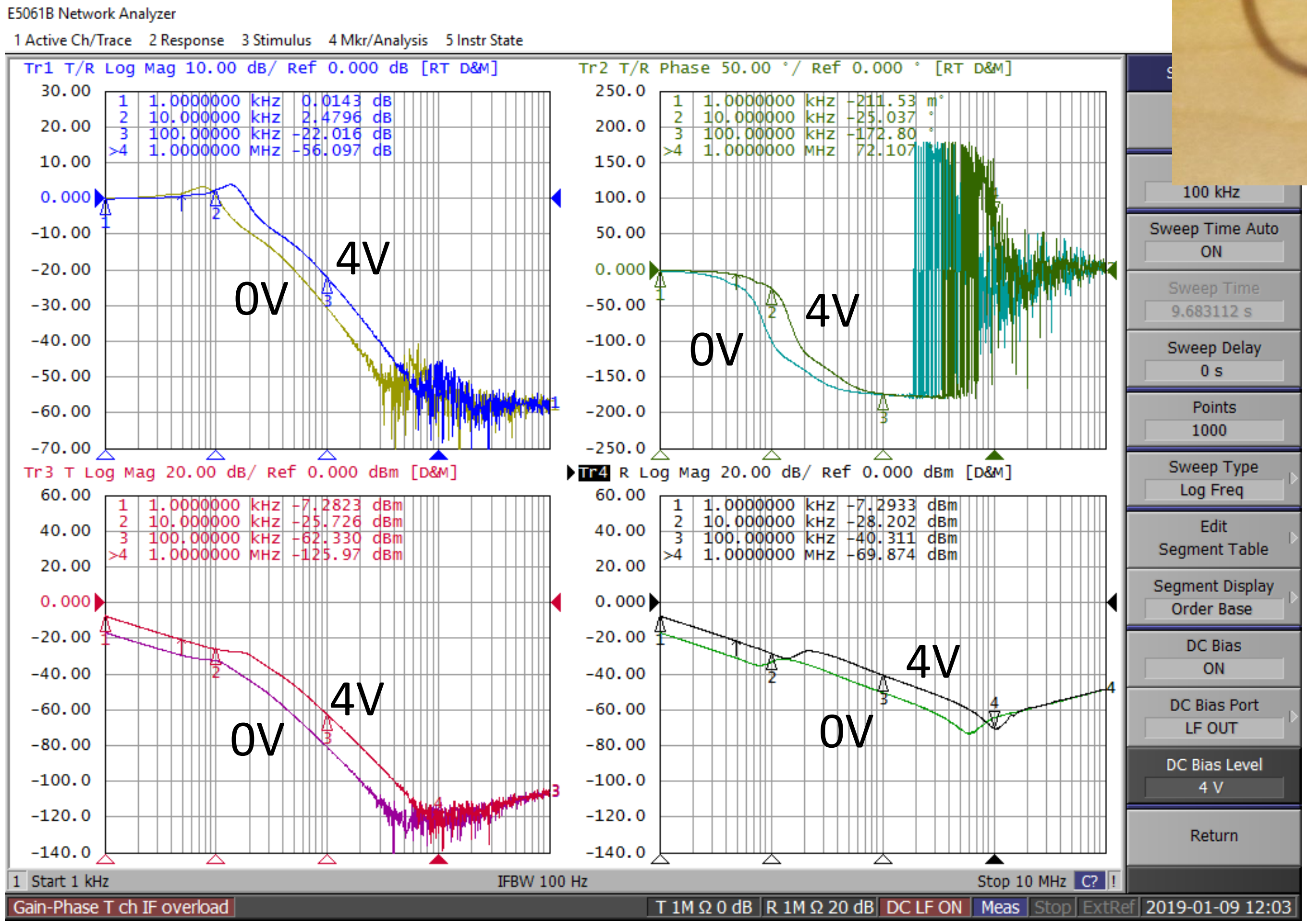
E5061B Gain-Phase Results

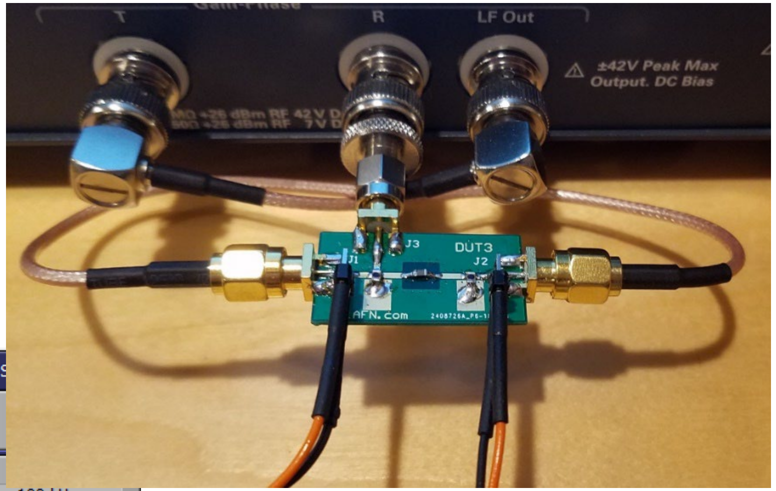




E5061B
0dBm source
0 and 10V DC bias
0A current bias

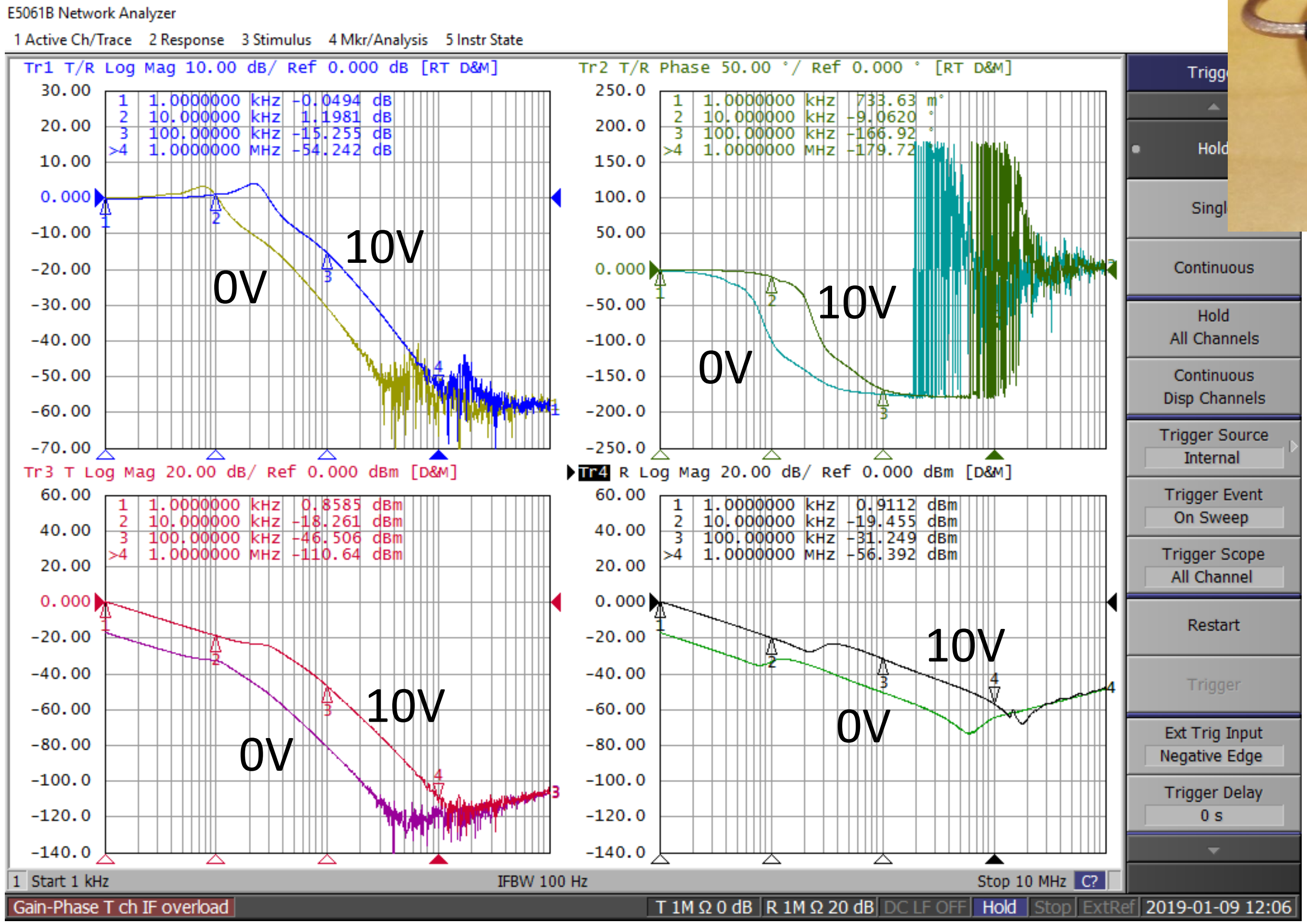
E5061B Gain-Phase Results

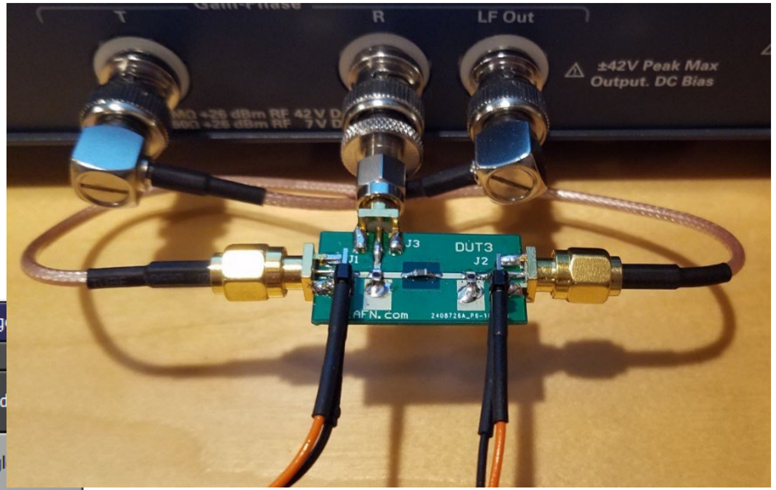




E5061B
10dBm source
0 and 4V DC bias
0A current bias

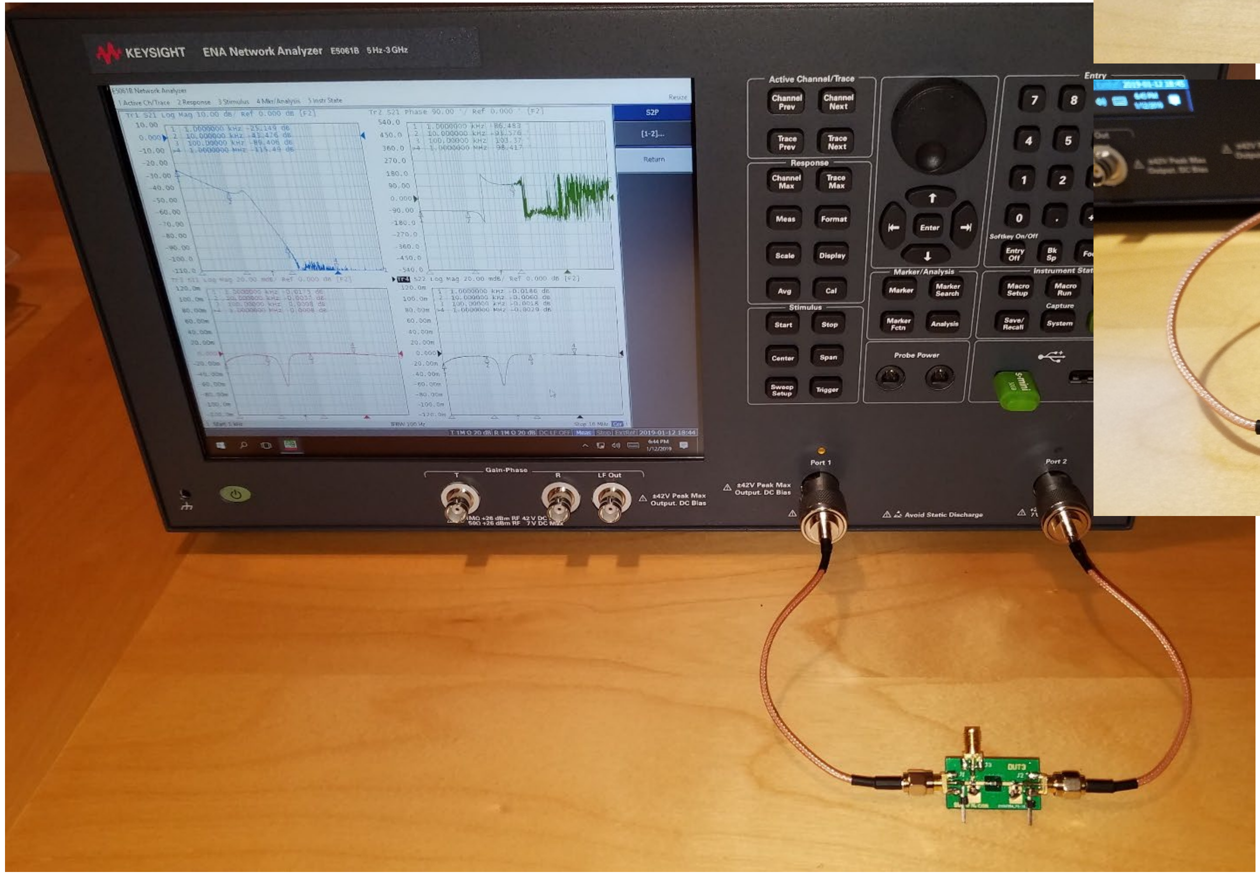
E5061B Gain-Phase Results

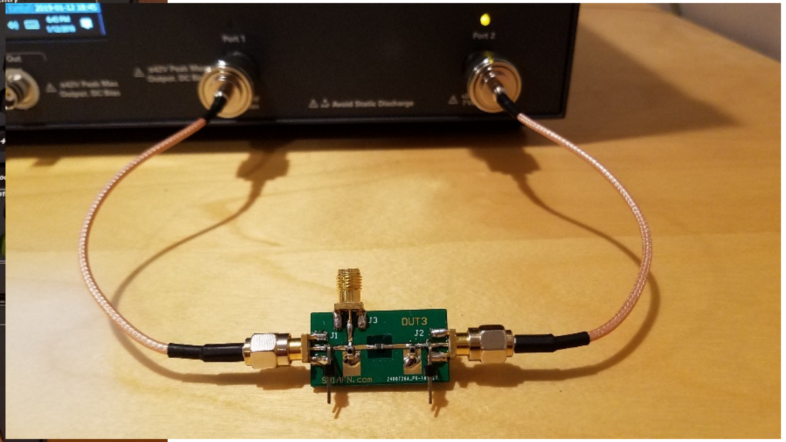




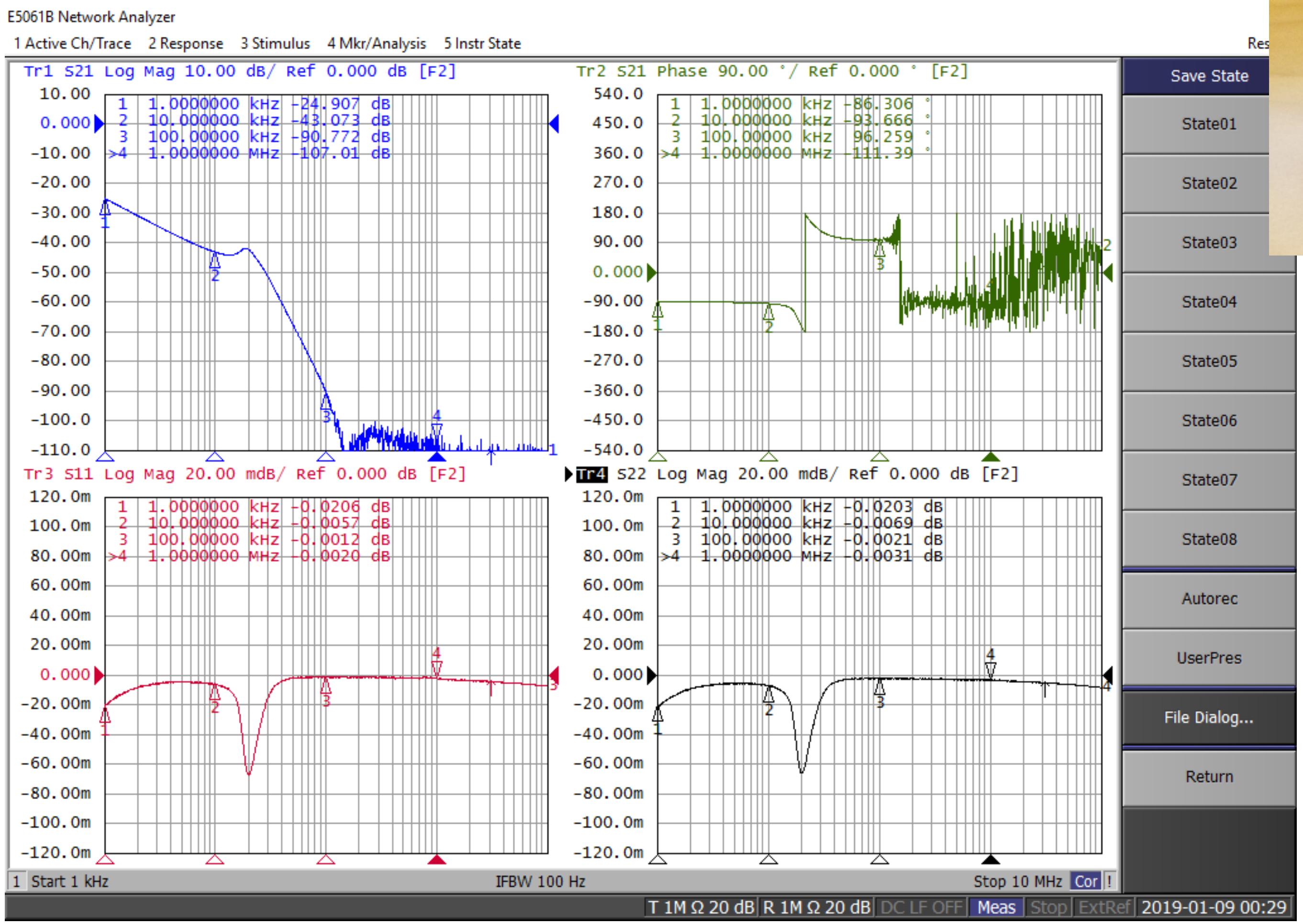
E5061B
10dBm source
0 and 10V DC bias
0A current bias

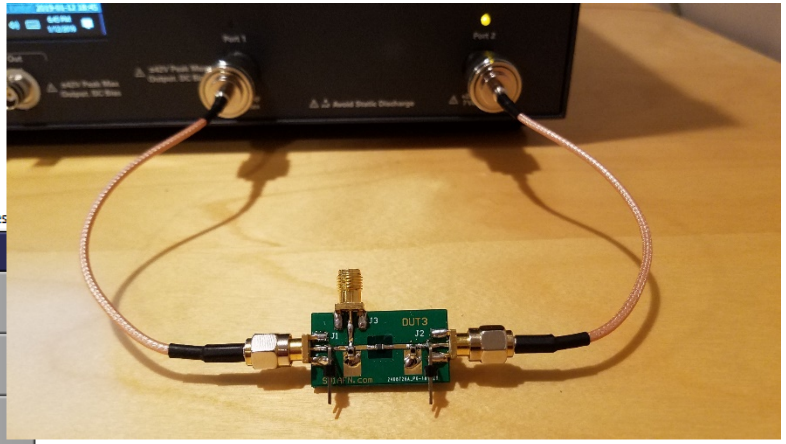
E5061B S-parameter Setup





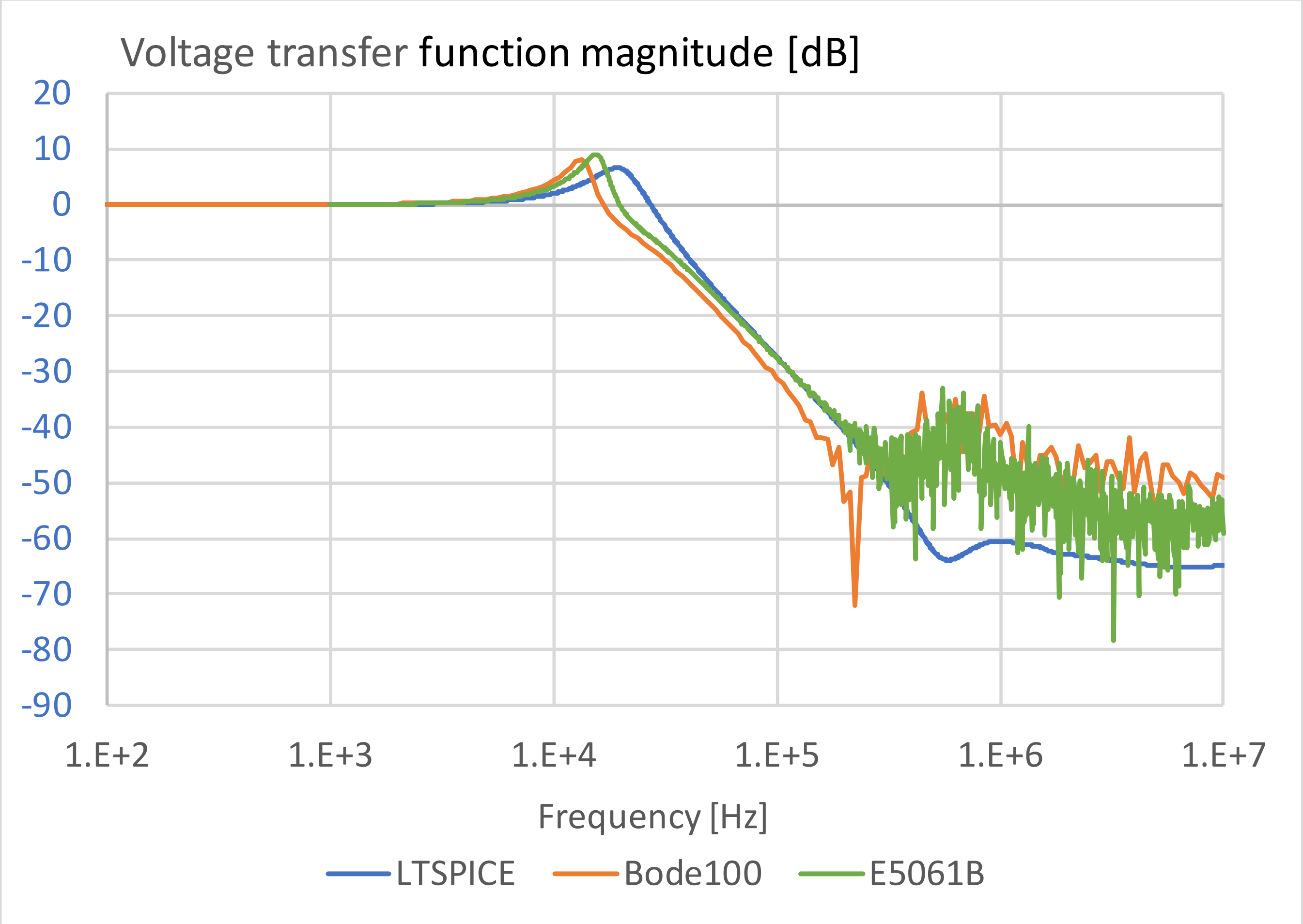
E5061B S-parameter Results





E5061B
0dBm source
No bias

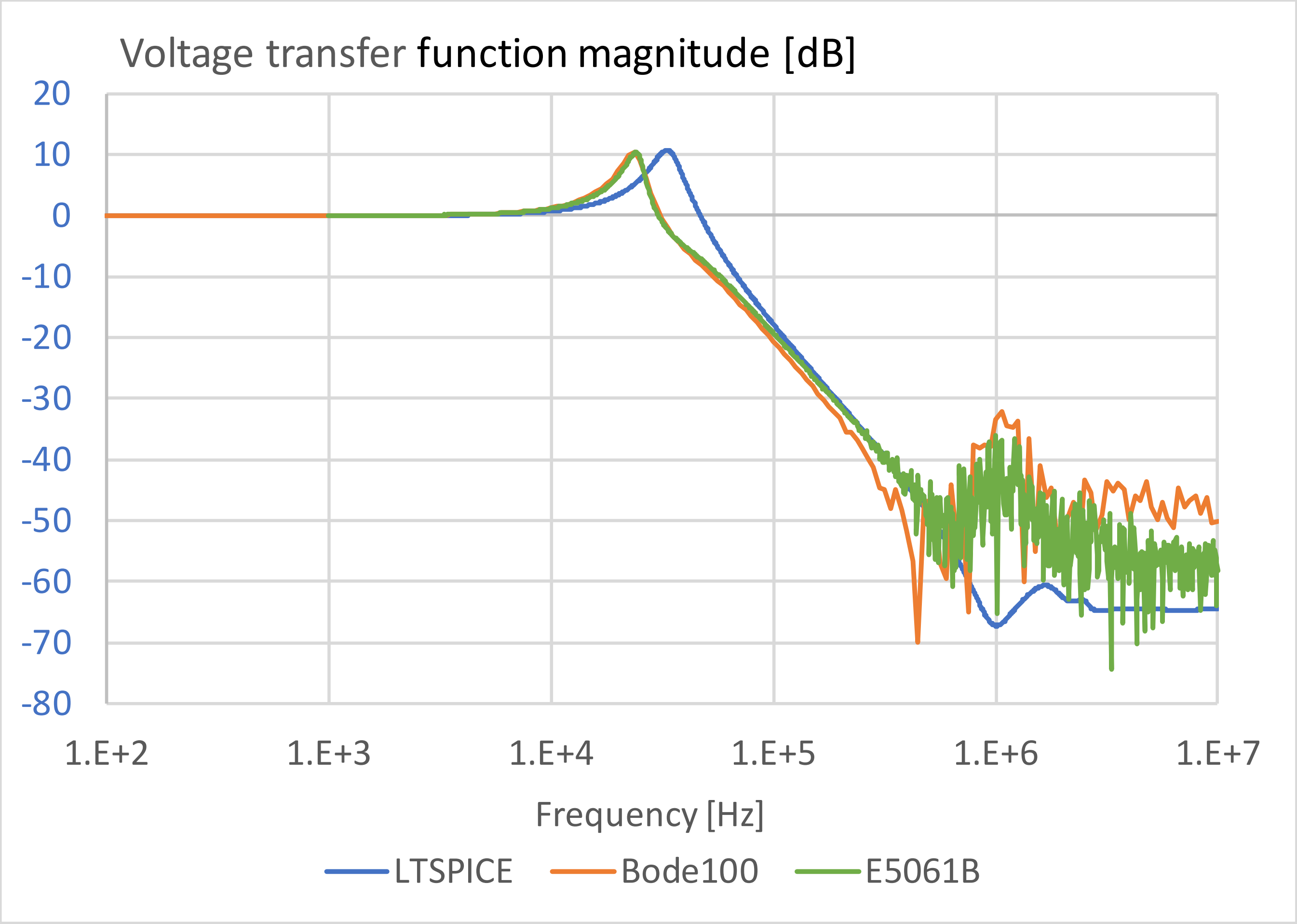
Correlation with No Bias



0dBm source

- LTSPICE
- Bode100
- E5061B GP side

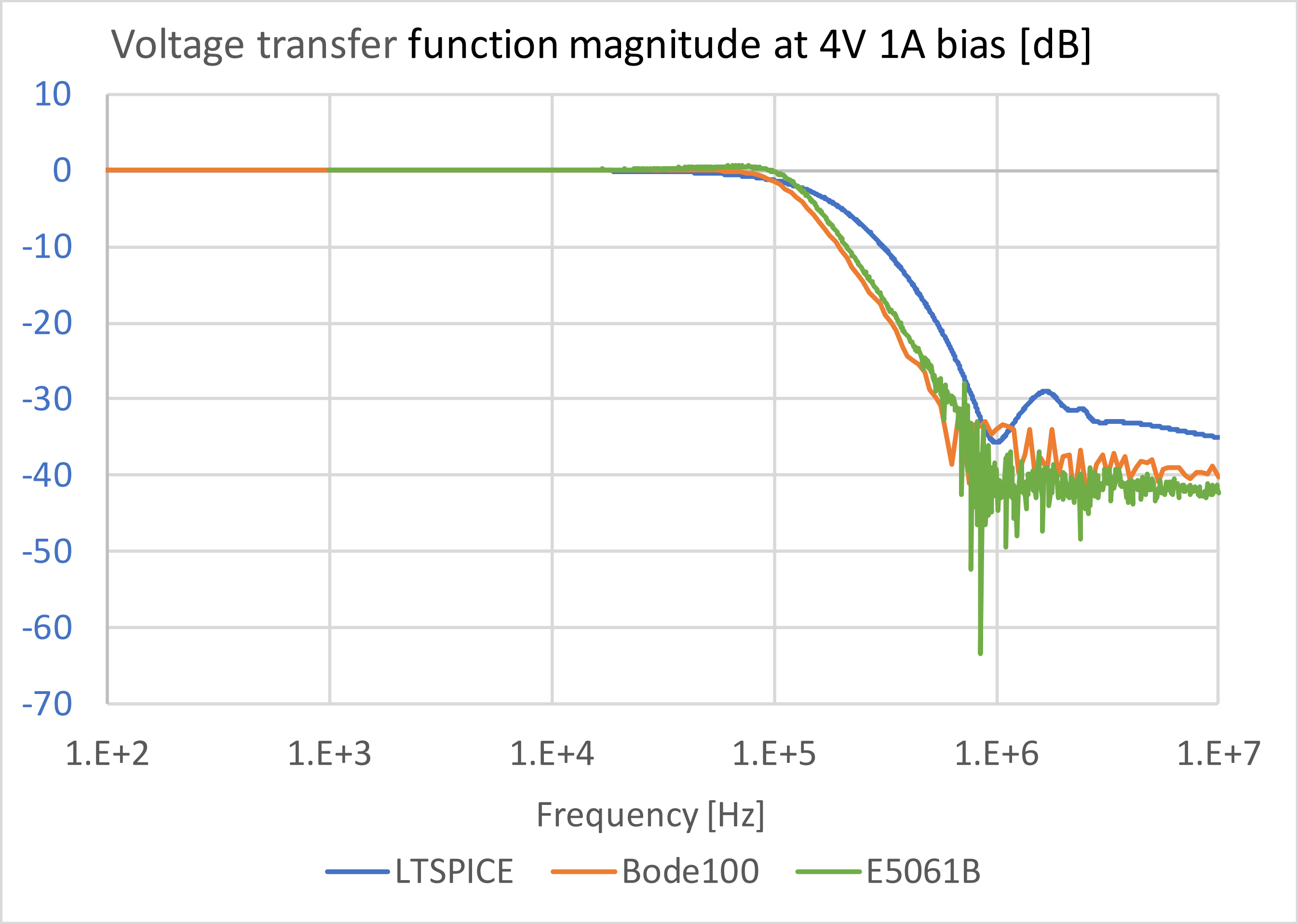
Correlation with Voltage Bias



0dBm source

- LTSPICE
- Bode100
- E5061B GP side

Correlation with Voltage and Current Bias



0dBm source

- LTSPICE
- Bode100
- E5061B GP side

Acknowledgement and Resources

Special thanks to

- Keysight and Picotest for providing demo equipment
  - https://literature.cdn.keysight.com/litweb/pdf/5990-4392EN.pdf
  - https://www.picotest.com/products_BODE100.html
- Murata for assisting with dynamic models and samples
  - https://www.murata.com/en-us/tool

- Simulations were done with Analog Devices' free LTSPICE
- Filter evaluation boards
  - https://www.sv1afn.com/rf-experimenter-s-pcb-panel.html

This presentation is based on the following training course materials

https://www.cei.se/course-056-power-integrity-advanced-design-and-characterization-group.html

https://www.cei.se/course-055-signal-integrity-advanced-high-speed-design-and-characterization-group.html

https://www.conted.ox.ac.uk/courses/making-successful-power-distribution-designs

THANK YOU!

Any Questions?