2025 IEEE INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILITY, SIGNAL & POWER INTEGRITY

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Removing Communication Barriers Between CAD and Instrumentation Companies with Open Source PCB

Ken Willis, Cadence

Abstract and Speaker Bio

As power integrity (PI) analysis evolves to address microohm-level impedance challenges, the gap between simulation and measurement accuracy has widened due to complex 3D interactions and the absence of standardized reference platforms. This paper presents an open-source PCB that can be used as a reference board, designed to bridge communication barriers between end users, CAD software developers and instrumentation manufacturers. The board's simplicity, reproducibility, and confidentiality-free design enable consistent benchmarking and correlation studies across tools and organizations. The proposed platform incorporates a variety of via structures and connectivity options, facilitating detailed investigations into solver accuracy, probe coupling, and port definition effects. Full-wave 3D simulations and empirical measurements demonstrate the impact of probe orientation and de-embedding on microohm impedance characterization. By providing a shared, open hardware foundation, this initiative fosters collaborative development, enhances model validation, and supports the advancement of PI validation methodologies.

Ken Willis

AE Group Director, Cadence Design Systems

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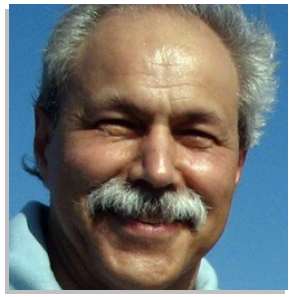
Ken Willis is an Application Engineering Group Director focusing on SI solutions at Cadence Design Systems. He has over 25 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, technical marketing, and management positions with the Tyco Printed Circuit Group, CompaqComputers, Sirocco Systems, Sycamore Networks, and Sigrity.

Co-authors



Istvan Novak

Principal SI/PI Engineer, Samtec

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Istvan works on advanced SI/PI designs at Samtec and was previously a Distinguished Engineer at SUN later Oracle. He introduced the first 25µm power-ground laminates for large rigid PCBs and worked to create a series of low inductance, controlled-ESR capacitors. He is a Life Fellow of the IEEE with 25 patents, author of two books on PI, teaches SI/PI courses, and maintains a popular SI/PI website. He was named Engineer of the Year at DesignCon 2020.

Shirin Farrahi

Sr. Principal Software Engineer, Cadence

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Shirin Farrahi is working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

Kristoffer Skytte

Application Engineer Architect, Cadence

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Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. His recent efforts are on examining differences between measurement and simulation. He holds an M.Sc.EE. degree from the Technical University of Denmark.

John Phillips

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John has 30+ years experience working on SI, PI, and EMC challenges at the chip, board, and system level in applications including high-end computing and mil-aero. He holds an MSc. from Bolton University, UK. His current interests are SI/PI co-simulation and modelling for high-speed interfaces.

GUSTAVO BLANDO

Sr Signal and Power Integrity Manager, Amazon (AWS)

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Gustavo Blando is a Senior Signal and Power Integrity Leader and Engineer with nearly three decades of experience in high-speed digital systems and advanced signal and power integrity design. Since 1996, he has contributed to the development of complex electronic systems across a range of companies and technologies, and he currently leads advanced SI/PI efforts at Amazon's Annapurna Labs. Gustavo is a recognized authority in the field, having authored numerous technical papers and magazine articles. His work spans high-speed interconnects, simulation and measurement methodologies, and system-level design practices. He is deeply committed to advancing the state of the art and mentoring the next generation of engineers.

Mario Rotigni

Retired

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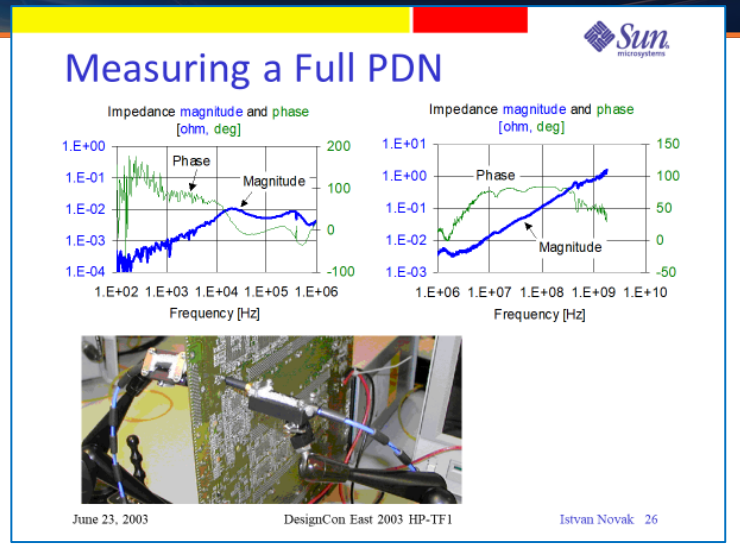
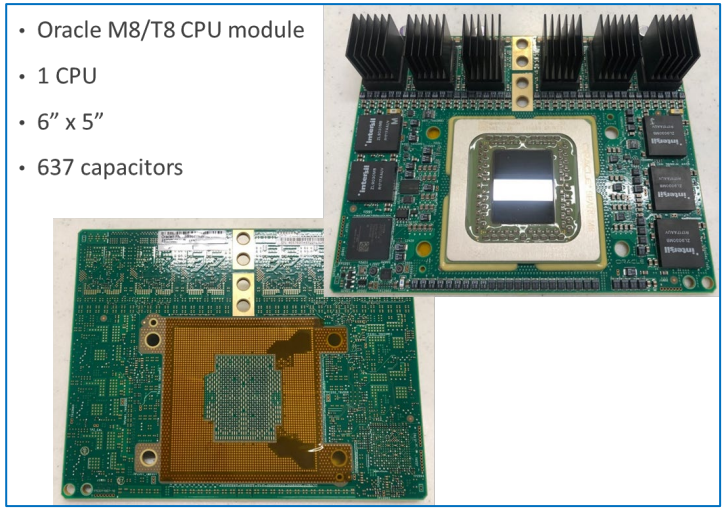
Mario retried after a 45-year career in R&D working on micro-controllers and EMC for automotive applications. He has co-authored 22 papers about EMC of Integrated Circuits and is a member of the IEEE & IEEE EMC Society.

Background, motivation

- Paradigm Shift #1: late 1990s
  - Requirements to measure milliohms
  - Frequency domain design and verification
  - Horizontal incremental impedance was relatively small
  - 3D interactions in PI measurements were small
  - **Solution: VNA with Two-port Shunt-through connection**
  - Frequency and time-domain verifications lined up
- Paradigm Shift #2: early 2020s
  - Requirements to measure microohms
  - 3D interactions in PI measurements become dominant
  - Horizontal incremental impedance becomes relatively high
  - Increasing gap between frequency and time-domain verification results
  - **Solution: ???**





From: Is Power Integrity the New Black Magic?
Cadence Design Forum, April 2021

From: Cadence Live Boston, September 12, 2023

Background, motivation

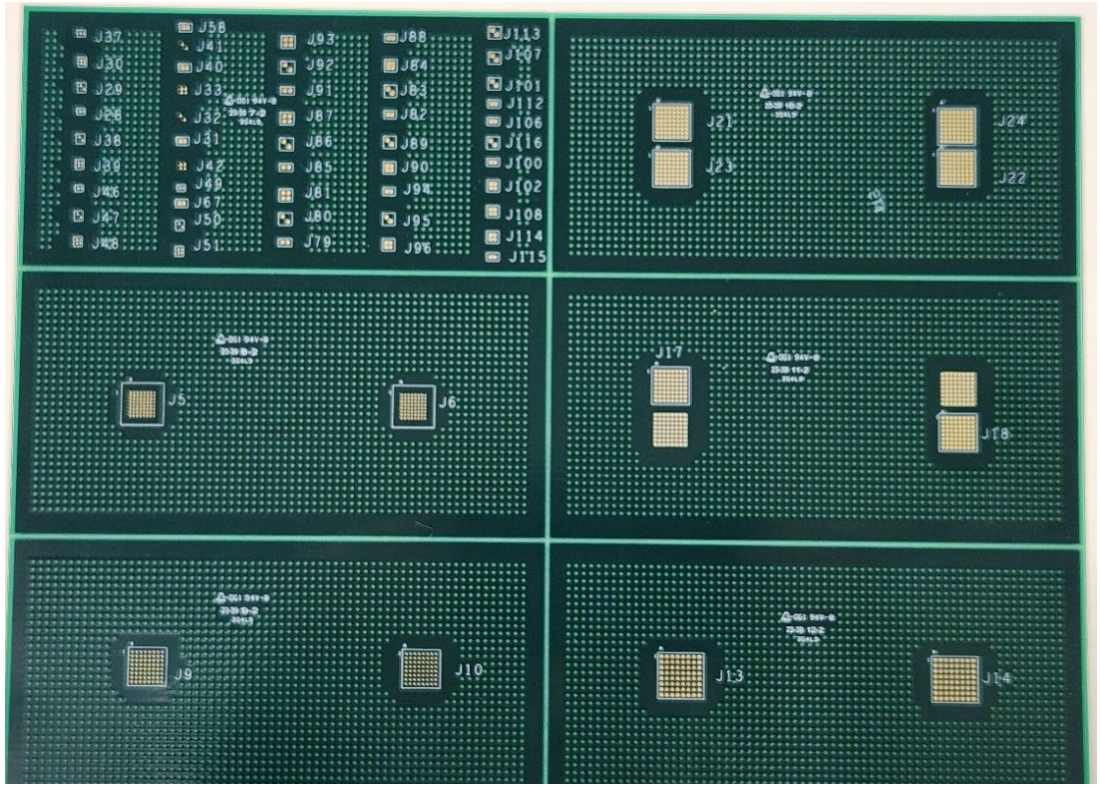
- Simulating and/or measuring microohm AC impedances is very challenging
- Correlation between measured and simulated data is hard
- When questions arise about accuracy of models, simulation or measurement results, resolution is hard because
  - the lack of a readily available reference platform
  - confidentiality concerns
- Simple easy-to reproduce reference platform is needed that anyone can make, measure and simulate
- Solution: open-source PCB reference structures

How open source PCB can help

- Open-source HW reference piece removes confidentiality barriers
  - CAD companies can refine their SW and share their simulation results without revealing confidential details
  - Instrumentation manufacturers can improve their HW and suggested test procedures without revealing confidential details
  - Known HW (either the same piece or nominally identical replica) can be used for round-robin studies
- All parties involved can refer to the same structure

Open source PI board

- Goals
  - Simple stackup and construction
    - Allows various laminates and copper weight
  - No special material
  - No special technology
  - Mix of plated through holes and blind vias
  - Simplest possible structures to analyze
  - Include via arrays
  - Include reference pieces
  - Any assembly is optional



Nominal stack-up and materials

APCT Passion | Commitment | Trust

STACKUP & IMPEDANCE REPORT

DFM Engineer: John Macanas

Job Name: **53929**
Customer : **SAMTEC INC**
Part Name: **PCB-112938-SIG-XX**
Rev: **00**

Customer Required Finished Thickness: **63.000 (± 6.300) mils**
Estimated Finished Thickness: **62.656 mils (Over mask on plated copper)**
Estimated Over Lam Thickness: **58.456 mils**

Lyr	Vendor	Image
CM		0.700 mils
L1	Oak Mitsui	2.000 mils [redacted] SIG Base Cu: 0.50 oz 0.600 mils HTE 10%
	EMC	3.064 mils Dk: 3.80 EM-827 1080 (65.0%)
L2		1.200 mils [redacted] P/G Base Cu: 1.00 oz RTF 97%
	EMC	3.000 mils Dk: 3.83 EM-827 (1-1080)
L3		1.200 mils [redacted] P/G Base Cu: 1.00 oz RTF 97%
	EMC	6.164 mils Dk: 3.80 EM-827 1080 (65.0%)
	EMC	Dk: 3.80 EM-827 1080 (65.0%)
	EMC	28.000 mils Dk: 4.40 EM-827 (4-7628) FILLER CORE
	EMC	6.164 mils Dk: 3.80 EM-827 1080 (65.0%)
	EMC	Dk: 3.80 EM-827 1080 (65.0%)
L4		1.200 mils [redacted] P/G Base Cu: 1.00 oz RTF 97%
	EMC	3.000 mils Dk: 3.83 EM-827 (1-1080)
L5		1.200 mils [redacted] P/G Base Cu: 1.00 oz RTF 97%
	EMC	3.064 mils Dk: 3.80 EM-827 1080 (65.0%)
L6	Oak Mitsui	2.000 mils [redacted] SIG Base Cu: 0.50 oz 0.600 mils HTE 10%
SM		0.700 mils

DRILL TABLE

Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Stacked Via	Min Drill Size (mils)	Drill Depth (mils)	Pad Size (mils)	Hole Qnty	Do Not Hit Layer	Related Process
1	6	Mechanical	PTH	----	----	0.000	58.5	0.000	0	----	Final Assembly - 1/6
1	2	Laser	Micro Via	Copper Fill	No	6.000	3.7	0.000	0	----	Final Assembly - 1/6
6	5	Laser	Micro Via	Copper Fill	No	6.000	3.7	0.000	0	----	Final Assembly - 1/6
1	3	Laser	Micro Via	Copper Fill	No	10.000	7.9	0.000	0	----	Final Assembly - 1/6
6	4	Laser	Micro Via	Copper Fill	No	10.000	7.9	0.000	0	----	Final Assembly - 1/6

	Plating Type	Panel Size	Grain Direction
Final Assembly - 1/6	**Pattern Plate**	**18 x 24**	**18**

EMC Elite Material Co., Ltd. Technical Data
http:\\www.emctw.com

High Tg / Low CTE / Lead Free
EM-827 / EM-827B

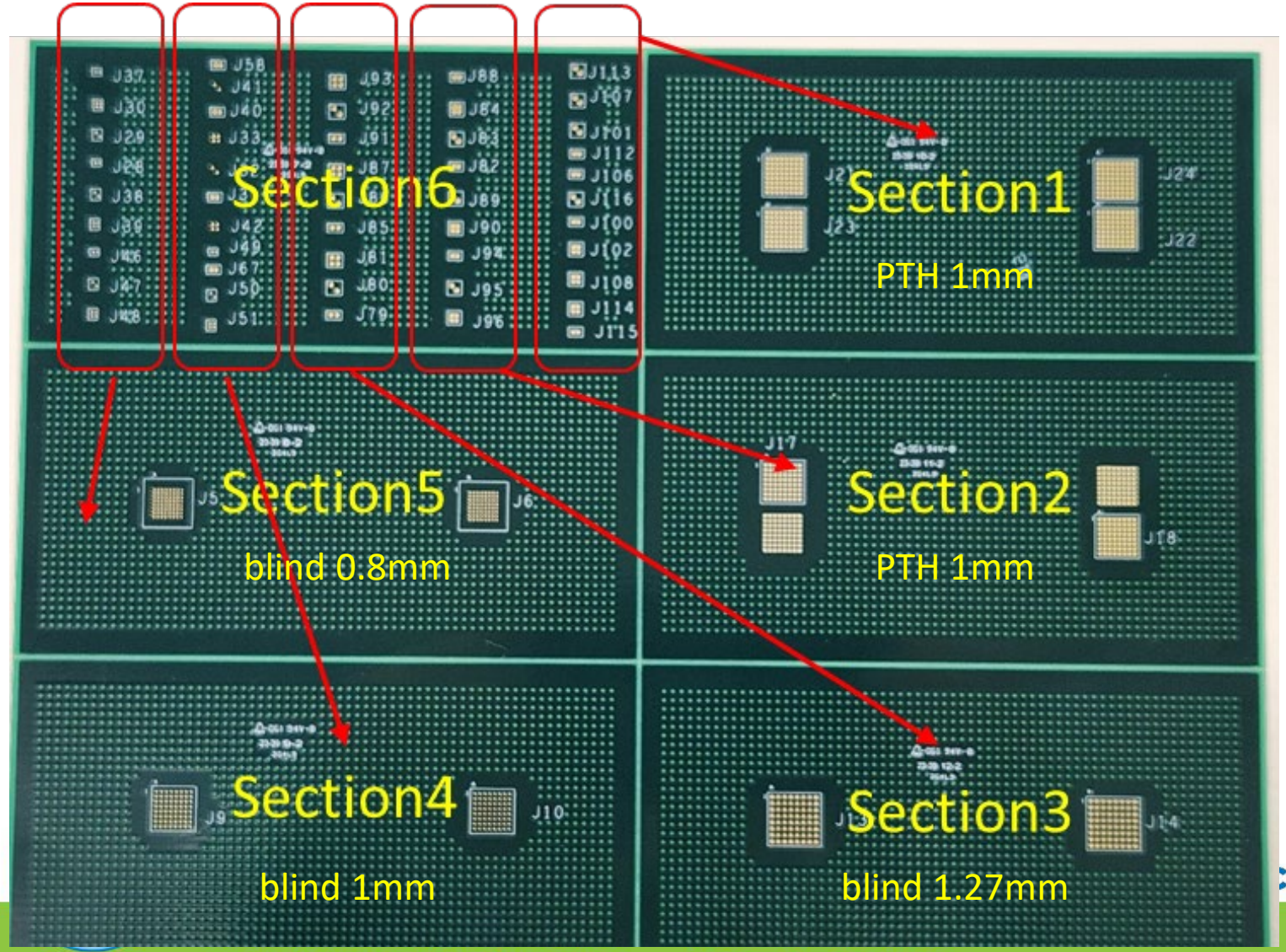
- Low Z-axis CTE < 3.0% (50~260℃)
- Excellent thermal stability for lead-free processing
- For general application

Basic Laminate Property

Property	Item		IPC-TM-650	Test Condition	Unit	Typical Value
Thermal	Tg		2.4.25	DSC	℃	175
			2.4.24	TMA	℃	160
			2.4.24.4	DMA	℃	185
	CTE, X/Y-axis		2.4.24.5	< Tg, TMA	ppm/℃	12/15
	CTE, Z-axis		2.4.24	< Tg, TMA	ppm/℃	45
				> Tg, TMA	ppm/℃	225
	Z-axis Expansion		2.4.24	50~260℃	%	2.6
	Td		2.4.24.6	TGA (5% W.L)	℃	350
	T288		2.4.24.1	Clad	Min.	20
				Etched	Min.	>30
Electrical	Dk (R/C: 50%)	1 MHz	2.5.5.9	C-24/23/50	-	4.8
		1 GHz			-	4.2
	Df (R/C: 50%)	1 MHz	2.5.5.9	C-24/23/50	-	0.018
		1 GHz			-	0.019
	Volume Resistivity		2.5.17.1	C-96/35/90	MΩ-cm	$>10^{10}$
	Surface Resistivity		2.5.17.1	C-96/35/90	MΩ	$>10^{9}$
Physical	Water Absorption		2.6.2.1	E-1/105+D-24/23	%	0.12
	Peel Strength (HTE)	0.5 oz	2.4.8	As Received	lb/in	6.5
				After Thermal Stress	lb/in	6.5
		1.0 oz	2.4.8	As Received	lb/in	8.5
				After Thermal Stress	lb/in	8.5
	Flexural Strength	Warp	2.4.4	As Received	MPa	460~500
		Fill		As Received	MPa	390~430
	Flame Resistance		UL-94	A & E-24/125	-	V-0

Rev: 2017 Aug.

Layout blocks



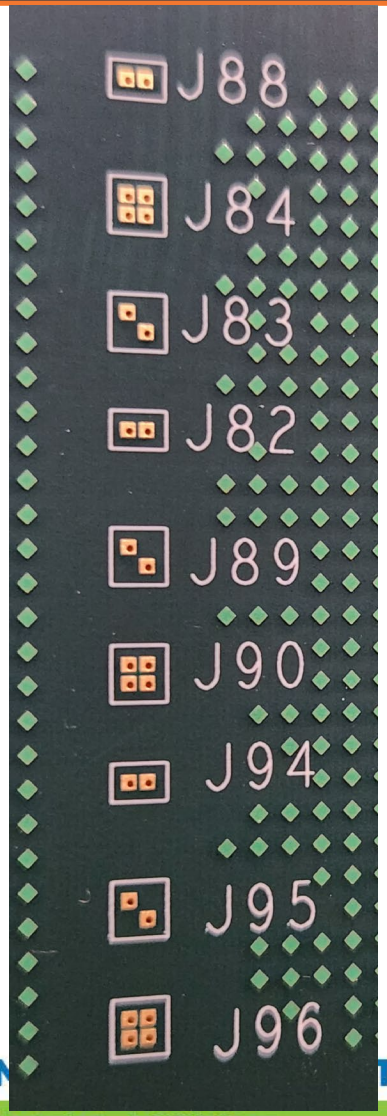
Overall board outline: 10” x 7.5”

- Sections 1&2: PTH arrays, 1mm pitch
- Section 3: blind via arrays, 1.27mm pitch
- Section 4: blind via arrays, 1mm pitch
- Section 5: blind via arrays, 0.8mm pitch
- Section 6: reference pieces for Sections 1 - 5

Reference block, column 5

All plated through holes

1mm grid



J88: both vias (straight) land on L3

J84: all four vias land on L2

J83: both vias (diagonal) land on L2

J82: both vias (straight) land on L2

J89: both vias (diagonal) land on L3

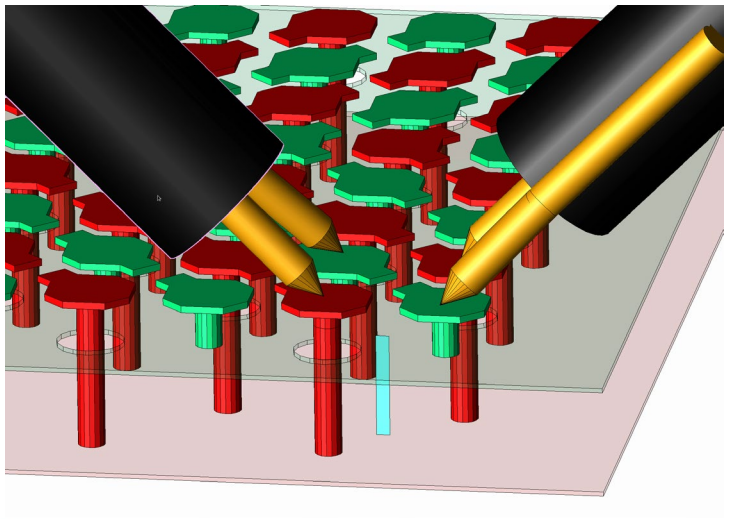
J90: all four vias land on L3

J94: straight pair landing on L2 and L3

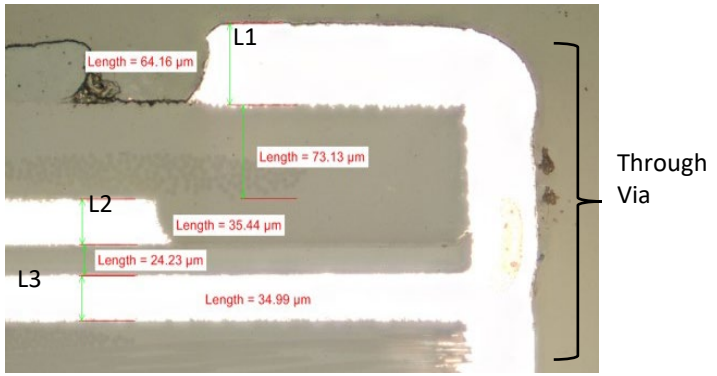
J95: diagonal pair landing on L2 and L3

J96: checker-board quad landing on L2 and L3

Reference block, j84

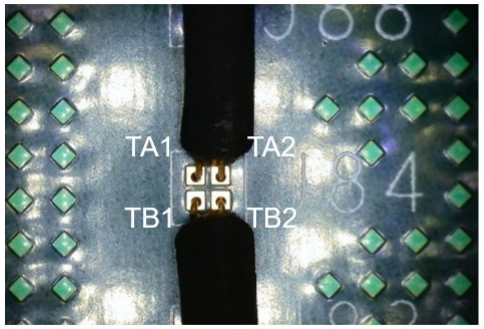


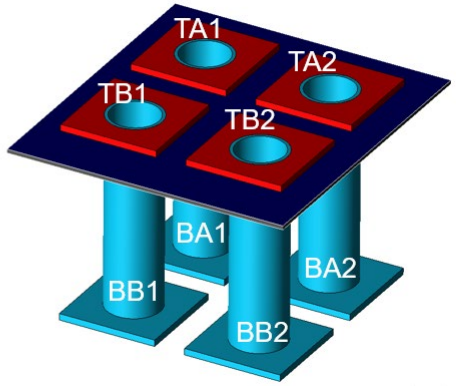
- Four plated through holes
- Building block of larger arrays
- 1mm square pitch
- Checker-board pattern (though it does not matter)
- All four vias connect to L2
- Multitude of connection options

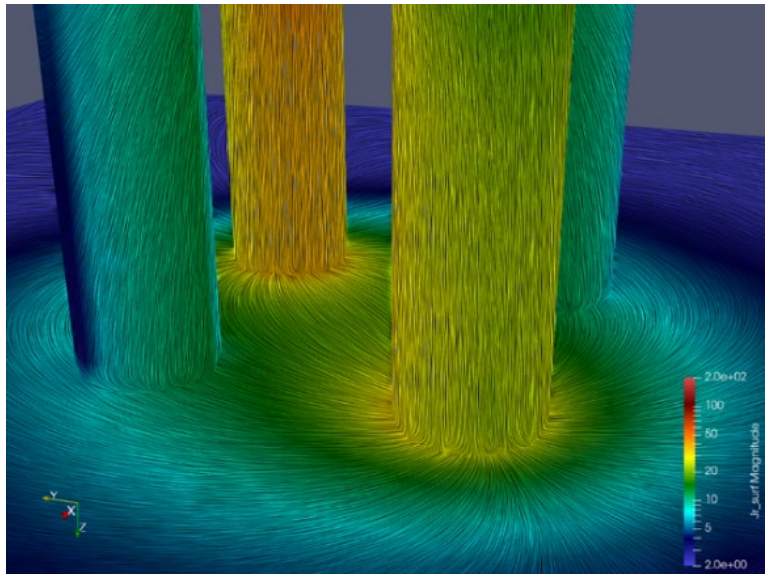


Visualizing low impedances

- Full FEM 3D simulations show the complexities involved in measuring a simple plane short impedance
  - Practical restrictions mean measurements must often be taken on one side
  - Current spreads to neighboring vias
  - Via barrels add magnetic coupling







Current density distribution at 1MHz during diagonal resistance measurement using Clarity3D ®

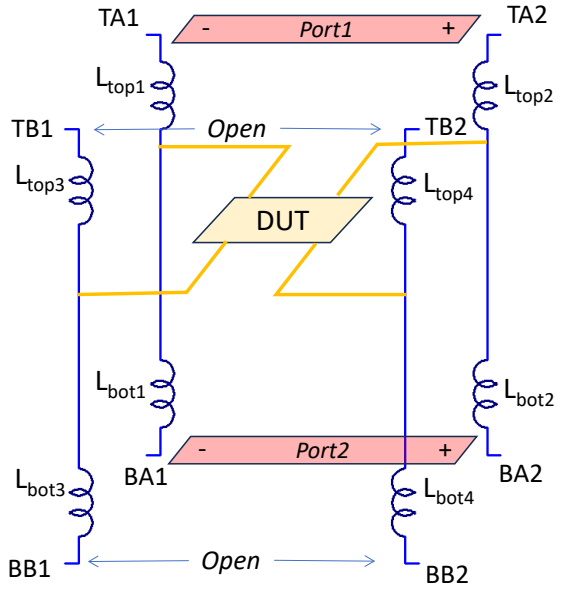
From: “Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization,” DesignCon 2024

Connections, Z definitions

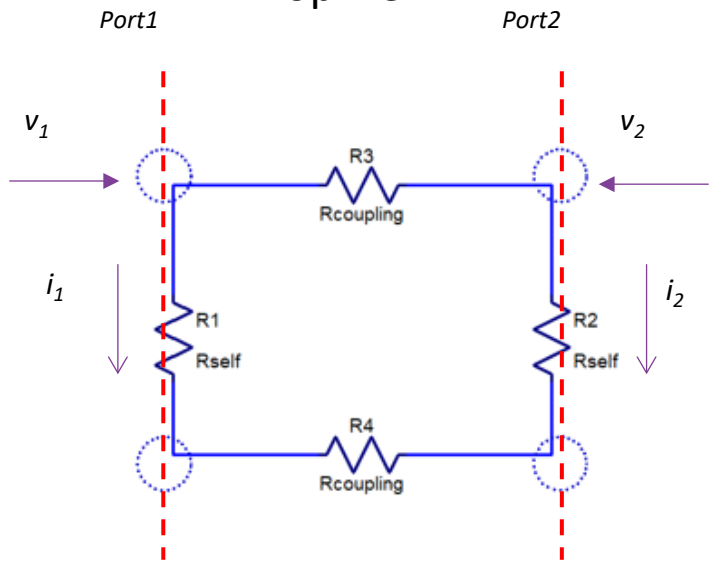
- Impedance can be calculated from the S matrix
- **With two power-ground via pairs, there are multiple options to approximate impedance**
  - TOP-DOWN data along one via captures the DUT impedance closely
    - No loop coupling, no spatial attenuation
  - DUT impedance can be approximated from S21
- **The s-to-z transformation uses all four S parameters**
  - Reflection terms are very inaccurate for large reflections
  - For many PDN impedances $|s_{ii}| \sim 1$

$$\begin{bmatrix} Z_{11n} & Z_{12n} \\ Z_{21n} & Z_{22n} \end{bmatrix} = \begin{bmatrix} \frac{2\Delta_1 S_{11} + S_{12}S_{21}}{4} & \frac{S_{12}}{2} \\ \frac{S_{21}}{2} & \frac{2\Delta_2 S_{22} + S_{12}S_{21}}{4} \end{bmatrix}$$

3D view:



Top view:

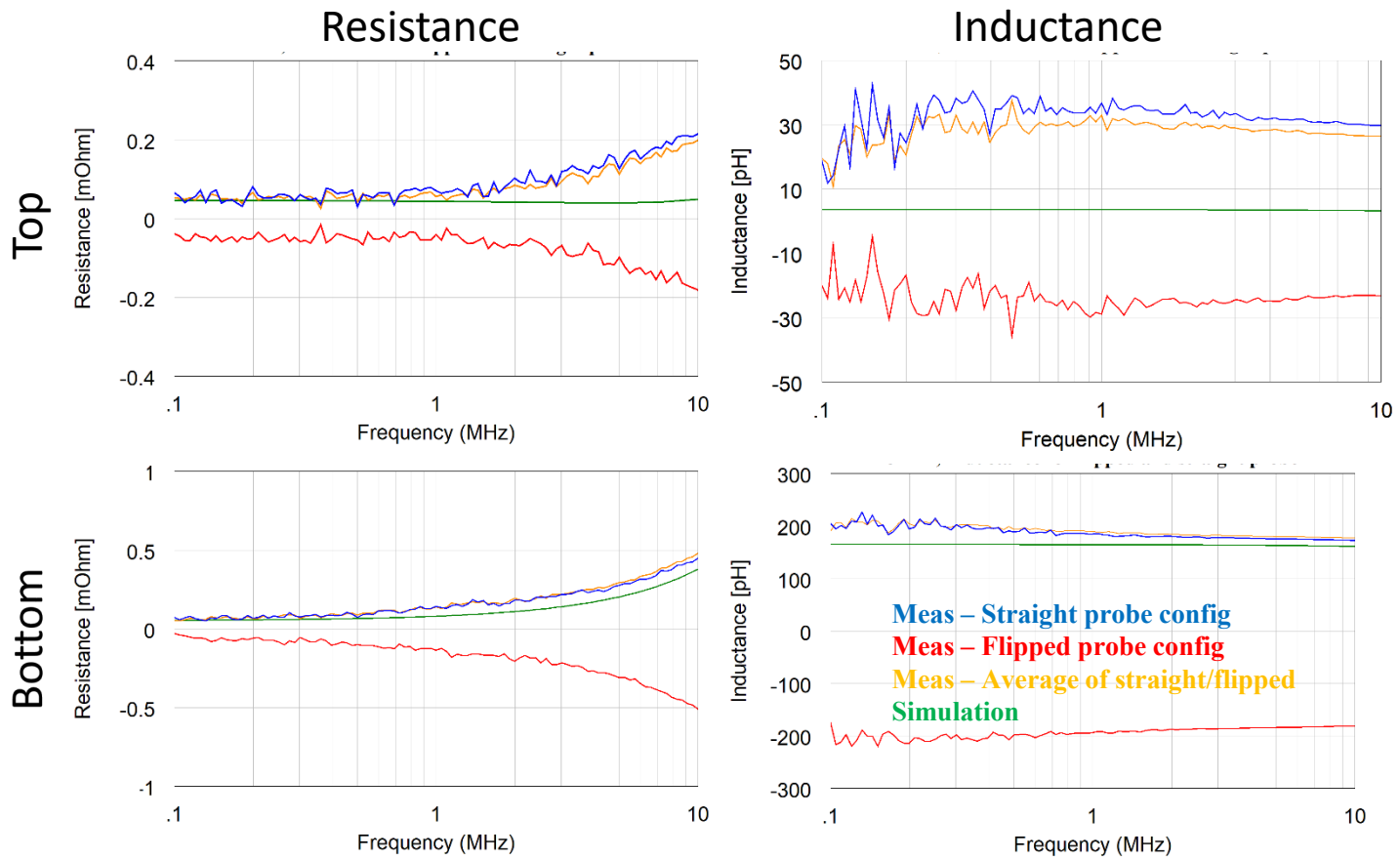


"Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization," DesignCon 2024

Correlations

- Probe orientation matters
  - Average of straight and flipped configuration cancels probe-tip coupling
- Simulation to measurement
  - Average of straight and flipped measured values correlate well
  - Top side probing (short via)
    - Resistance in good agreement to 3 mhz – short via section is masked by probe coupling
    - Measurement series inductance and coupling > inductance being measured. Indications that probe contributes around 30-35ph
  - Bottom side probing (long via)
    - *Good agreement between simulation and measurement. ΔL 35ph – probe coupling may add or subtract from measured DUT impedance*

Probes are not de-embedded



"Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization," DesignCon 2024

Summary, Conclusions

- We have shown a versatile open-source PI reference board
- Simple, easy to reproduce
- Offers multiple PI connectivity options
- Challenges to study
  - Impact of solver choice on accuracy
  - Port definitions
  - Probe coupling (size, position, orientation of probe loops)
  - Probe de-embedding, including probe-to-probe crosstalk

THANK YOU

The authors also wish to thank PacketMicro and DuPont for their material support to the project

QUESTIONS?

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References

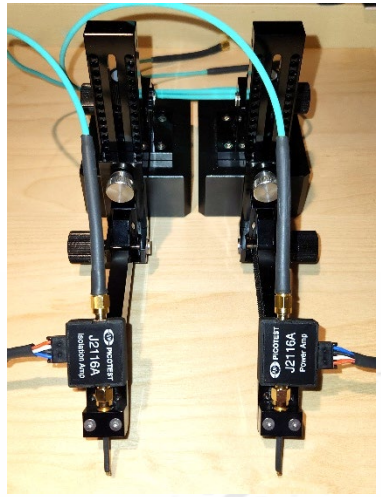
- http://packaging-benchmarks.org/
- https://www.samtec.com/standards/ieee/

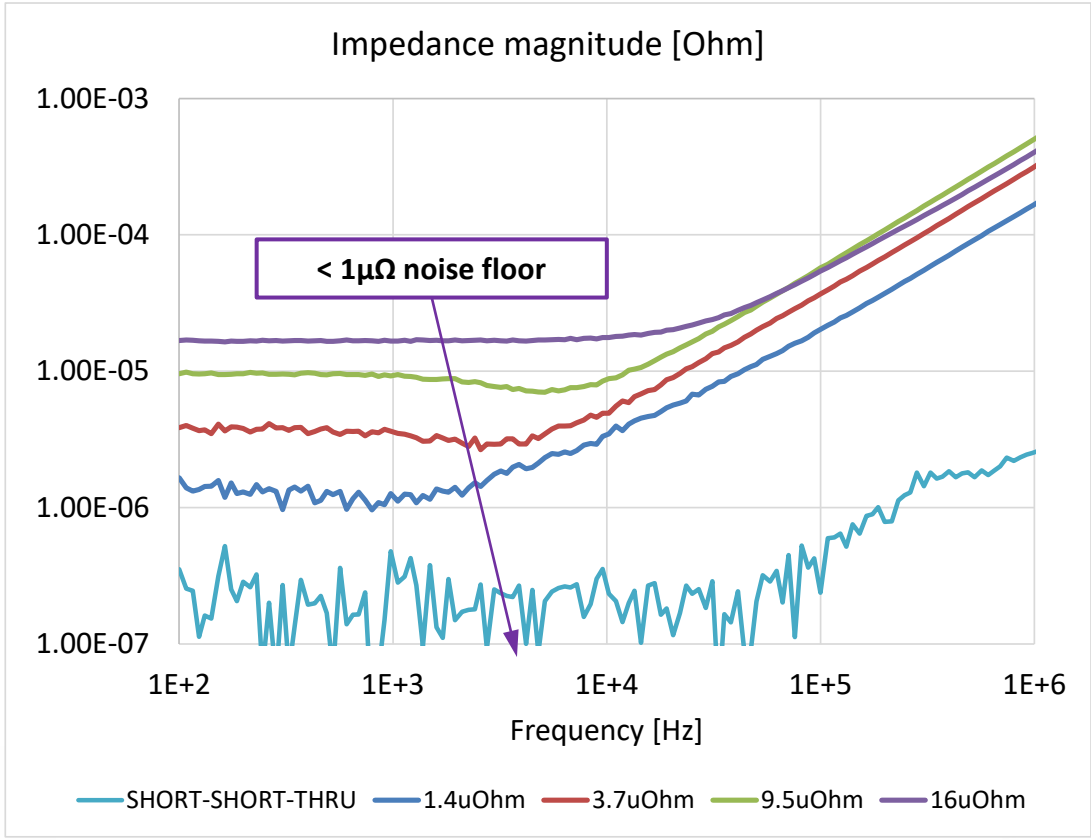
The open-source HW CAD package:

- https://www.samtec.com/tc-edms-benchmark

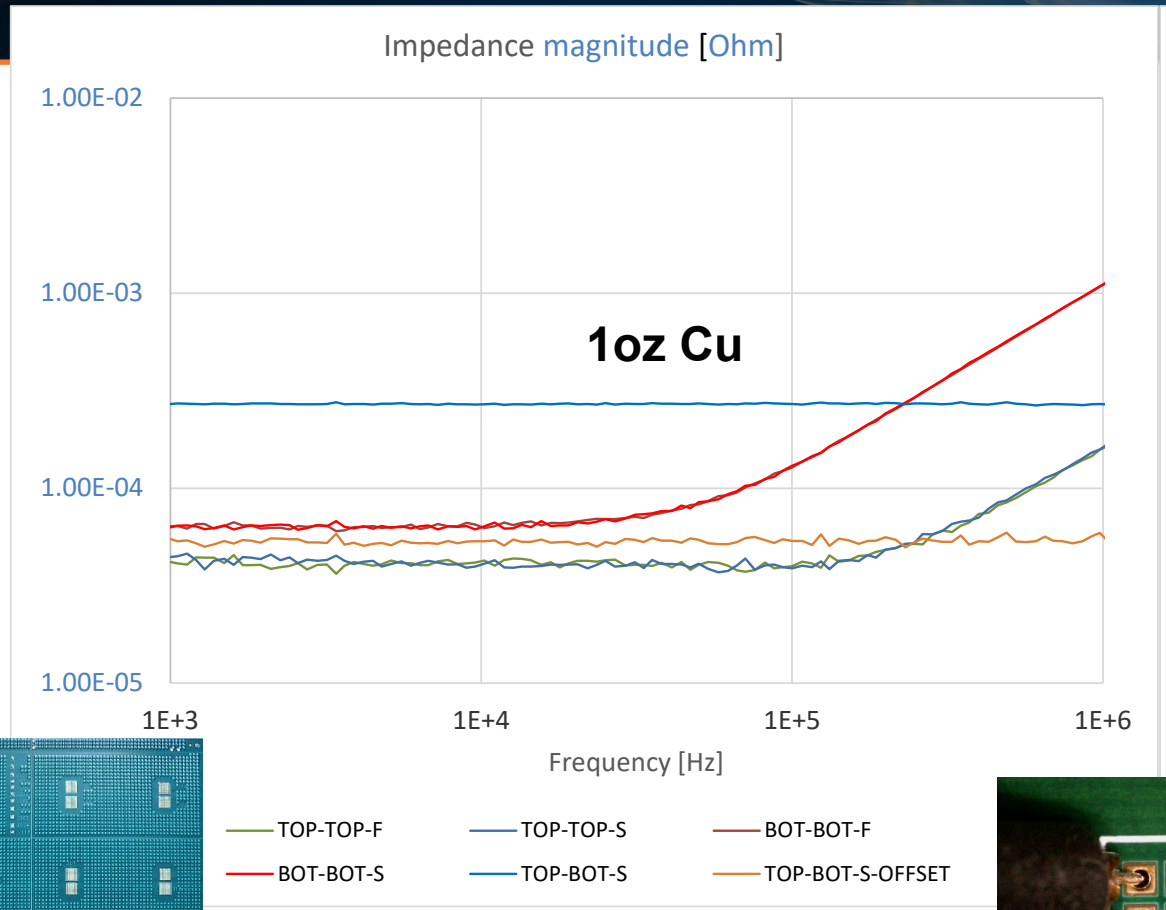
Noise Floor Investigation

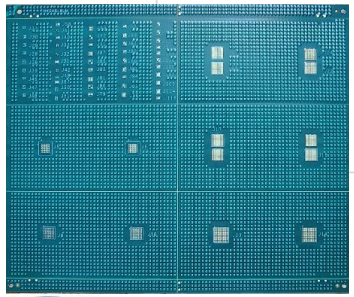
- 1Hz IFBW
- 0dBm source power
- No averaging
- SOLT calibration (including Isolation)
- 20dB 20dBm power booster on Port1
- 20dB low-noise pre-amplifier on Port2



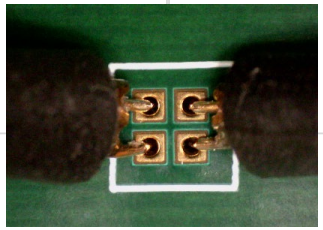


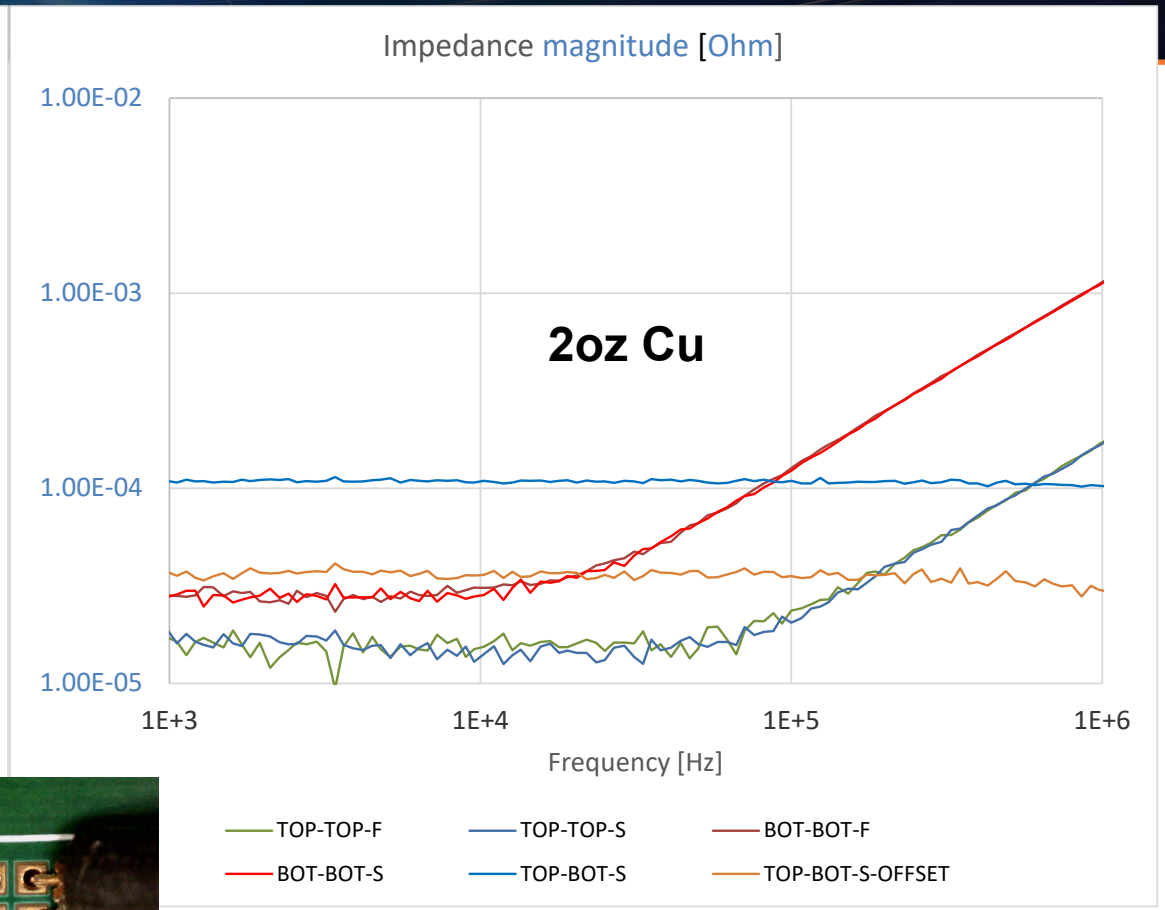
1oz vs. 2oz Copper





Board with 1oz 3-mil FR4 laminate
Boards courtesy of PacketMicro





Board with 2oz 8um HK04 laminate
Boards courtesy of DuPont