

Towards Developing a Standard for Data Input/Output Format for PDN Modeling & Simulation Tools

Ravi Kaw, Agilent Technologies, Inc.
5301 Stevens Creek Blvd, Santa Clara, CA 95051
Phone: (408) 345-8893, Fax: (408)345-8088
email: ravi_kaw@agilent.com

Istvan Novak, Sun Microsystems, Inc.
One Network Drive, Burlington, MA 01803

Phone: (781)442-0340, Fax: (781)442-0402
email: istvan.novak@sun.com

Madhawan Swaminathan
Georgia Institute of Technology, GA 30332
Phone: (404)894-3340; Fax: (404)894-9959;
email: madhawan.swaminathan@ece.gatech.edu

Abstract - This paper explores the design and verification environment of Power Delivery Networks (PDN) in an attempt to point out areas for improving the tools and the methods. It also points out potential interfaces between PDN tools that can be standardized so that the models can be ported between various available tools.

1. INTRODUCTION

Power Delivery Network design is a system level problem that includes elements of the system board, IC packages, and the ICs housed within those packages. In general, there are three basic requirements for PDNs that designers need to consider, either by simulations or by measurements:

- a) the PDN has to deliver sufficiently clean supply to the ICs
- b) the PDN has to provide low-noise reference path for signals
- c) the PDN should not radiate excessively

In order to make sure that the PDN delivers clean supply to active devices, one can/should simulate the time-varying voltage across the supply rail, which requires the knowledge of the currents and the (frequency dependent) impedance profile of the PDN at all N points of interest: $v(t) = \mathbf{Z} * i(t)$, where $i(t)$ is the $1...N$ vector of excitation currents, $v(t)$ is the $1...N$ vector of the resulting noise voltages, and \mathbf{Z} is the $N \times N$ impedance matrix of the PDN. An illustration of a PDN is shown in Figure 1.

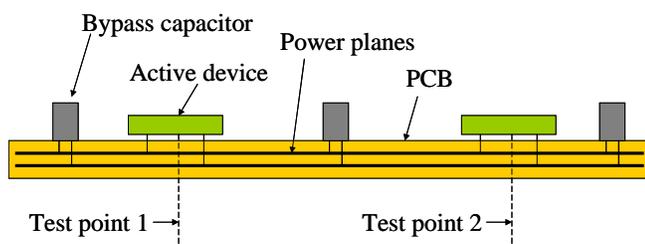


Figure 1: Sketch of a PDN with two test points, PCB, bypass capacitors and active devices.

One aspect of the PDN simulation is to determine the $i(t)$ current signature entering/exiting the PDN. Silicon designers may have the necessary information about the current signature, but for many silicon users, the current signature information is unavailable. This leaves the only possibility for silicon users to measure/simulate the impedance profile [1]

of the PDN, and complete the $v(t) = \mathbf{Z} * i(t)$ equation with assumed $i(t)$ equaling some percentage of watts/V [2], or stop short of calculating $v(t)$ altogether and just stay with the impedance profile. The user needs the impedance matrix (or any other network matrix) as a function of frequency, for a number of ports, representing the noise sources and other points of interest: bypass capacitors, test points.

The reference path for signals is not an inherent function of the PDN, but in many designs the PDN acts also as reference to one or more signals. The PDN may be of significant size in terms of wavelength of the highest frequency of interest, and therefore a full-wave solution may be necessary to obtain the noise. Here the user may want to simulate the impact of reference-layer transitions, reference-plane changes over split planes, SSN due to shared vias, due to finite plane resistance and inductance, including plane perforations [3].

As for radiation, the user again may be interested in the impedance profile of the PDN, to avoid resonances that may get excited by the signals or noise sources [4]. There are some differences between cases a) and c): common-mode currents that may not create SI problems may create excessive radiation. Also, point-of-load PDN structures tend to have a progressively band-limited filtering as we move away from the active device through the package and onto the board, so high-frequency noise appearing on the board may not find its way back to the silicon but it can create too much radiation from the board.

This design space includes an ever growing mix of modeling tools, simulation tools, methodologies of design, evaluation metrics, and formats for transferring data across interfaces. So the following discussion begins with a description of general elements of PDNs, and metrics for evaluating them. This is followed by a list of improvements required for modeling and simulation tools. A brief discussion is presented about the design methodologies used. This points to the lack of standards at the boundaries of silicon-package and package-board. The paper concludes with suggestions for such standards that can allow seamless exchange of design information across functional boundaries

2. PDN CLASSIFICATION

PDNs can be classified into two categories: Core PDN and IO PDN. The physical contents of Core PDN extend from the core switching networks and power/ground (P/G) grid that reside inside an integrated circuit, package P/G for core, core P/G network on PCB, and VRM (voltage regulation module). Sockets and bypass capacitors on chip, on package, and on PCB, also form parts of this network. Cores of large ASICs or CPUs may have dedicated Core PDN, feeding only one core; these are called Point-of-load circuits. In some designs, core P/G planes also act as reference planes for some of the signals, and therefore the return-path function of these PDNs must also be considered.

On the other hand, the IO-PDN generally includes signal delivery nets (SDN). Its physical contents extend from the chip-IOs (including their P/G), on-chip bypass caps for IOs, interconnections/redistributions, package and related PDN/SDN on the PC Board, and VRM. Sockets, connectors, and bypass caps at all stages are also included. Though not typical in today’s designs, IO-PDNs feeding only the ICs IO sections, without serving as signal reference, can also be constructed.

Finally, not only both classifications described above can be either pure PDN, or PDN+SDN, but there are PDNs, which combine all of these functions: the same PDN may feed core(s) and IO(s) and may also serve as signal reference path.

3. CORE PDN

Core PDN consists of various elements: (a) on-chip switching circuits whose details can be acquired from RTL information and test vectors provided by user; (b) location(s) or potential locations of on-chip bypass capacitors and their value if already designed in; (c) P/G grid (often provided in GDS format); (d) Package P/G structure and location(s) of bypass capacitors and their value if already designed; (e) PCB P/G structures supporting the core P/G, including bypassing schemes (locations and values); (f) VRM(s). Test points may also be included as separate nodes in each structure. An illustration of a possible physical realization is shown in Figure 2.

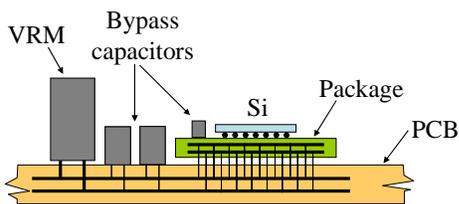


Figure 2. Illustration of a core point-of-load PDN.

On-chip switching activity depends on the circuit type and the logic vectors used. This core ‘current signature’ is modeled in several ways. This data is provided by the silicon designer. Some tools use the core test-vectors as a starting point.

Because of the complexity of modeling the current signature it is often measured under known conditions [5]. Core loading is best described as net by net resistance. This can be condensed for the entire core or divided by circuit blocks. Some vendors use statistical models as well [6]. Others have proposed the use of a Gaussian current pulse [7]. Bypass capacitor (values and location) should also be supplied by the chip designer. This should include non-switching gates that act as native bypass caps, which is switching pattern sensitive. On-chip P/G grid can be modeled as an RC circuit, or RLC circuit, or as a more comprehensive EM based broadband circuit (tool development effort is required for some of this) [8]. Three commercial tools offer modeling capability of this structure with varying degrees of sophistication [9], [10], [11].

Package P/G nets can be modeled with several commercial tools available now. Most modeling tools use a single frequency for extraction. Modeling tools need some upgrades and these have been listed later in this document. At least two modeling tools can create wideband models of the package and the PCB, either separately or together. One preferred PDN design methodology suggests use of separate models for each package and the PC Board that can be put together in the simulator [12]. At the systems level the individual package models should be simplified into a simple circuit with all bumps shorted and all balls shorted. Sometimes it becomes necessary to expand the model to provide finer granularity.

Figure 3 shows a simplified lumped equivalent circuit of the Core PDN as seen from the silicon. The IC core transient current is represented by the current source on the right. The bandwidth of the model and that of the transient noise is the widest at this point, extending way into the GHz region. The IC distribution with the interfacing package impedance creates the first major filtering, where the bandwidth usually drops below a GHz. Through large packages, the series distribution and the attached package capacitors further limit the bandwidth to the low MHz to few times ten MHz range. The board horizontal impedance with the bulk and mid-frequency capacitors create the next filtering step, reducing the bandwidth to the kHz range, which bandwidth eventually has to be handled by the VRM.

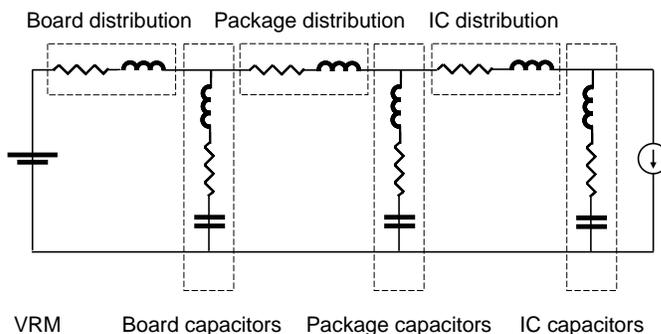


Figure 3. Simplified lumped equivalent circuit of a point-of-load Core PDN.

Output data of impedance vs. frequency can be based on measurements also, although this can capture only a limited condition of logic activity. Still this is a good starting point. The output should be compatible with popular simulators like Spice, although there is a growing need for faster simulators [13]. In case of large data file, macro-models may be used [14].

Because the PDN physically encompasses a big part of the system, noise appearing on the PDN may create not only signal-integrity issues, but also Electromagnetic Compatibility (EMC) problems. Capturing the near-field and/or the far-field radiation from a PDN with complex geometry is a very challenging task. As a first step in preventing EMC issues, the key requirement is the proper capturing of potential structural resonances.

3.1. Metrics for evaluating Core PDN

The generally accepted metric for the design of core power is impedance vs. frequency. Alternately one can use voltage-ripple + current signature [2].

Figure 4 shows illustrative core-PDN impedance profiles for a high-power CPU. Trace 'a' plots the self impedance magnitude at the board-package interface, which is the parallel of the board impedance and package+silicon impedance. The peak at 100MHz comes from the die-package resonance [15], and it is characteristic to most large package applications. The smaller peak at three decades lower frequency may be the result of the PCB-to-package inductance resonating with the on-package capacitance. Trace 'b' shows the same PDN at the silicon-package interface.

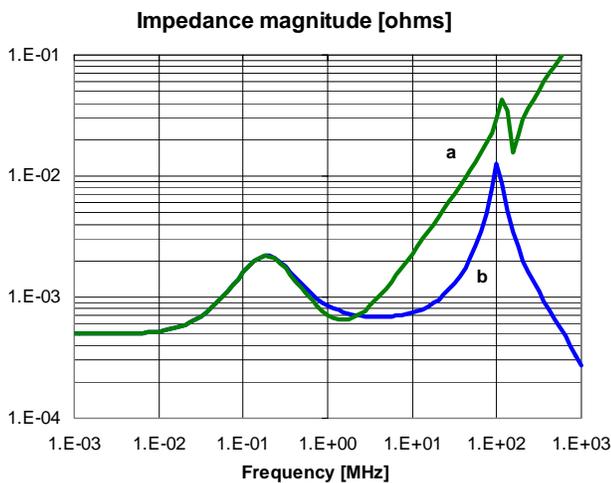


Figure 4: Illustrative impedance profiles of a high-power CPU core. Trace a: impedance of core PDN at the board-package interface. Trace b: core-PDN impedance of the same network at the silicon.

Note that besides self-impedance profiles, transfer impedance curves are also useful for EMI purposes, in determining the amount of core-clock leakage from the IC to the PCB.

4. IO PDN + SDN

Power supply noise is dependent on the return currents on the planes. Therefore the IO PDN discussion includes SDN also. The elements of IO PDN involve the following:

- 1) On-chip switching circuits (IOs). This can be in the form of driver models or an extracted net that captures the related IO structures as well. These files can become voluminous. One fix is to create macro-models that can support the various nuances of the drivers, like variable drive strengths, etc. A key item in these extracted models is the pre-emphasis. That should be included as well. Some of this sophisticated macro-modeling is still being developed at university level [16], and has yet to be commercialized. Changes have been proposed to the IBIS models to capture some of the complexities of modern IOs [17].
- 2) On-chip bypass - both add-on and native (supporting the IOs), extracted by user. The native capacitance is pattern sensitive.
- 3) On-chip P/G grid (supporting the IOs).
- 4) Package P/G and IO nets, plus bypass caps.
- 5) PCB P/G structures, signal nets, and bypass schemes used.
- 6) Connectors for signal nets on the PCB, and for P/G (if used).
- 7) Far end package IO structures and input circuitry of the receiver circuit. This should include the terminations, the ESD network, etc. Again a macro-model may be useful substitute of a large extracted net.
- 8) VRM(s)

Most comments listed under core-PDN apply to IO PDN as well.

The IO power and signals interact non-linearly via the drivers, and should preferably be modeled and simulated together. Both frequency domain and time domain simulations are required. It is also preferable to have broadband models for both PDN and SDN structures.

The return currents on the planes generate the coupling between the PDN and the signal lines. Hence, signal referencing is a very important constituent of I/O design in the package and board. Providing appropriate path for the return currents translates into the assignment for power and ground at the package – board interface. Since most ICs today support thousands of signal I/Os with comparable power and ground I/Os, thousands of interconnects need to be analyzed in the package to assess the impact of power supply noise on eye diagrams. To complicate matters further, the PDN consists of multiple plane layers containing thousands of vias and loaded using hundreds of capacitors. Though the complexity of the problem is enormous, approximations based on the understanding of the return currents can greatly simplify the problem to be solved. Macro-modeling is one of many methods that can be used to simplify the problem. An example is shown in Fig 5 where a multi-layered PDN is first modeled

using an electromagnetic solver and the frequency response at specific points represented using a macro-model in Spice. Using transmission line models of interconnects referenced to the macro-model, power supply noise can be simulated. Since the distributed nature of the PDN is captured in the macro-model, this method does not degrade the accuracy of the results. Moreover, non-linear macro-models can be connected to the signal lines to improve the accuracy of the simulations.

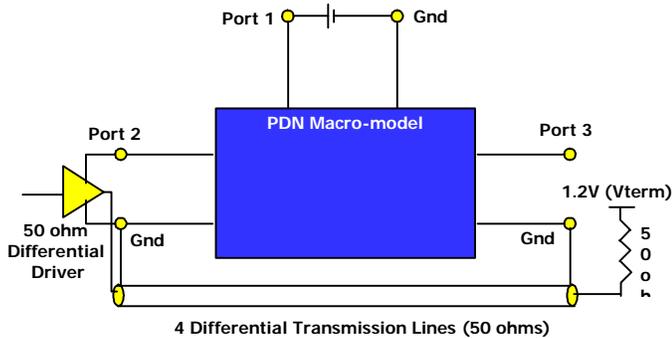


Figure 5: PDN and SDN Modeling using Macro-models

Though macro-modeling provides a method for coupling the PDN and SDN models, it has limitations. Most macro-modeling methods are limited to a finite number of ports. Even if this limitation is overcome, the spice netlist for a PDN macro-model with many ports can become unmanageable. In addition, since macro-models are generated using band limited frequency data, these models can violate causality. Macro-models violating causality can lead to the artificial closure of the eye, as shown in Fig 6 where a 30mV voltage reduction is seen when causality is violated using macro-models [18].

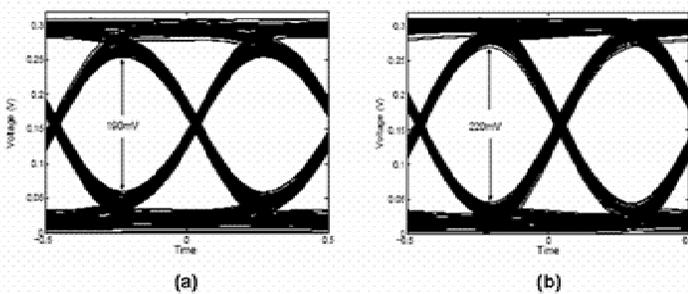


Figure 6: Impact of Power Supply Noise on Eye Diagrams (a) before and (b) after causality enforcement

4.1. Metrics for evaluating IO PDN

Eye Diagram. The standard for this is best described by the user, depending on their requirements. Since the power supply noise on the PDN couples into the signal lines, the eye diagrams are a good metric for evaluating the impact of noise on signal propagation.

Logic Failure: This has been suggested by some, but is not commonly used. This is a more difficult problem to simulate since logic failure mechanisms vary between systems.

Delay: This has been suggested by some, but is not commonly used. A more important parameter could be the jitter.

Impedance Vs frequency: Similar to the core PDN, impedance could be defined for the I/O power delivery network. However, since the return currents dictate the noise on the power planes, impedance at multiple points need to be computed.

5. DESIRABLE COMMON BASIC FEATURES FOR BOTH PDNs

The starting point for PDN design is always a DC design. That requires a DC resistance calculator. The terminals for this should be defined by the user. This may simply condense all the sources (solder-bumps or wire-bonds) and all the sinks (balls or pins) into a two terminal net for each power and ground net, OR break them into groups specific to some circuit blocks OR simply group them into geographical regions. It should be noted that DC resistance is not modeled by every modeling tool. Some tools try to mimic DC conditions by choosing a frequency at which the skin depth is equal to half of trace thickness, but this is not representative of the many via sizes or plane thickness, which may be different from the trace thickness.

6. PROPOSED REQUIREMENTS FOR MODELING TOOLS

A very important requirement for modeling the PDN is the ability to analyze these structures at multiple levels and pass information between levels. An example is shown in Fig 7 consisting of the behavioral level, transistor level and physical level.

The behavioral level captures the architectural details of a microprocessor such as current drawn, frequency, power etc with compact models of the PDN. The transistor level consists of spice simulations with non-linear circuits and circuit models of the PDN. The physical level contains the three-dimensional structures of the PDN with detailed analysis using electromagnetic simulators. One method for passing information between levels is through both linear and non-linear macro-modeling. Though system definitions and designs tend to follow these three options, presently, none of the commercial tools support these three levels. Most tools are confined to just one level.

Here is a wish list of upgrades that could be incorporated:

- Can download stack-up info from various design tools and include a reasonable library of material properties.
- Support rapid extraction of frequency dependent impedance of multiple P/G plane stack-up for quick PDN only analysis, AND “P/G+signal” extraction for accurate PDN+SDN analysis.
- Support “condensation/merging” of P/G pins and/or vias, when needed to simplify models.
- Support de-embedding of reference nodes inside a structure that do not need to be connected to the global ground; e.g: bypass cap nodes. This is especially true of tools that yield S-parameters.

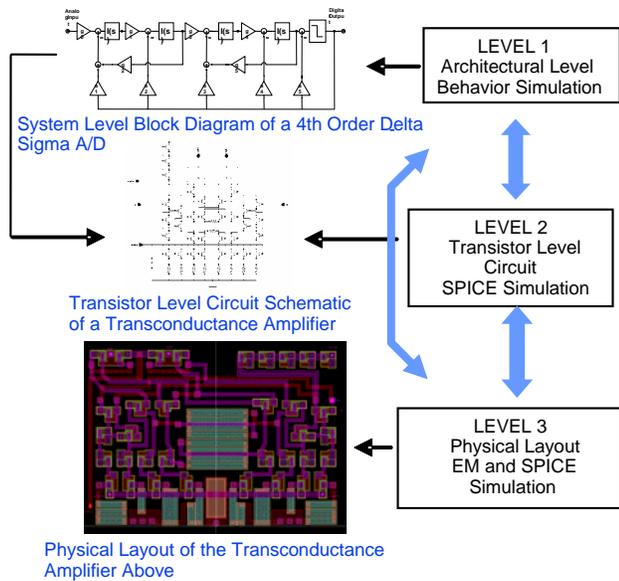


Figure 7: Hierarchy in PDN Analysis

- Accept incorporation of different electrical models for decoupling caps and other passive elements, when modeled together.
- Generate frequency dependent impedance for all structures (IC, Package, and PCB) to include PDN+SDN for IO power.
- Output compatibility with network simulation tools
- Should also be able to convert between S,Y,Z,ABCD formats, and also from frequency dependent model parameters into equivalent time domain sub-circuits without causality problems.
- Model PCBs, Packages, On-chip P/G Grid, Sockets, Connectors, VRMs (could be several tools)
- Multi-port macro-model generation capability to reduce complexity.
- Calculate bandwidth of validity for the user. Provide methods to enhance it.
- Must be flexible enough to model portions of a system (pkg by pkg, or portions of PCB, or pkg + small portion of PCB around it), so that models of either can be used elsewhere.
- Should deliver output that can be used in a simulation engine elsewhere (outside the tool’s framework) in a standard format.
- Sensitivity analysis based on tolerances of geometry and material properties would be helpful in a combined modeling/simulation tool.
- Incorporate effect of trace edge shape, otherwise error in Z_0 and crosstalk of up to 10% or more can result [19].
- Use actual shape of via structures.
- Include all couplings (e.g: between traces and between vias, etc.)
- Include effective and accurate ways to account for ‘holy’ planes, splits, irregular plane outlines, and large internal cutouts.

An EM based numerical method is required to model the linear network consisting of planes, decoupling capacitors, vias and other power distribution interconnect structures. Since, the target impedance is a measure of the performance, the output are impedance parameters varying as a function of frequency. This could be 1-port, 2-port or n-port parameters, but it is advantageous to limit the number of ports. Modeling tools have evolved over time; however, most lack in one capability or another.

7. PROPOSED REQUIREMENTS FOR SIMULATION TOOLS

Most designers use simulation tools like HSPICE or ADS. New simulation tools have also emerged ([9] and [10]). Here is a short list of requirements that are not fully incorporated into any of these tools:

- Fast and reasonably accurate simulators to handle large busses along with their P/G network (PDN+SDN). Certain design methodologies require these simulators to handle very large number of nodes.
- Accept lumped as well as behavioral (Macro-models) models compatible with IBIS-4. Pre-emphasis would be helpful and often quite necessary.
- Support time-domain and frequency-domain analysis with built-in software for conversion of waveforms between them.
- Should be able to handle required bandwidth. Allow user to test for passivity and bandwidth.
- With the shrinking noise margins in presence of structures whose geometrical tolerances are rather large (5 to 10%), statistical simulation methods, other than Monte-Carlo type, are needed to get faster results [20].

8. METHODOLOGY

Modeling, simulation, and analysis of PDN is done in several ways, depending on the size and type of system. Some tools include all these functions, and are therefore used for small systems with one or two packaged ICs [9]. Others model packaged parts separately and PC Boards separately, and then place them all together in the simulator [12]. So methodology is usually user defined. The format of interface data used also varies by user: some use impedance matrices, others use transmission matrices based on ABCD parameters [21]. That is why conversion between Z, Y, ABCD, etc, is necessary for all modeling tools. PDN design can get too complicated in a hurry due to the enormous number of nodes involved. This requires judicious choice of reduction of the problem based on an understanding of the macro-space (board level) requirements versus micro-space (chip-package level) requirements. The IC design community learned by default about the importance of standards for data transfer, which involves data format as well as rules of interpretation of that data across tool boundaries. Unfortunately it is so complicated that every design house must have a “methodology team”. Hopefully that will not happen to PDN design community if we adopt standards early on.

9. STANDARDS

One of the biggest stumbling blocks at the moment is the lack of a standardized interface definition at the boundaries (silicon-package and package-board) [22]. If we had a standard way to exchange simulation information at these boundaries, the 'owners' of each section could go out and develop better simulation tools without the risk of being incompatible with tools for the other sections. It is instructive to think about the silicon-package-board-package-silicon path as a high-speed serial link, where we have several good examples of having interface standards. All of the serial-link standards have compliance points and specifications that people have to maintain at those points, together with the definitions of the interfaces. This allows a cable manufacturer to develop a compliant cable without knowing the board and silicon details. The PDN is physically more complex, because it is a multi-node network. The challenge is to find the proper level of abstraction to describe the interfaces so that they capture all of the important aspects (such as a wide area array package-board or package-silicon connection) and yet it maintains a simple and generic form. For each interface we may want different complexity levels; the package-board interface can be rightfully modeled with a single node when only the silicon is simulated, and similarly the silicon-package interface can be rightfully modeled as a single lumped node when only the board is simulated. Specific suggestions have been made for specifying broadband target impedance in frequency domain at each interface. Similar suggestions have been made for specifying current signature/ripple voltage in time domain.

10. CONCLUSION

Core and IO PDN designs require complex tools, capable of doing co-analysis of silicon, package and board. Standardized interface definitions and data input/output formats are required to enable further developments of these tools.

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