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Waveform Distortion in Length-equalised Clock-Distribution Interconnects

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Abstract

To reduce the skew among signals, it is a common practice in physically large multiconductor clock-distribution networks to equalise the length of interconnects. Equalisation of length is usually done by forming a serpentine of some of the traces. To keep the required board area small, arms of the serpentine may have non-negligible coupling. The crosstalk among the serpentine arms will modify the transfer function of the trace and results in distortions of the time-domain clock waveform. A scaled microstrip DUT was designed, built, simulated and measured to show some aspects of the frequency and time-domain response of a clock serpentine.

I. INTRODUCTION

To achieve high operating speed in computing and communications equipment, it is often necessary to reduce the skew among dedicated signals to the minimum possible. In synchronous systems, the most critical signals are the clock signals which provide the timing for transferring data. In complex systems the number of clocked circuits may be very large. The large number of devices in itself means that the passive clock distribution network must be physically large, which can give rise to significant skew unless all interconnections from the clock source to any given load have the same propagation delay. Entirely new techniques with dedicated hardware solutions may also be used to reduce the skew even further [1].

II. CLOCK DISTRIBUTION NETWORKS

II.1. Daisy-chain clock distribution

A significant advantage of daisy-chaining the clock loads that practically there is no limit on the number of loads that one single driver can drive. This fact in itself reduces the skew by eliminating the skew of active parts in the successive fan out stages.

It is also known that the propagation delay of passive interconnects is modified by the loads along the trace. Approximating the daisy-chained clock inputs as small capacitances, the load will increase the delay. In simplified calculations the delay is obtained by simply adding the total load capacitance to the total line capacitance in the expression of delay. On the other hand, the presence of loads on the transmission line not only increases the delay, but also increases the transition time of the signal gradually from the source toward the far end, which phenomenon further complicates the accurate calculation of skew in daisy-chain topologies [2].

II.2. Parallel clock distribution

To eliminate the excess delay and skew due to daisy chaining, each clocked device can have its dedicated clock driver and trace in a parallel system (e.g., star network, or H-tree). One possible realisation is shown in Figure 1. If the current capability of the driver permits, several traces can be driven by the same driver. For a large number of clocked devices this approach requires a correspondingly large number of drivers (possibly in the same package so that chip-to-chip skew can be minimised) or even better a strong driver to drive all clocked devices from the same source. In such networks, the skew can be ultimately minimised by equalising the physical length of interconnects leading to each device. Figure 1 shows a meander-like serpentine.

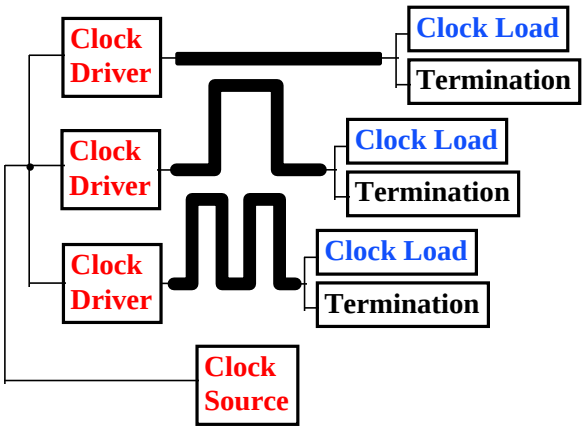

Figure 1.: Topology of a parallel clock-distribution network. For the sake of simplicity, parallel far-end terminations are assumed on all traces. Note that near-end series termination instead of the parallel one could be used instead to reduce the current requirement.

The length of traces is determined by the maximum of lengths between any clocked device and the clock source. Traces which otherwise would be shorter may have the excess length in the form of a meander-like serpentine. If the arms of the serpentine are far enough that coupling between them cannot affect the waveform, the equalisation of length works without any deterioration of waveform. If, however, coupling is not negligible, which can be easily the case when the tight board area does not permit the sufficient spreading of serpentine arms, the crosstalk shows up on the far-end waveform. The crosstalk behaviour of coupled transmission lines is widely covered in the literature. In printed-circuit applications the typical constructions are the planar microstrip and stripline multiconductor transmission lines [3], [4].

However, in terms of the effect of coupling on the waveform, there is a significant difference between applications of generic logic signals and of the clock serpentine. In most digital applications, crosstalk is viewed as the injected noise from a trace carrying a logic signal (active trace) onto a neighbouring trace which carries a different or no signal at all (victim trace). In such cases the time-domain transient response of the multiconductor system is used to predict the resulting noise. In clock-distribution circuits, and especially in clock serpentines, all of the traces involved carry the same periodical signal, and therefore it is the steady-state (i.e., the frequency-domain) solution at the discrete frequencies of the clock signal that determines the response of the network. The frequency-domain description of crosstalk is also covered in the literature to illustrate the crosstalk behaviour of coupled traces, see e.g., [5].

III. Device Under Test

To investigate the effect of coupling in the arms of a clock serpentine, a blown-up model of a three-trace serpentine was designed (see Figure 2), built, simulated and measured. A blown-up model was chosen in order to be able to reduce, or possibly neglect the effect of the losses in the traces. The microstrip structure had an overall length of 1800 mm, the nominal trace impedance was 50 ohms. The electrical parameters were calculated by a field-solver software [6]. The per-unit-length electrical parameters of the DUT are shown in Table I.

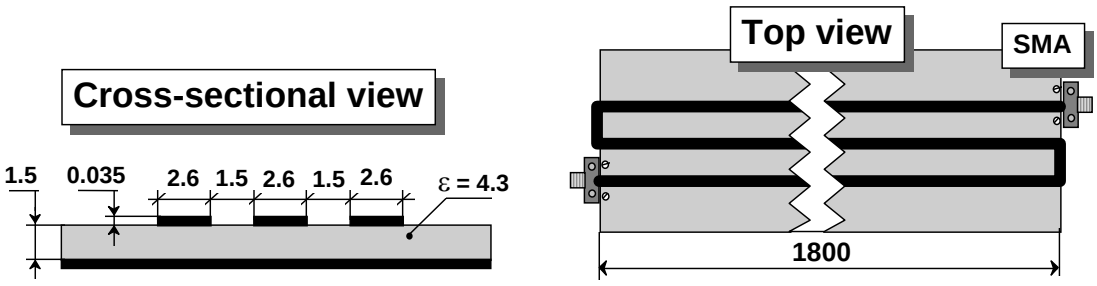

Figure 2.: Device Under Test constructed on a 1.5 mm thick FR4 material. The three coupled microstrip traces are looped to form a serpentine. All dimensions are given in mm.

+CMATRIX =

+	**1.258e-013**	**-1.076e-014**	**-8.159e-016**
+		**1.273e-013**	**-1.076e-014**
+			**1.258e-013**

+LMATRIX =

+	**3.113e-010**	**5.286e-011**	**1.619e-011**
+		**3.089e-010**	**5.286e-011**
+			**3.113e-010**

+RMATRIX =

+	**4.907e-004**	**4.012e-005**	**1.307e-005**
+		**4.914e-004**	**4.012e-005**
+			**4.907e-004**

+fskin = 1.000e+009

+rskin =

+	**3.555e-003**	**3.560e-003**	**3.555e-003**

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*** All values are for one mm length**

*** RMATRIX calculated at a frequency of 1.000e+009**

Table I. Per-unit-length electrical parameters of the DUT.

IV. SIMULATION AND MEASUREMENT RESULTS

First the step response of the serpentine was investigated. Figure 3 shows the simulated response of the DUT for a piece-wise-linear step with 0.2 nsec rise time. The simulation used lossy coupled transmission line models with the input data shown in Table I. On the left, the overall response is shown. To see the deterioration of the rising edge, on the right the horizontal scale is stretched 10 times around 35 nsec. The following details are important to note on the waveform: (a) the plateau between approximately 10 and 30 nsec is the near-end crosstalk waveform that is coupled directly from the input to the output of the second arm, and (b) on the zoomed scale it is well noticeable that in contrast to the 0.2 nsec input-drive edge, the rising edge of the output waveform is approximately 3 nsec long. Because of the plateau of the direct feedthrough near-end crosstalk, the markers are set to the 0.2 and 0.8 V points (20% and 80% of steady-state full-scale values) rather than the 10% and 90% values. Figure 4 shows the measured responses under the same conditions. Note the good correspondence between the simulated and measured waveforms.

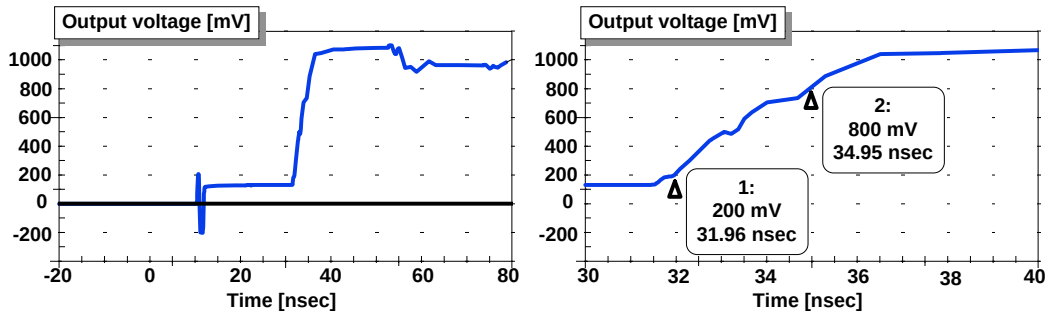

Figure 3: Simulated time-domain response of the serpentine to a 0.2 nsec 0-to-1V piece-wise-linear step stimulus.

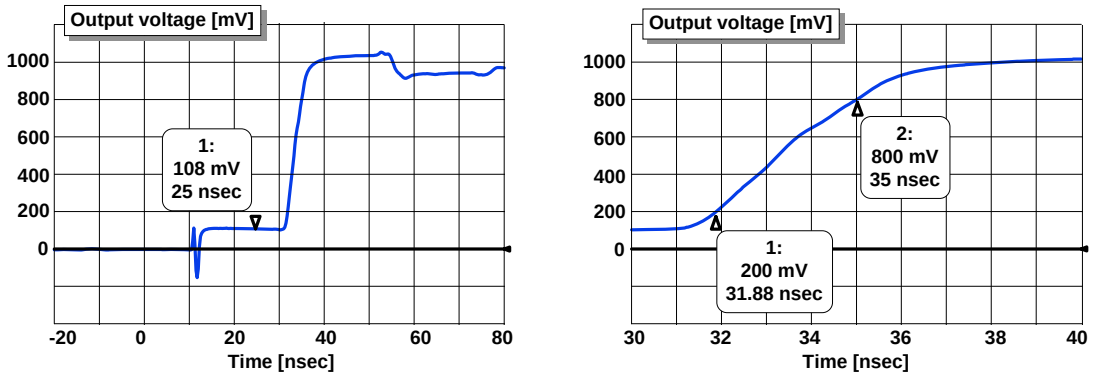

Figure 4: Measured time-domain response of the serpentine to a piece-wise-linear step stimulus.

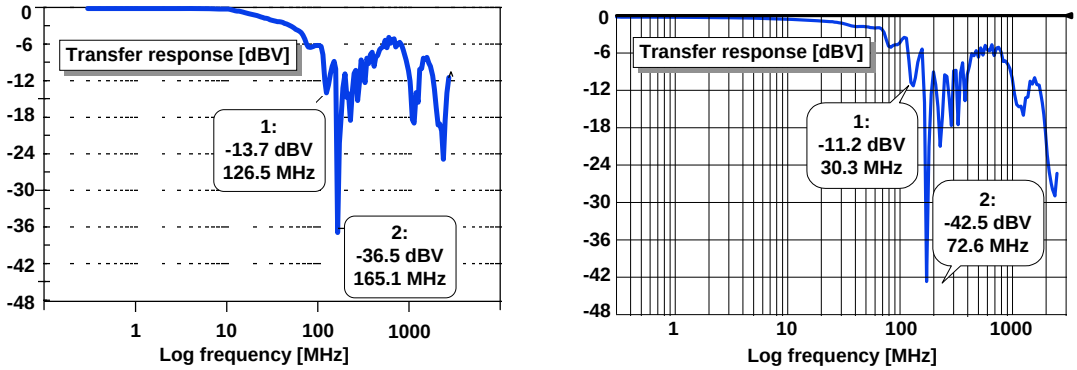

Figure 5: Simulated (on the left) and measured (on the right) frequency-domain response of the serpentine.

The distortion of time-domain waveform shows up as a roll-off and dips in the frequency-domain response. Figure 5 on the left and right shows the simulated and measured transfer functions, respectively. Note again the good correspondence between the simulated and measured values. The sharp dips in the frequency response suggest that for a periodical clock signal we can expect sudden changes in the output waveform as the input frequency varies. This is in fact verified on the measured waveforms of Figure 6.

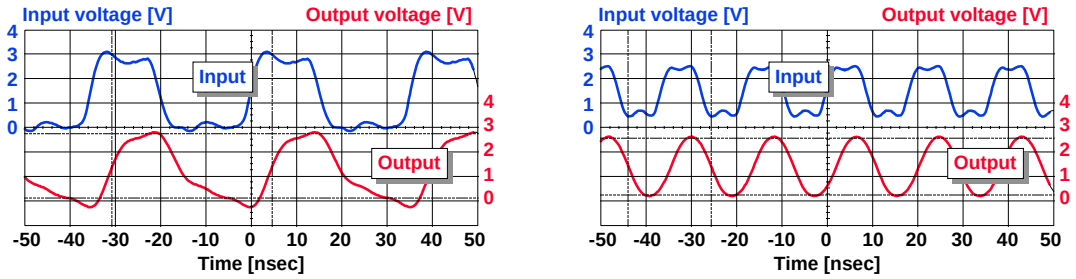

Figure 6: Measured time-domain waveforms on the DUT for periodical excitations with two different frequencies.

In Figure 6, the periodical response of the DUT can be seen for two different input frequencies. For both measurements the source was a square-wave generator with a source impedance of 50 ohms. The source voltage was set to swing between 0 and 3 volts across a nominal 50-ohm load. The output rise and fall times with the nominal 550-ohm load were set to 5 nsec. The DUT was driven by the 50-ohm source impedance of the generator and was terminated at the far end by the 50-ohm input impedance of the oscilloscope. On the waveforms on the left, the input frequency was 28.3 MHz. The measured transition times on the output waveforms between the 10% and 90% points were 6.5 nsec and 10 nsec, respectively. Note the undershoot and the significant increase of transition time on the falling edge. On the right, the input frequency was 54.4 MHz, the output rise and fall times were 5 nsec. Note the

change of waveshape of the output signal, which looks more like a sinewave, suggesting that the harmonics of the square wave are significantly attenuated by the dips in the frequency-domain response.

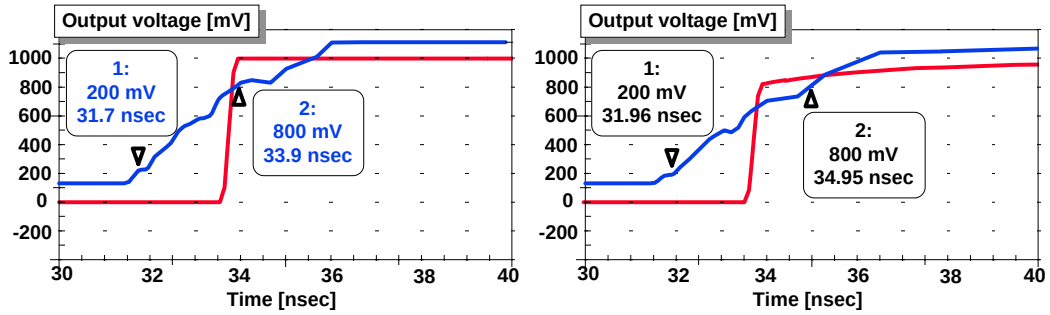

Figure 7: Simulated waveforms with lossless (on the left) and lossy (on the right) models. Fast edges are from the equivalent uncoupled trace.

Another question to be answered whether the increase in output transition time is associated with a reduced or increased overall delay in the serpentine. Some comments in the literature suggest that meander-shaped clock-distribution networks are also associated with and increased delay [7]. For the Device Under Test in our case, Figure 7 shows the simulated lossless (on the left) and lossy (on the right) step responses of the DUT serpentine and those of a single trace with the same overall length. Note the vertical shift of the serpentine's waveforms which is due to the crosstalk plateau on the left of the waveforms, and due to the reflection overshoot on the right of the waveforms. Since the waveform on the left graph assuming a lossless meander trace also shows a significant increase of output risetime, we can conclude that the increase of the transition time of the serpentine's output is primarily not due to the losses. And because the approximate delay to the 50% midpoint of the waveforms on the meander and on the equivalent-length straight trace is approximately the same, it can also be concluded that the meander itself will not noticeably change the total delay of the path.

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References

[1] Wayne D. Grover, "A New Method for Clock Distribution," IEEE Transactions on Circuits and Systems -I, Vol.41, No.2, February 1994, pp. 149-160.

[2] I. Novak, "Modeling, Simulation, and Measurement Considerations of High-Speed Digital Buses," IEEE Transactions of Instrumentation and Measurement, Vol. 41, No.6, December 1992.

[3] A. Feller, H.R.Kaupp, and J.J.Digiacomo, "Crosstalk and Reflections in High-Speed Digital Systems," Proceedings of the Fall Joint Computer Conference, 1965, pp. 511-525.

[4] Hong You, M. Soma, "Crosstalk Analysis of Interconnection Lines and Packages in High-Speed Integrated Circuits," IEEE Transactions on Circuits and Systems, Vol.37, No.8, August 1990, pp. 1019-1026.

[5] C. R. Paul, Introduction to Electromagnetic Compatibility. New York: John Wiley, 1992.

[6] R. Raghuram, D. Divekar, P. Wang, Electrical Modelling and Simulation of Interconnects and Electronic Packaging," presented at the International Society for Hybrid Microelectronics (ISHM), San Francisco, October 1992.

[7] Michael K. Williams, "Design Trade-offs in High-Speed Clock Distribution and Reception," Proceedings of the 1993 Autumn Japan High Speed Digital Design Symposium, Hewlett Packard, 1993.