Overview of Some Options to Create Low-Q Controlled-ESR Bypass Capacitors

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Abstract:
Low-Q bypass capacitors with controlled ESR offer the advantage of creating resonance-free Power Distribution Networks (PDN) with low sensitivity to component tolerances, and achieving a predictable impedance profile with the minimum number of components. Low Q bypass capacitors, termed Bypass Resistors, can be created either by reducing the inductance of the part, and/or by raising the Equivalent Series Resistance (ESR). In multi-layer capacitors, ESR can be raised by using resistive plates, and/or resistive terminations, or by adding resistance externally with low inductance. Low-resistance capacitor plates can be patterned outside the high-frequency current loop. In thin-film capacitors, ESR can also be raised by reducing the thickness of capacitor plates.

I. Introduction

The most common component in PDN is the capacitor. Bypass capacitors in many designs have to cover a very wide range of frequencies, from the low kHz values up to hundreds of MHz on boards, and possibly up to the GHz range in packages. It is not practical with today's components to cover this entire frequency range with a single capacitor or multiple copies of the same capacitor. PDNs have to provide a pre-defined impedance profile [1], and it is the designer's task to select the proper capacitor types and values to synthesize the target impedance profile. One possible approach is to place the *Series Resonance Frequencie*s (SRF) of moderate-Q bypass capacitors along the frequency axis [1]. While this approach works well up to about 100MHz, the uncertainties in ESR and *Equivalent Series Inductance* (ESL) of the capacitors may shift the SRFs of parts, pushing anti resonance peaks higher. In addition, the low ESR associated with *Multi-Layer Ceramic Capacitors* (MLCC) tends to create a resonance peak between the capacitors' inductances and the plane capacitance. It was realized ([2], [3], [4], [5]) that the resonance peaks are suppressed if capacitors have substantially higher ESR. A well-defined (controlled) ESR not only reduces the resonance peaks, but together with low-inductance packages, the Q of the part can be substantially reduced, so that the impedance profile of an individual capacitor has a pronounced flat bottom. This helps to separate the adjacent capacitor banks, hence further reducing the sensitivity of the design based on Distributed Matched Bypassing [5]. ESR values of bulk capacitors come in a wide range; depending on dielectric material and construction, milliohms up to ohms and their impedance profiles usually have the flat bottom. High-frequency capacitors, however, evolved to have low ESR and medium-to-high Q. Though techniques have been evaluated to raise the ESR of ceramic capacitors, as of today no commercially available such component exists. This paper gives an overview of some of the possible solutions to create low-Q controlled-ESR bypass capacitors, which were termed *Bypass Resistors* [5].

II. Generic considerations for Bypass Resistors

The Q of a capacitor is defined as Q=sqrt(ESL/C)/ESR. It was shown ([4], [5]) that the sensitivity of PDN impedance to component tolerances is reduced with Q<<1 parts. Q can be minimized by reducing ESL or increasing C, and/or increasing ESR. ESL is determined by the current loop encompassing the internal structure of the capacitor and the external connections (pads, vias, traces, planes) completing the loop. For most capacitor constructions, higher capacitance with the same dielectric material requires a more complete 'fill' of the body, which tends to reduce the high-frequency inductance. The capacitance of Bypass Resistor is therefore a single value: the highest capacitance in the case style with the given dielectrics. Controlled ESR can span a few decades, from milliohms to ohms with E3 or E6 series.

III. Some possible constructions of Bypass Resistors

III.1 Reducing inductance and Q in bulk capacitors

Tantalum and electrolytic capacitors in the multi-hundred uF capacitance range may exhibit a few hundreds ohms of ESR. The large volumetric capacitance allows us to create small-size capacitors, which could have low inductance and low Q. Traditionally, however, even the brick-style cases exhibit large inductance. This is due to the clip connections at both terminals. Recently, multi-anode constructions were introduced, which reduce mostly ESR, but reduce inductance only proportionally to ESR. Inductance and Q can be lowered by face-down constructions [6]. The construction of such a capacitor is shown on the left side of Figure 1. Its measured impedance and inductance profiles are shown on the graph of Figure 1, traces A. As a comparison, conventional-construction capacitor of the same capacitance and case style are shown in traces B. Some of these capacitors are offered in different ESR bins. This means each part has to be tested for ESR, and this raises the possibility of obtaining these capacitors with a known and guaranteed range of ESR.

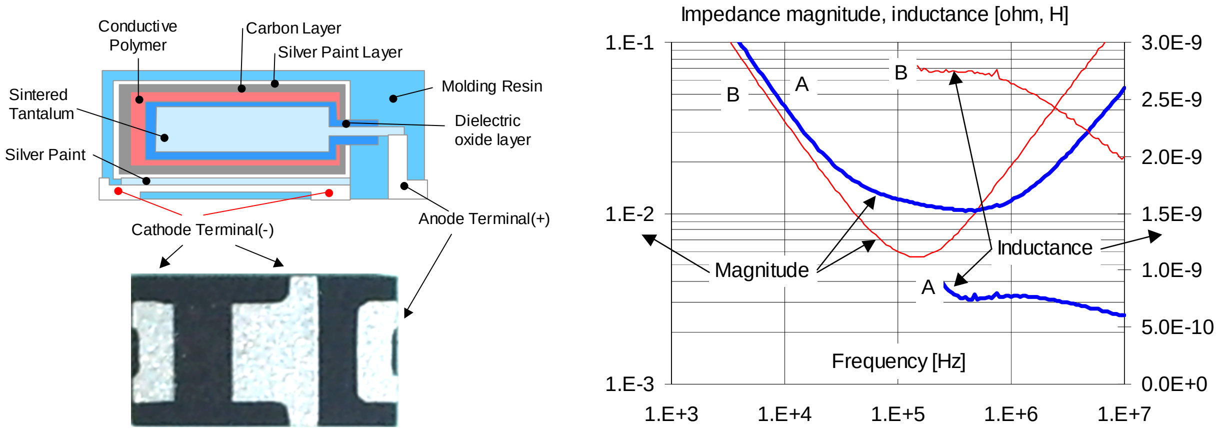

Figure 1: Left: construction and bottom view of face-down capacitor in D-size case. Right: impedance magnitude and inductance versus frequency measured on two 470uF D-size capacitors. Traces A: face-down construction from vendor A, Traces B: conventional construction from vendor B.

III.2 Adding resistance to MLCC

As shown on the left of Figure 2, series resistance can be added by incorporating highly resistive material into the capacitor construction: resistive capacitor plates, resistive terminations [7], or low-inductance external embedded resistors [5]. The graph in Figure 2 shows the impedance magnitude, real part and inductance of a 0603-size 10nF MLCC with 4 ohms of ESR.

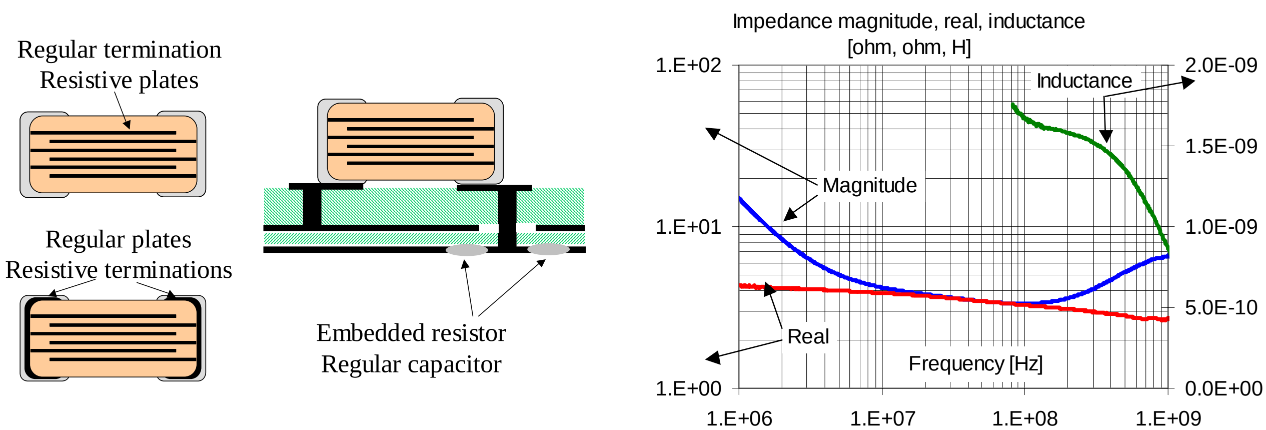

Figure 2: Left: three construction options to add resistive material to multi-layer capacitors. Right: impedance magnitude, impedance real part and inductance of a 10nF 0603-size capacitor with resistive plates, ESR=4 ohms.

III.3 Patterning the plates in MLCC

In MLCC parts, most of the series resistance comes from the capacitor plates. For conventional two-terminal parts, the plate construction is shown in Figure 2. The cumulative resistance of the plates is: $ESR=L/(\sigma TWN)$, where σ is the conductivity of capacitor plates, L, W and T are the length, width and thickness of plates, respectively, and N is the number of metal plates. In a given case style and dielectric material, higher capacitance requires more and thinner dielectric layers, which drives N up. If N grows faster than how T drops, ESR goes down.

Without changing the numbers in the above ESR expression, resistance can be increased by forcing current through narrowed channels on the plates, called patterning. We want to increase ESR by patterning the plates without increasing ESL of MLCC parts, therefore we have to pattern the plates in areas outside the 'keep-out' zone, determined by the high-frequency current loop (see top-left sketch in Figure 3). Some of the options are:

- use vertical capacitor plates and pattern them away from the PCB planes, above the 'keep-out' zone, or
- with horizontal plates, pattern only those which are above the 'keep-out' zone, or
- pattern horizontal plates outside the 'keep-out' zone, horizontally displaced from the high-frequency current loop

The sketches on the left of Figure 3 illustrate some of these options. On the top left, an MLCC is shown with horizontal plates, which is the regular mounting style. The high-frequency current loop closes on the bottom plates, where patterning would also increase inductance. Patterning on the upper plates (outside the 'keep-out' zone) increases ESR without increasing ESL. The top middle sketch shows the front view of an MLCC with its body extending horizontally beyond its terminals. Patterning in the extra horizontal area increases ESR without increasing ESL. On the bottom left, an MLCC is shown with vertical plates. Patterning outside the high-frequency path (patterning is shown as white U shape) increases ESR without impacting ESL. Multi-terminal MLCCs raise the possibility to connect each plate only to one or few of the terminals, thus increasing ESR. Due to the thin capacitor plates, all terminals are still connected to plates at a very low height, close to the PCB return path, thus inductance is hardly impacted. On the mid bottom of Figure 3, an eight-terminal capacitor is shown. The graph on the right shows the impedance real parts and inductances for two eight-terminal capacitors with the same 0508 case size and same 470nF capacitance. Thick lines: capacitor plates not connected to all terminals (manufacturer C, traces C). Thin lines on the same graph show the values when plates are connected to all terminals (manufacturer D, traces D). SRF is indicated by a small V-shape section of the impedance magnitude curves. Note that with the single-terminal plate connection, inductance changes by a few percent, whereas resistance increases by a factor of at least three.

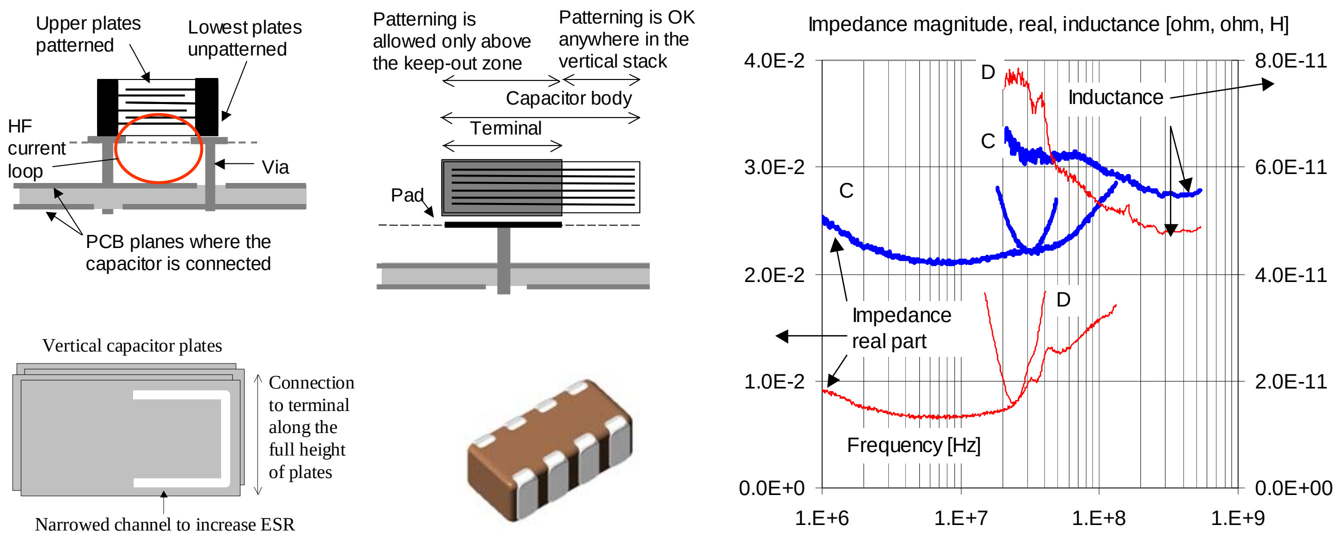

Figure 3: Plate patterning options are shown on the left. Impedance real parts and inductances of multi-terminal capacitors with single-terminal plate connection versus all-terminal plate connection are shown on the right. For both capacitors, SRFs are indicated by a short V-shape segment of their corresponding impedance magnitude curves.

III.4 Thin film capacitors

Instead of increasing the resistivity of capacitor plates, ESR can also be increased by making the plates thinner. Thin-film capacitors can be constructed with low or high dielectric constant materials and with single or multiple layers [8], [9]. Low-Dk, multi-layer film capacitors are becoming available [10]. The plastic film capacitors have low volumetric capacitance, and their primary application is low-distortion audio circuits. For low-inductance applications, plastic film capacitors can be made in reverse geometry with significant length. 0603-XX (60-mil wide and 30-mil, 2-mm, 4-mm, 6-mm, 8-mm, and 10-mm length) reverse-geometry film capacitor samples were measured in different configurations. Figure 4 shows the measured impedance of 0603-4mm and 0603-10mm capacitors in a via array and on regular 0603-size pads mounted in the middle and at the end. The impedance profiles show that the electrical properties of long reverse geometry capacitors can be altered by changing the lengths and/or positions of connections to the terminals. ESR of the 10-mm long part can be manipulated in a 10:1 range merely by changing the mounting geometry. As long as the full terminal is connected, the inductance of a long reverse-geometry film capacitor drops inversely with its length. Note that connecting only part of the terminal raises not only resistance but also inductance. This solution is shown here as an illustration for the sketch on the mid-top of Figure 3.

Conclusions: low-Q controlled-ESR capacitors can be constructed in several different ways. Face-down bulk capacitors, MLCCs with resistive plates, resistive terminations and/or with properly patterned plates, as well as film capacitors have been shown to achieve low Q.

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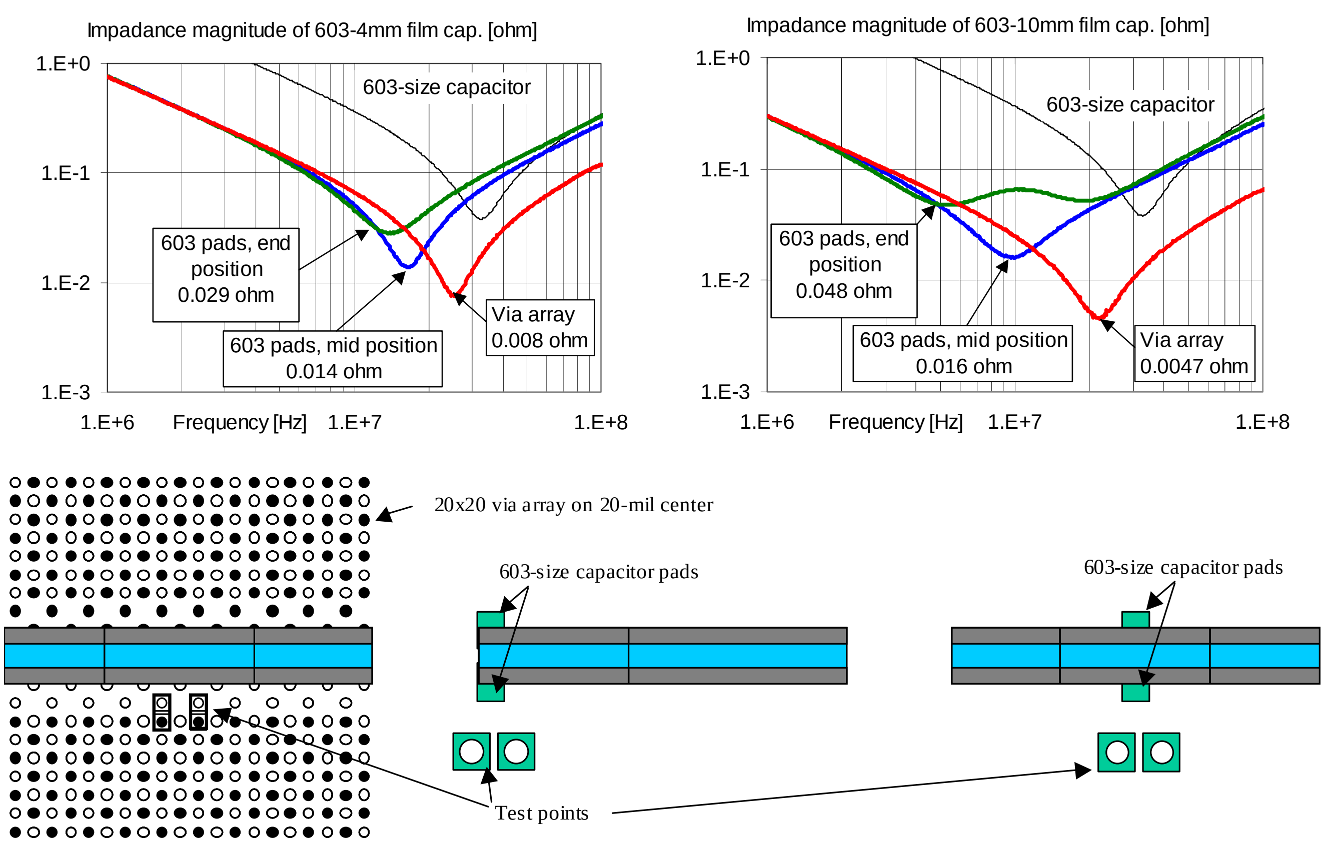

Figure 4: Impedance magnitudes of 4-mm long (on top left) and 10-mm long (top right) 0603-XX film capacitors, mounted and measured in three different configurations, shown on the bottom. The impedance magnitude of a 0603-size capacitor is shown for reference: its impedance was the same in all three configurations. Left: 20x20 via matrix with checker-board pattern, capacitor mounted centered in the middle, measured immediately below capacitor. Center: capacitor mounted on regular 0603-size pads at its end. Right: capacitor mounted on regular 0603-size pads in the middle. Light shape: 10-mm part. Dark shape: 4-mm part. ESR is listed for each trace in its label.