

Modeling the Impact of Power/Ground Via Arrays on Power Delivery

Sun Microsystems

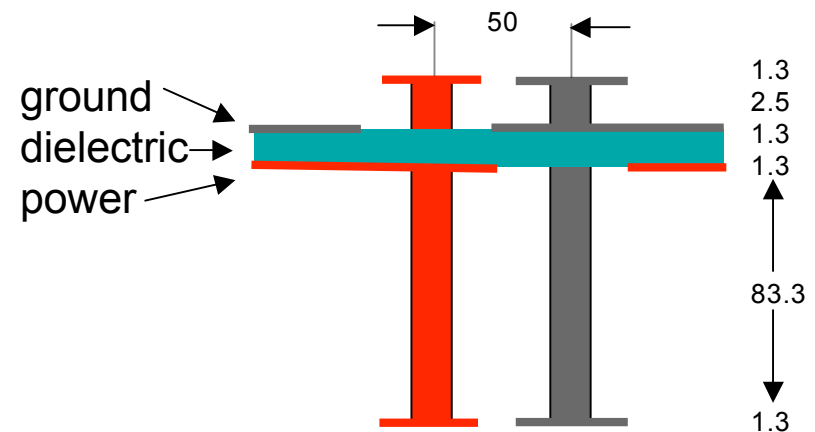
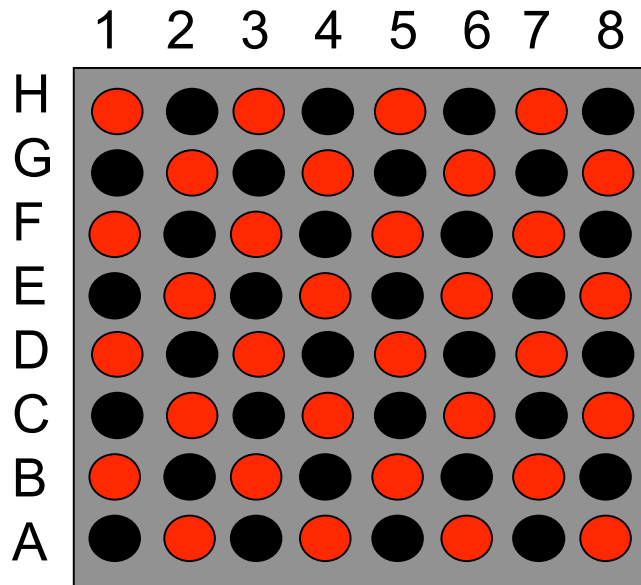
Jason R. Miller

Istvan Novak

Abstract

The impact of via arrays on power and ground planes is examined. Measurements of the plane impedance were made on a 8 x 8 via array as a function of via pair location. The results from full-wave field solution are compared to measurement data and excellent correlation is obtained. The results show that the impedance and effective inductance is a strong function of location within the array. The lowest impedance and inductance is measured on the array perimeter. A 4 X increase in the impedance and inductance occurs in the array center. By parameterizing the antipad diameter in simulation it is found that the impedance increases sharply when the antipads overlap.

Test Board Design



Sets of 8x8 via arrays with alternating P/G via pairs on 2.5" x 10" board

Test Board Measurements

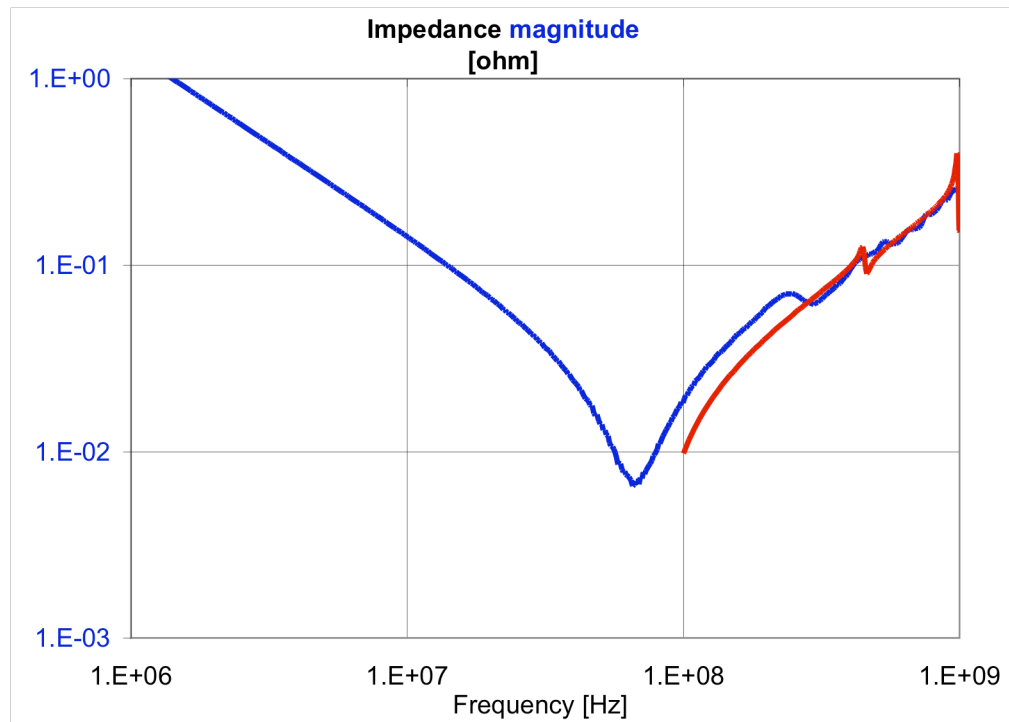
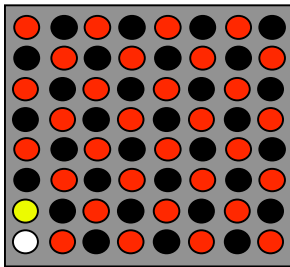
- HP 4396A VNA, 100 kHz-1.8 GHz
- Semirigid coaxial probes on opposite sides of the board
- Full two port calibration

Simulation Conditions

- Ansoft HFSS 9.2.1, 3D FEM solver
- Fully parameterized project
- 2.5" x 2.5" board with 64 vias was simulated

Simulation vs. Measurement

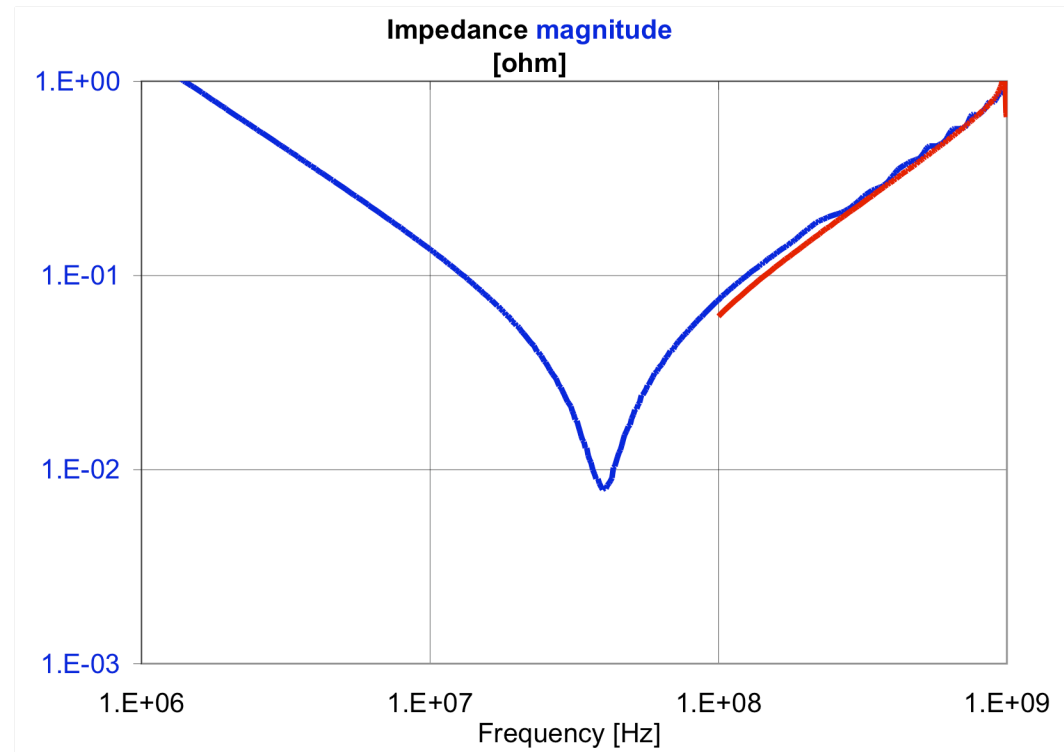
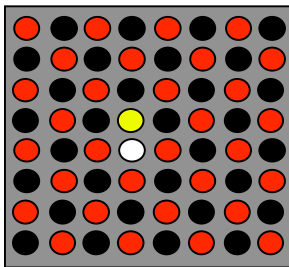
a1,b1



blue is measured
red is solver

Simulation vs. Measurement

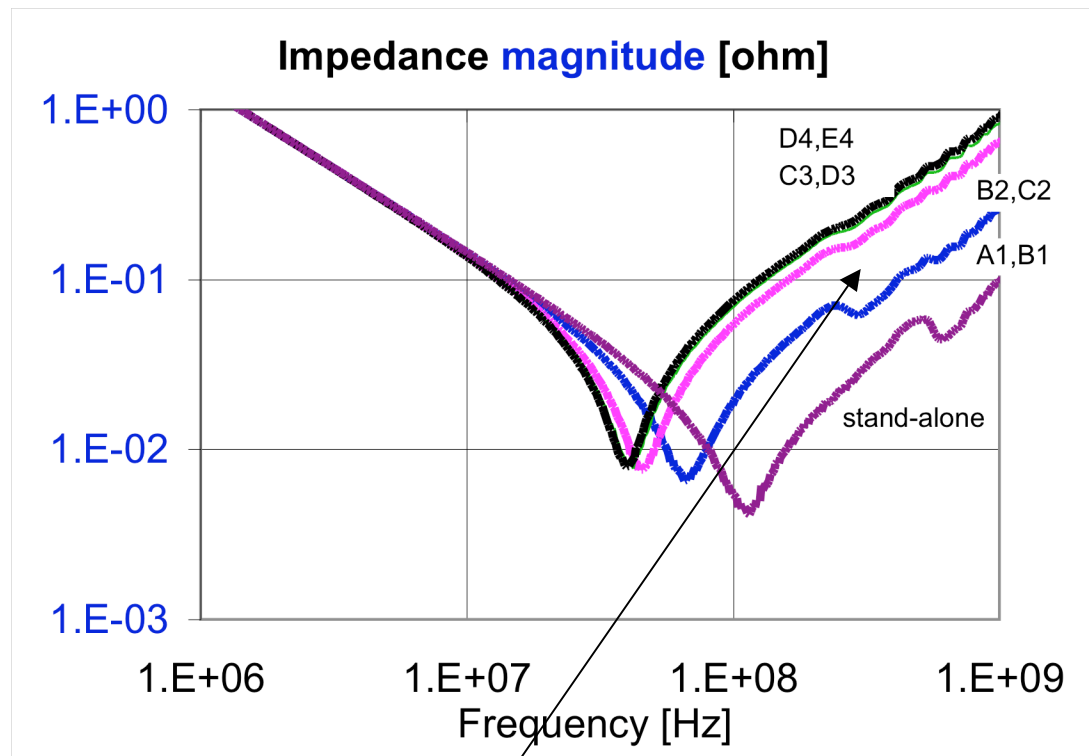
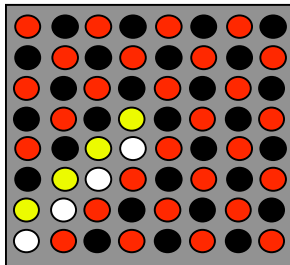
d4,e4



blue is measured
red is solver

Measurements on the Diagonal (1/3)

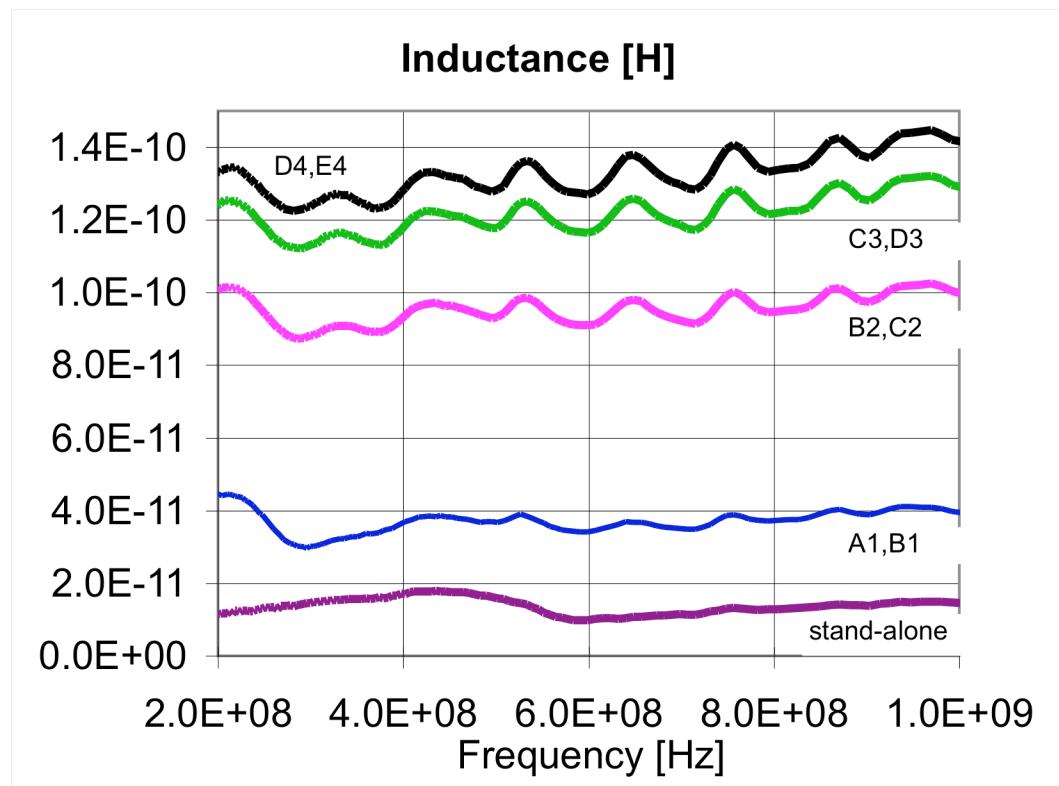
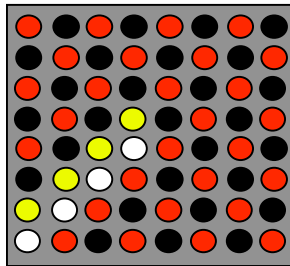
d4,e4
c3,d3
b2,c2
a1,b1



Impedance increases moving towards center

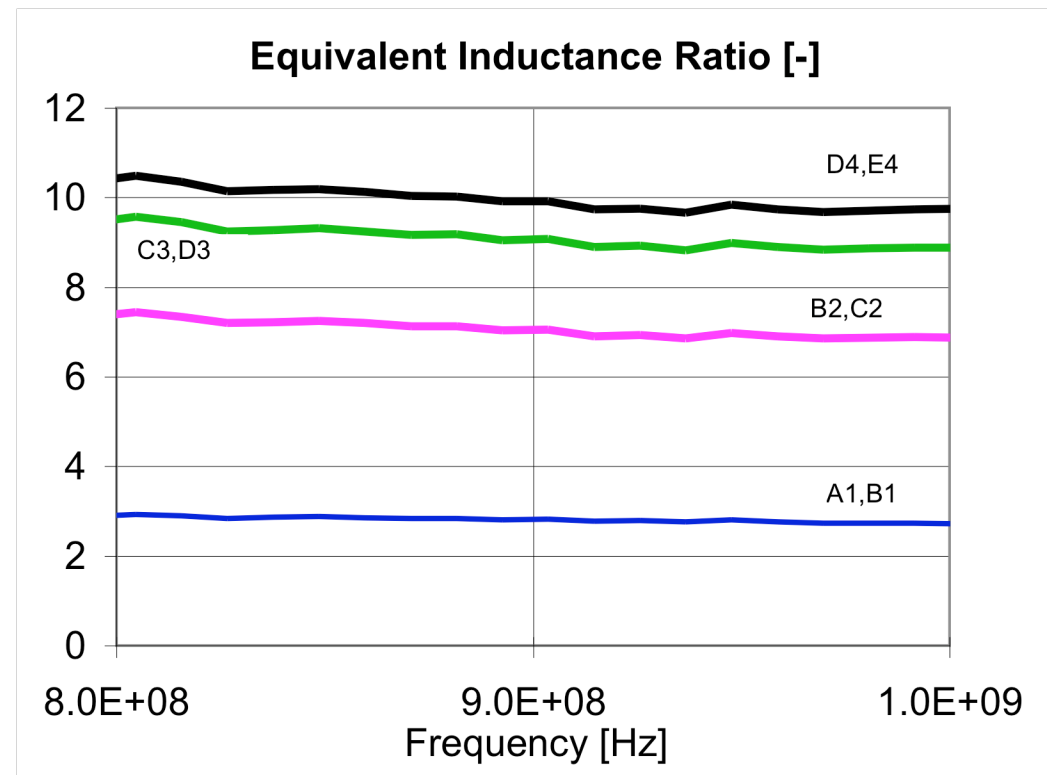
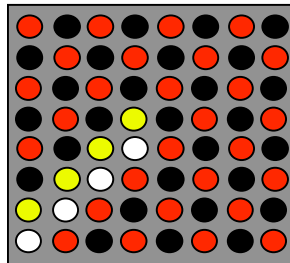
Measurements on the Diagonal (2/3)

d4,e4
c3,d3
b2,c2
a1,b1

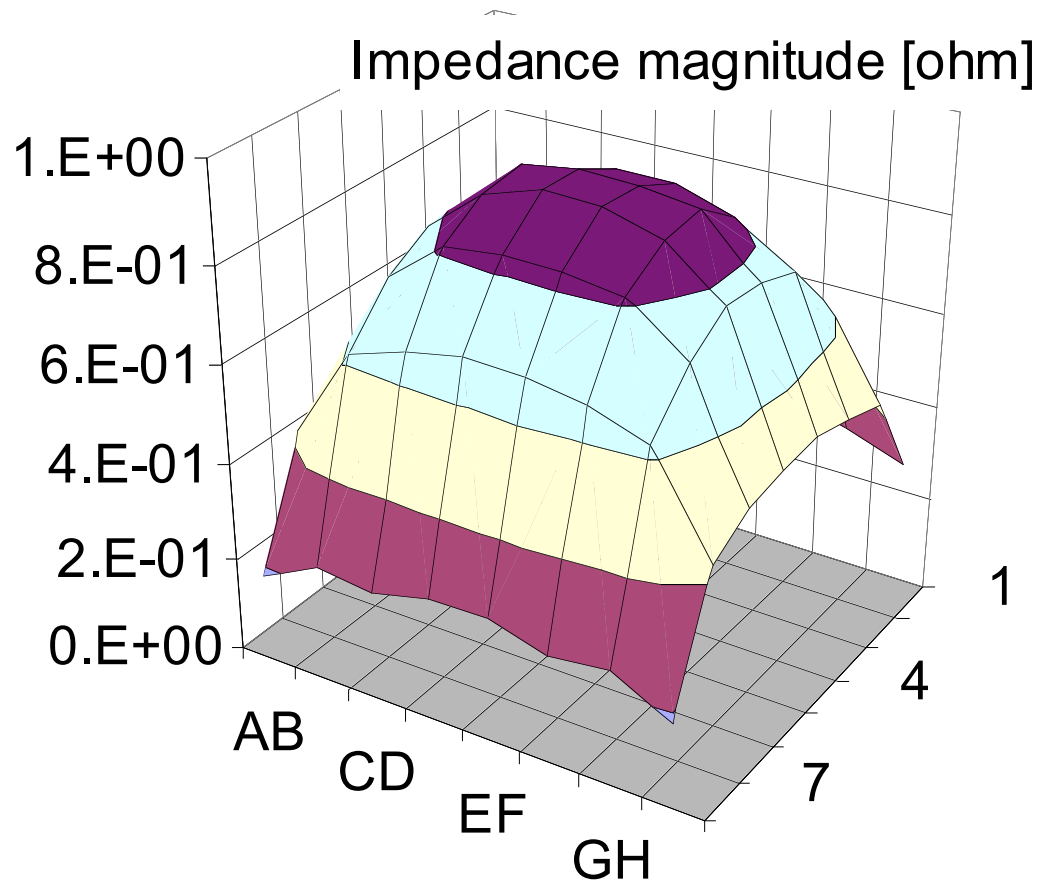


Measurements on the Diagonal (3/3)

d4,e4
c3,d3
b2,c2
a1,b1

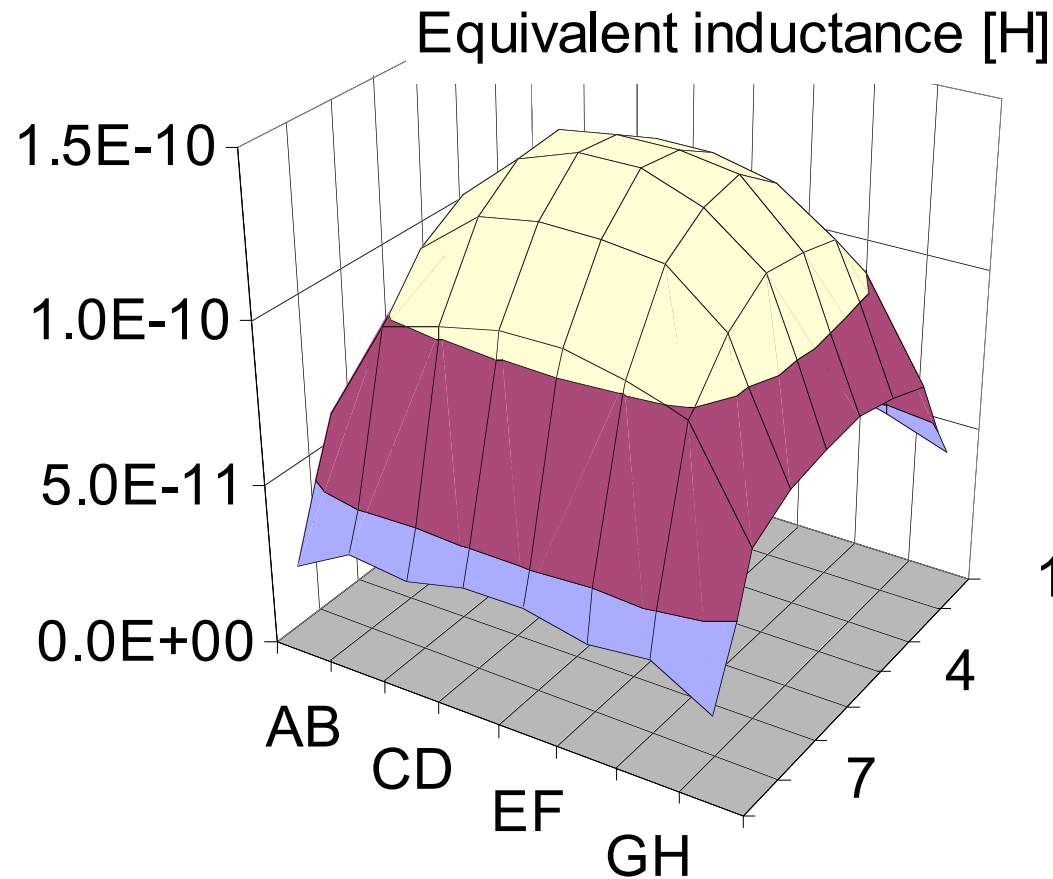


Full Matrix Measurement (1/2)



Measured impedance mag of entire array at 1 GHz.

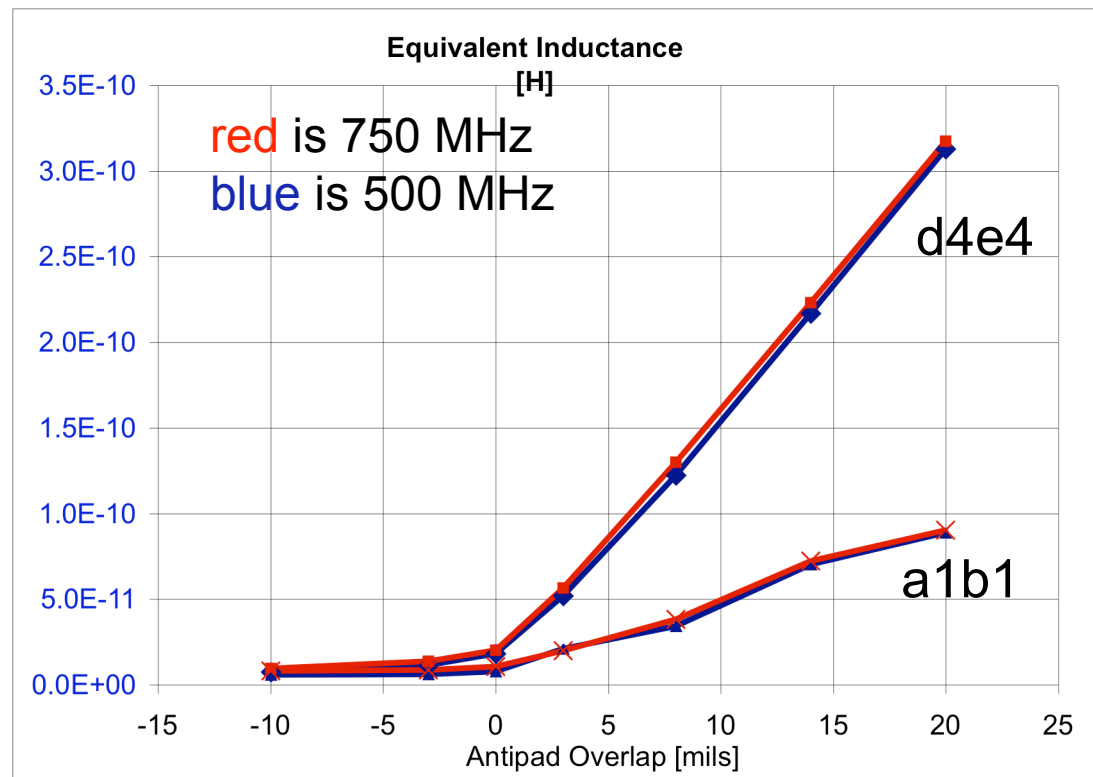
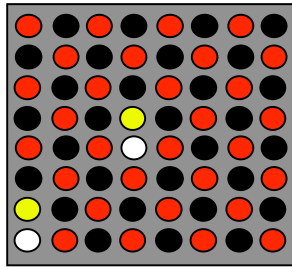
Full Matrix Measurement (2/2)



Equivalent inductance of entire array at 1 GHz.

Parameterization (1/3)

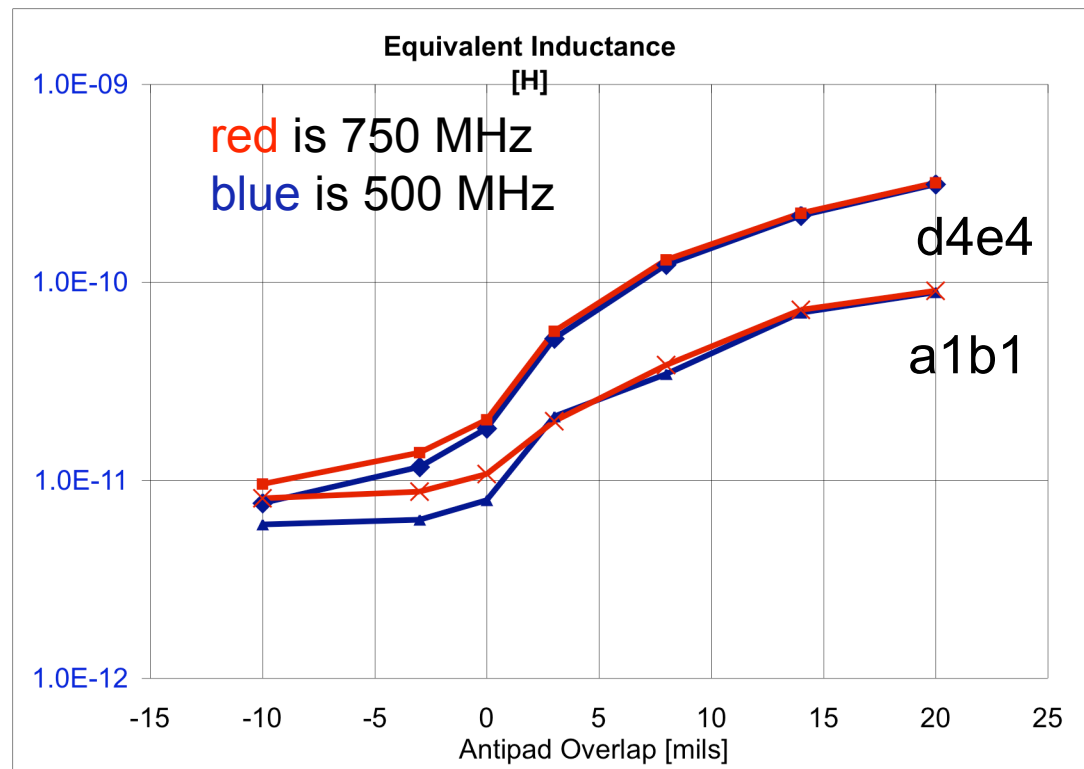
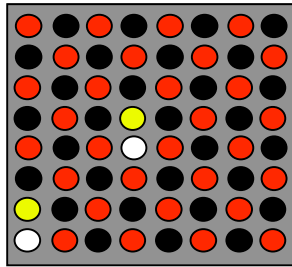
d4,e4
a1,b1



Simulated equivalent inductance at the two locations as a function of antipad overlap.

Parameterization (2/3)

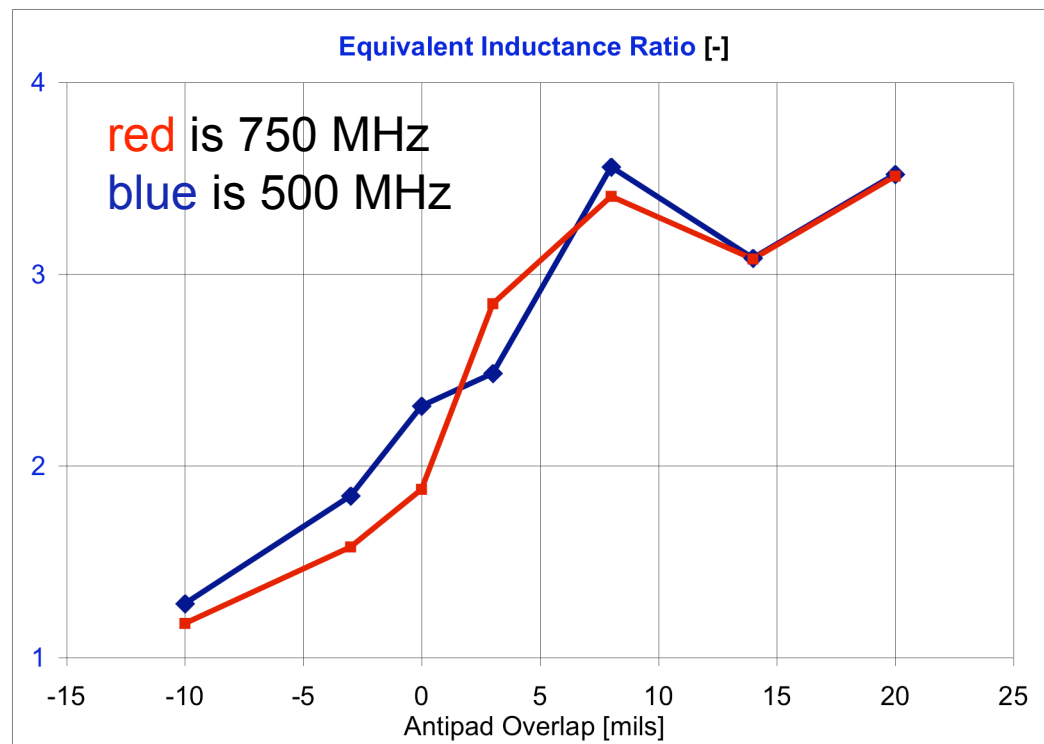
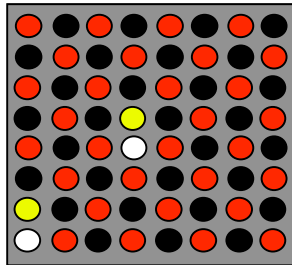
d4,e4
a1,b1



Simulated equivalent inductance at the two locations as a function of antipad overlap.

Parameterization (3/3)

d4,e4
a1,b1



Ratio of the inductance at the two locations as a function of antipad overlap.

Conclusions

- Measured and simulated data on via arrays showed that plane perforation can increase the impedance and inductance of via pairs within the array.
- Very good correlation was obtained between measurement and simulated data.
- The impedance in the array was found to be spatially dependent.
- It was shown that this variation is a strong function of antipad overlap. These results indicate that antipads in power/ground via arrays should not overlap in order to reduce the impedance and maintain a more uniform impedance across the array.

References

- Hyungsoo Kim, Jinguok Kim, Youchul Jeong, Jongbae Park and Joungho Kim, *Analysis of Via Distributions Effect on Multi-layered Power/Ground Transfer Impedance of High Performance Packages*, Proceedings of the 11th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 171-178, Oct. 2002.
- Zhiping Yang, Jim Zhao, Sergio Camerlo, and Jiayuan Fang, *Impact and Modeling of Anti-Pads on Power Delivery System*, Proceedings of the 12th Topical Meeting on Electrical Performance of Electronic Packaging, pp. 117-120, Oct. 2003.
- Istvan Novak, *Measuring MilliOhms and PicoHenrys in Power Distribution Networks*, DesignCon2000, Feb. 2000.