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Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination

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Abstract:
Power and ground planes should exhibit low impedance over a wide range of frequencies. Parallel ground and power planes in multilayer printed-circuit boards exhibit multiple resonances which increase the impedance and also the radiation from the edge of the board. Resistive termination along the board edges reduces the resonance peaks. Simple and straightforward design expressions, simulated self and transfer impedances, as well as measured impedance and radiation plots are presented for a pair of ten inch by ten inch pair of planes with 31mil FR4 dielectrics.

Introduction

With increasing clock speeds and decreasing supply voltages, the transient current injected into the power and ground planes of printed-circuit boards (PCB) is growing rapidly [1]. The transient current entering the planes have two sources: a) current spikes resulting from the switching activity of the silicon core and I/O cells, and b) signal return current associated with the signals through the system interconnects. While the first kind of transient current may be reduced and decoupled from the planes by adding capacitance locally to the silicon and/or making use of the package power-pin inductances, the return current of the high-speed signals is always present as long as single-ended signaling is used. To maintain signal integrity at high speeds, the power-distribution planes must exhibit a low enough impedance over the full bandwidth of signals, such that the simultaneously switching signals do not generate a plane shift which exceeds a predefined limit.

Power and ground plane characterization

The power and ground planes in a multilayer PCB may be considered as two-dimensional transmission lines. The impedance of a pair of circular parallel discs can be calculated analytically as shown in [2]. On the other hand, PCBs are rarely round shaped. Impedances of square-shaped parallel planes are widely analyzed in the literature for printed antennas. Analytical formulation is given, e.g. in [3].

In a heuristic approach ([4], [5]), the low-frequency equivalent components of the planes can be derived from a quasi-static model. For every unit square of the planes with side dimension of *w*, separation of *h*, the C_u static plane capacitance and t_{pd_u} propagation delay along the edge are:

$$C_u = e_0 e_r \frac{w^2}{h}, \qquad t_{pd\_u} = \frac{w\sqrt{e_r}}{c}$$

From the capacitance and delay, the equivalent Z_{ou} characteristic impedance and L_u inductance of the planes can be calculated:

$$Z_{0u} = \frac{t_{pd\_u}}{C_u} = 120p \frac{h}{w\sqrt{e_r}}, \qquad L_u = \frac{Z_0}{t_{pd\_u}} = m_0 h$$

In the above expressions all input and output parameters are in SI units, c = $3\text{x}10^8$ [m/sec] is the speed of light in vacuum, $\mu_o = 4\pi 10^{-7}$ [H/m] is the permeability of vacuum.

The capacitance of the planes with FR4 dielectric amounts to an about 500pF/inch^2 capacitance with 2 mil separation, and L_u = 63pH. For a plane size of ten inch by ten inch square, Z_{0u} = 0.035 ohms. Usually the innerplane capacitance is small compared to the total bypassing needs, but the capacitance exhibits low inductance. Note that L_u does not depend on the plane dimensions, only on the separation of planes.

Unfortunately, as it can be intuitively expected, the open boundaries at the periphery of planes create standing waves, which in turn show up in the impedance profile of the planes as peaks and valleys at higher frequencies. With open edges, frequencies of minima in the impedance profile depend on the location of sensing points (multiples of quarter-wave resonances), while maxima are determined by the dimensions of planes (multiples of half-wave resonances). The open structure also raises the concern of EMI/EMC radiations, see e.g., [6].

Dissipative edge termination

To make use of the low-inductance bypass capacitance formulated by the PCB planes, but at the same time reducing the concerns of standing waves and edge radiation, different techniques can be used to suppress the standing waves. The inherent dielectric losses of FR4 and alike materials together with the copper losses do help to some extent [3], but those wont reduce resonances sufficiently. In other solutions highly lossy dielectric materials are used ([7], [8]). The standing waves can also be reduced by selecting a proper reactive (capacitive) termination along the PCB edges [9]. By using the one-dimensional transmission-line analogy, one can reduce the standing waves by putting resistive termination along the open edges, for instance connecting a termination resistance of $R_t = Z_{ou}$ value at every *w* spacing along the board edges.

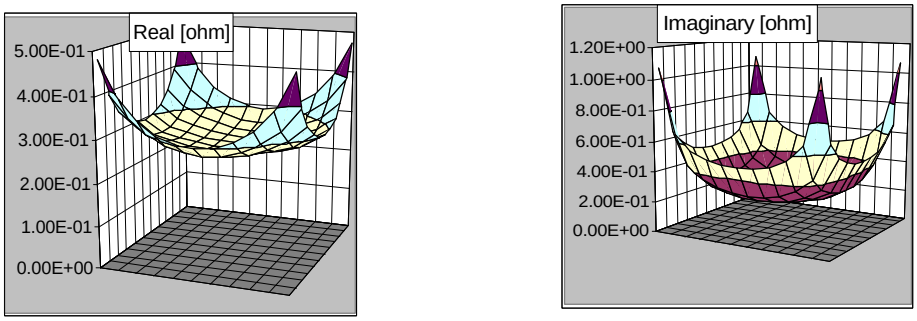
Since power and ground planes carry different DC voltages, a C_t DC blocking capacitor is also required in series of the termination resistance. In this discrete implementation, the L_t interconnecting inductance from the R_t and C_t components on the surface of the board going to the planes will eventually limit the effectiveness of the termination at higher frequencies. To achieve effective termination up to a predefined f_0 frequency limit, we must ensure that the *w* spacing between the termination components along the edge is set to the smaller of the following two limits:

a) the discrete terminations will approximate a continuous termination network as long as the *w* spacing is less than 10% of the wavelength at the highest (f_0) frequency, and
b) the ωL_t inductive reactance does not exceed R_t at the highest (f_0) frequency. Note that L_t is fixed and determined by the via and pad pattern, while R_t increases as the *w* spacing is reduced, thus making it possible to meet the goal over a wide range of input parameters.

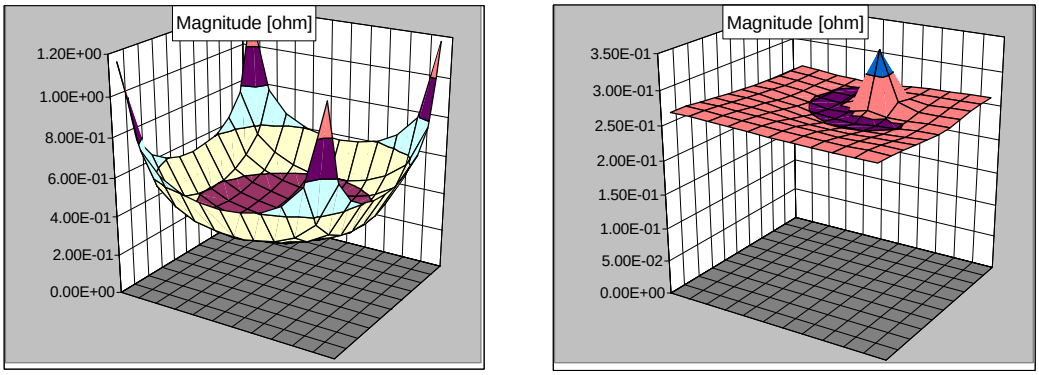
Once R_t and their *w* spacing are determined, the C_t DC blocking capacitor can be selected such that their corner frequency is lower than the lower self-resonance frequency of the planes.

Simulation model and results

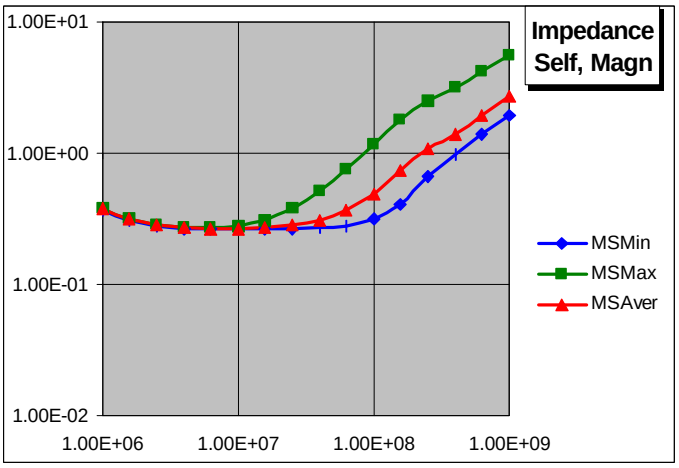
For a test device, a ten inch by ten inch square pair of planes with 31 mil FR4 dielectrics was selected. The DUT was simulated with a grid similar to what is described in [4] and [5]. The transmission-line grid size was set to one inch, and for the sake of simplicity lossless Tlines were used. The figure below shows the simulated self-impedance and trans-impedance profile of the terminated plane.



Simulated real and imaginary part of the self-impedance profile at 100MHz. The impedances are plotted at every inch of the grid.



Magnitude of self-impedance (on the left) and transfer-impedance (on the right) plots at 100MHz. The transfer impedance is shown from 3 inches and 4 inches away from the corner, where the peak of the impedance profile occurs.



Minimum, average and maximum values of the simulated self-impedance magnitudes (in ohms) over the planes at various frequencies (in Hertz).|

Measurement results

The DUT described above was measured with a HP8720D vector-network analyzer (VNA). Self and transfer impedances of the plane with and without edge termination were measured with the VNA connected in a four-node arrangement. Radiation from the edges were measured with the VNA source connected to the center of the planes, whereas the receive port of VNA was connected to the output of a HP11904 close-field probe.

References:

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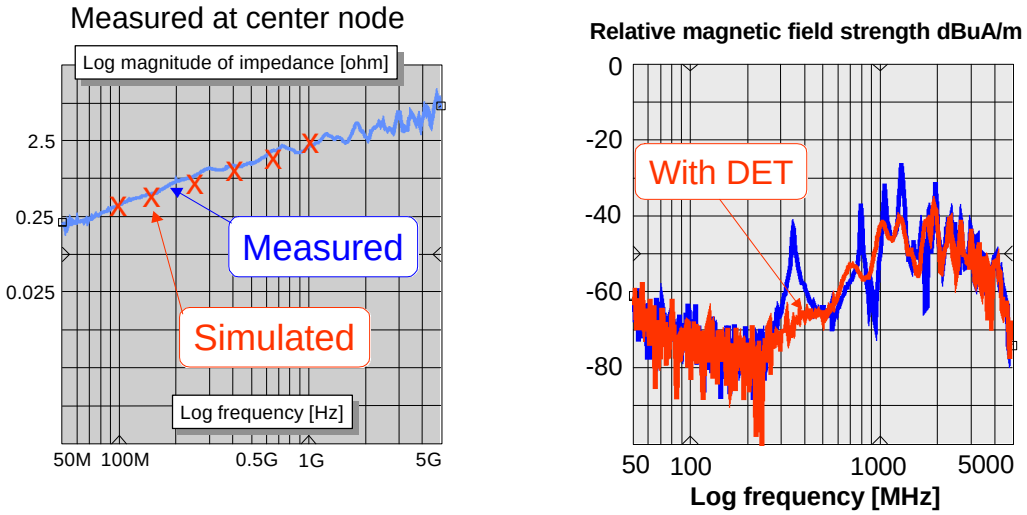

On the left, comparison of measured and simulated self-impedance magnitude values of DUT at the center of the planes. On the right, comparison of measured edge radiation with and without edge termination.