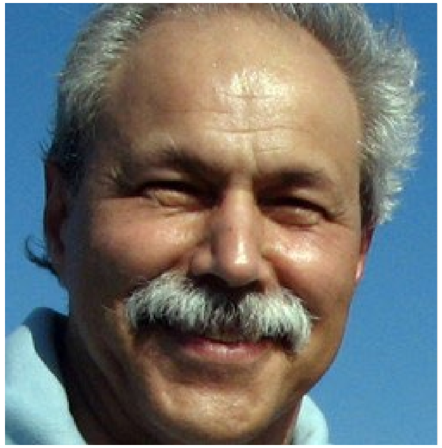
PI Challenges and Potential Solutions in the Age of AI and How They Relate to EMC

Istvan Novak, Samtec

September 24, 2025

Boxboro, MA

Speaker



Istvan Novak

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Istvan works on advanced SI/PI designs at Samtec and was previously a Distinguished Engineer at SUN later Oracle. He introduced the first 25µm power-ground laminates for large rigid PCBs and worked to create a series of low inductance, controlled-ESR capacitors. He is a Life Fellow of the IEEE with 25 patents, author of two books on PI, teaches SI/PI courses, and maintains a popular SI/PI website. He was named Engineer of the Year at DesignCon 2020.

Abstract

The power-hungry AI (Artificial Intelligence) and ML (Machine Learning) chips create new and unique Power Integrity (PI) challenges, which cannot be solved by traditional tools, materials and technologies. The kA current consumption together with the continued growth of the number of independent power supply rails requires multiple power planes in printed circuit boards (PCBs), which many times increases the total thickness to unmanageable levels and can cause Electromagnetic Compatibility (EMC) issues. Similarly, validation of the PDN becomes very challenging, since the equivalent power distribution network (PDN) impedance drops to tens of microohms, rendering the traditional PDN validation methods, whether attempted in the frequency or time domain, useless. This talk will illustrate and explain these challenges and will look at some of the possible solutions.

Outline

- Introduction: a personal history with EMC
- The Context: EMC vs. SI/PI
- Functions of PDN
- A Brief History of PDN
- Current PI Components and Technologies
- The Evolving Challenge
- The paradigm shift
- EMC Impact of PDN Noise on SerDes Signals
- Challenge: Increased Dynamic Range
- Potential solutions
  - Vertical PDN
  - HDI, thin laminates
  - Improved PDN impedance measurements and simulations
  - Open-source projects
- Summary

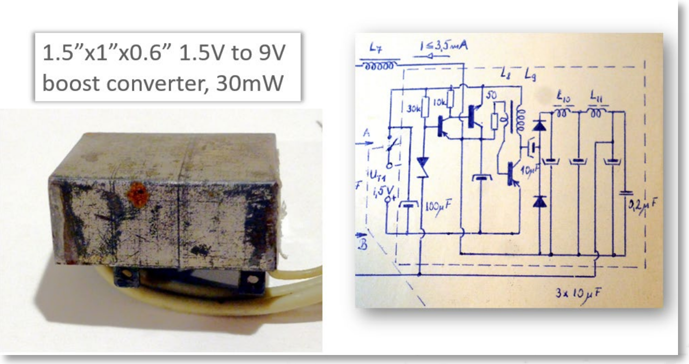
Introduction

A personal history with EMC

Background info on speaker (1)

- Hobby project
- Late 1960’s

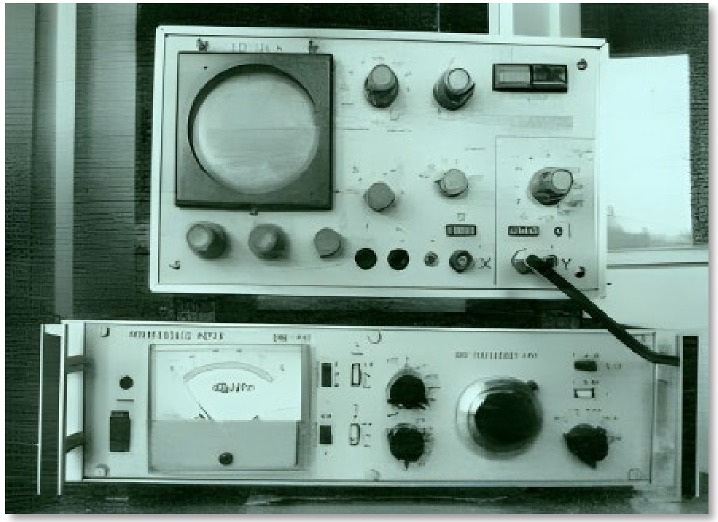
“Bypass Capacitor Requirements for Server Applications,” Kemet Technology Forum, May 2007



1.5”x1”x0.6” 1.5V to 9V boost converter, 30mW

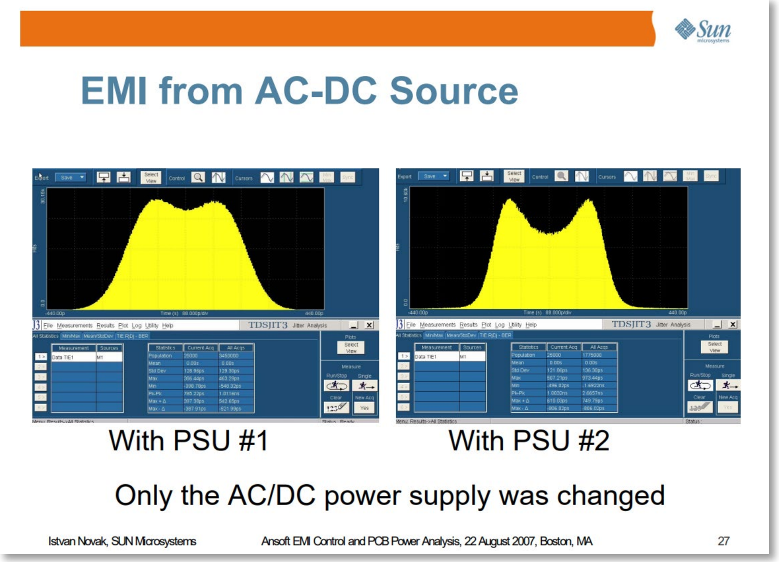
“Why We Love (and Hate) DC-DC Converters?,” CDNLive, Burlington, MA, August 2016

AM broadcasting interference measurements, late 1970s



Mihaly Narancsik, “History of radio monitoring station at Tarnok, 1924-2024“. Original: “Tárnok vevő és mérőállomás története a kezdetektől napjainkig 1924-2024,” 2024, in Hungarian

In-system interference, late 2000s



EMI from AC-DC Source

With PSU #1 With PSU #2

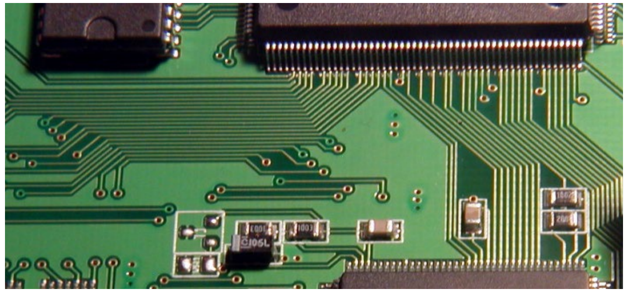
Only the AC/DC power supply was changed

Istvan Novak, SUN Microsystems Ansoft EMI Control and PCB Power Analysis, 22 August 2007, Boston, MA 27

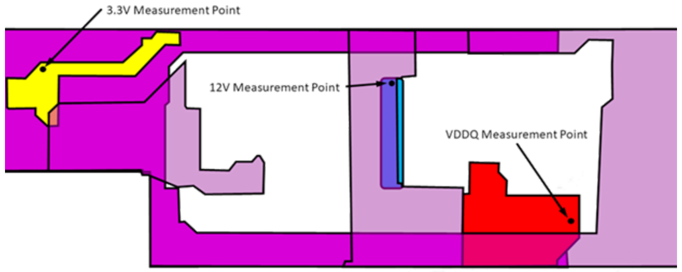
“Reducing EMI Noise by Suppressing Power-Distribution Resonances,” Ansys EMI meeting, August 2007, Boston, MA

The Context: EMC vs. SI/PI

- In a traditional view, the three disciplines are applied independently
- SI: 1D wave propagation effects
    - Reflections, termination, crosstalk



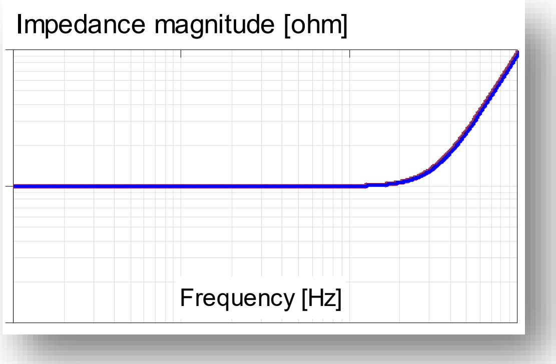
- PI: 2D and 2.5D wave propagation effects
    - Plane resonances, SSN due to via inductance



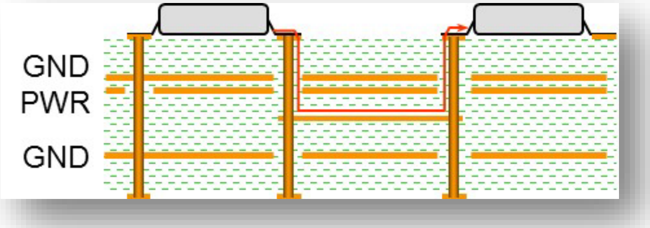
- EMI: 3D wave propagation effects
    - EM interaction through distance (out-of system or unknown source and/or victim)

Functions of PDN

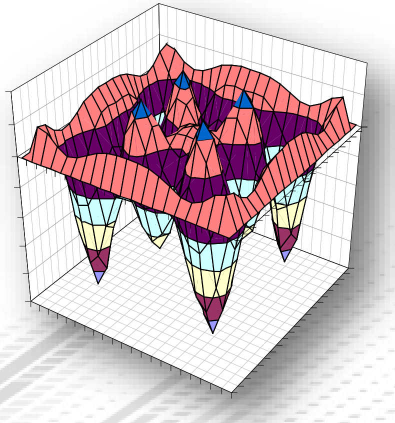
- Providing clean power to electronics (PI)
  - Key: proper impedance profile



- Provide solid return path for signals (optional), (SI)
  - Key: proper stackup

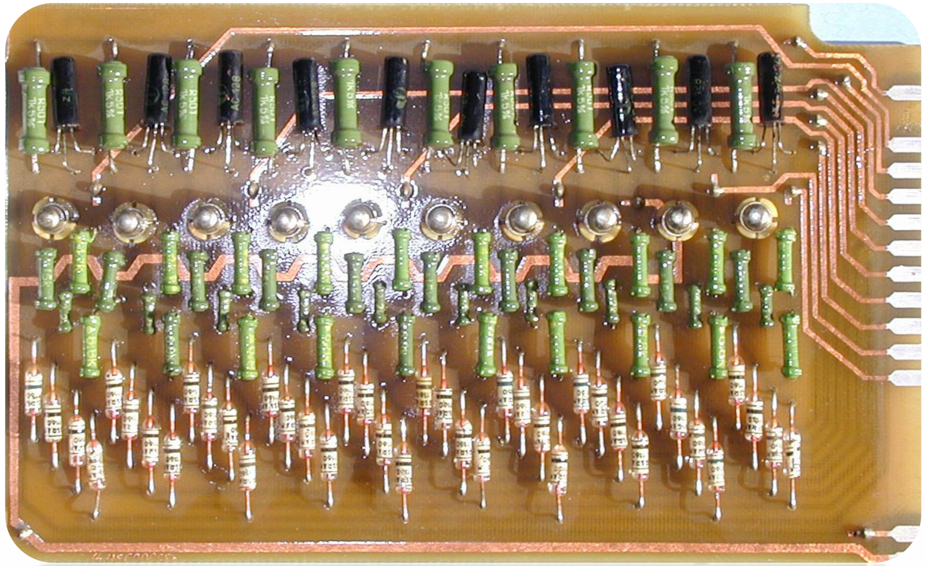


- Keep radiation and immunity from PDN within spec'd limits (EMI)
  - Key: resonance-free PDN structure

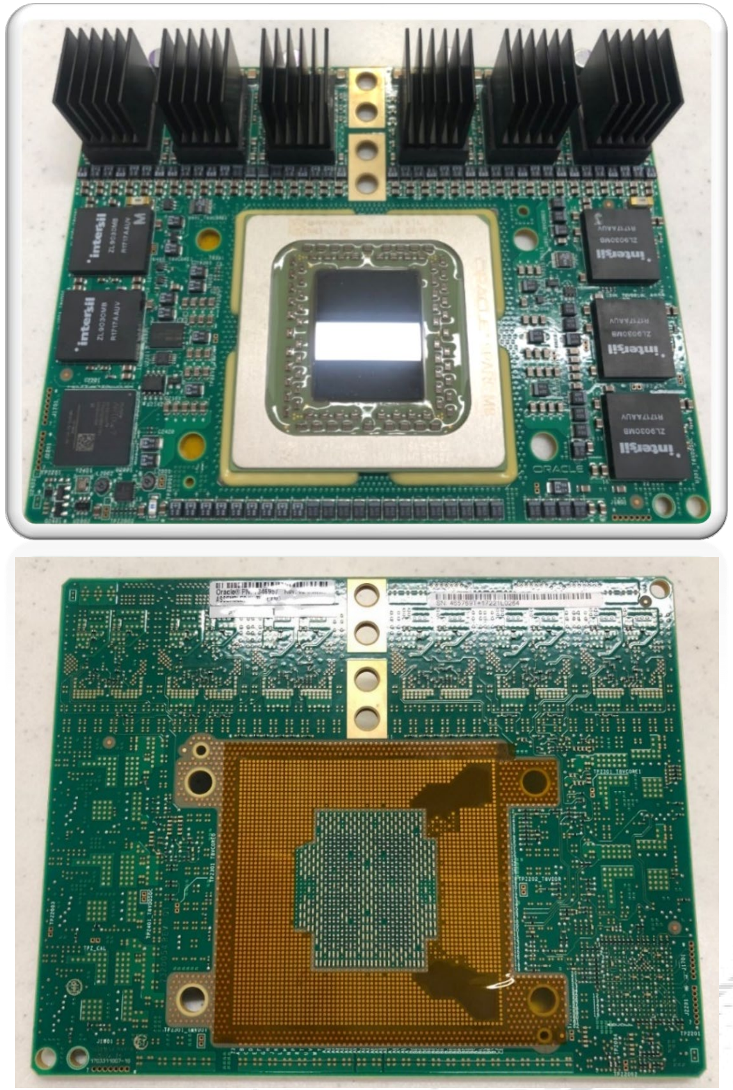


A Brief History of PDN

1970s:
DTL logic board, no bypass capacitors

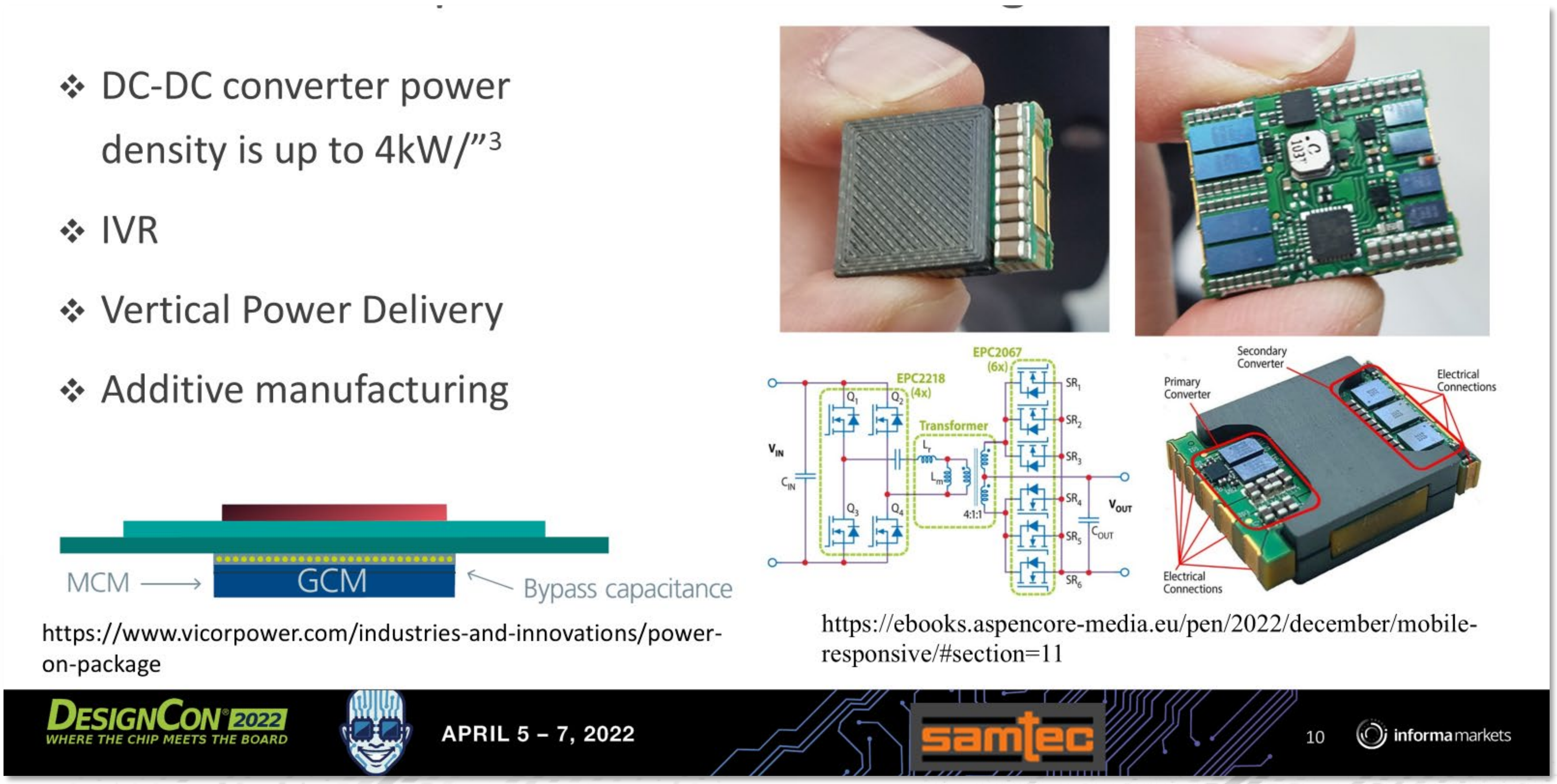


2010s:
Oracle/SUN T8/M8 CPU module
637 bypass capacitors



“The Future of Power Integrity Through the Eyes of Experience,” DesignCon 2023

Current PI Components and Technologies



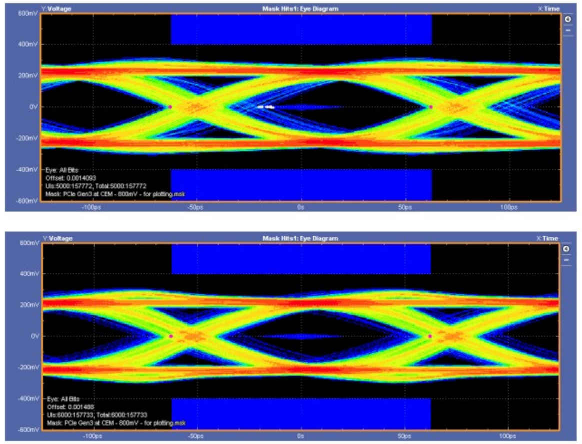
- DC-DC converter power density is up to 4kW/”^{3}
- IVR
- Vertical Power Delivery
- Additive manufacturing

https://www.vicorpower.com/industries-and-innovations/power-on-package

https://ebooks.aspencore-media.eu/pen/2022/december/mobile-responsive/#section=11

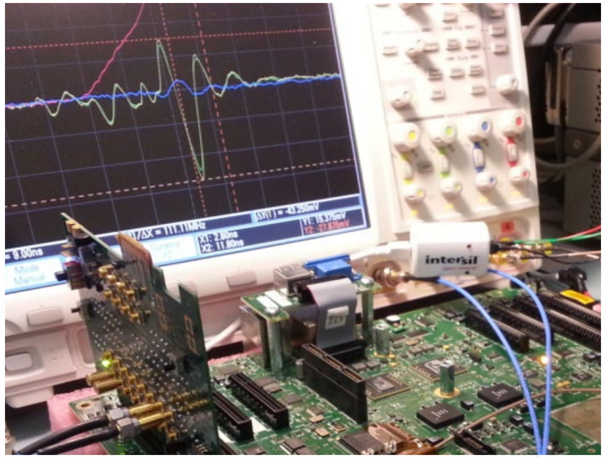
The Evolving Challenge

In-system PCI-E interference from DC-DC converter, late 2010s



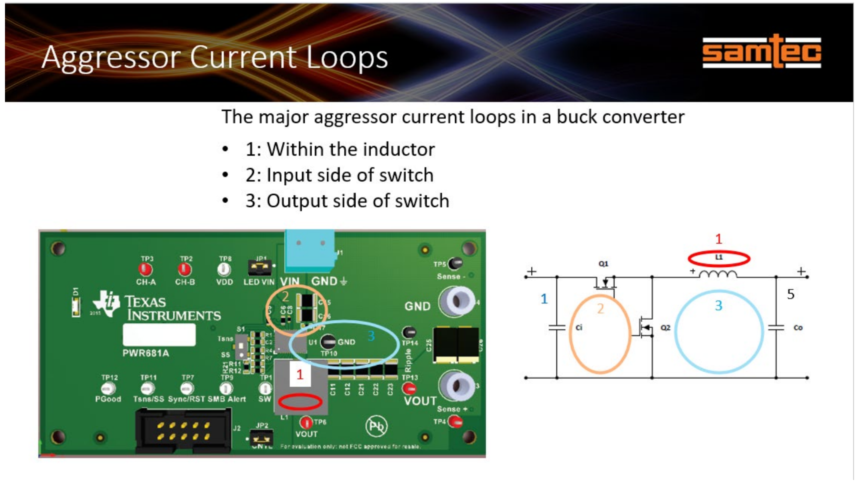
Eye: All Bits
Offset: 0.0014093
UIs:5000:157772; Total:5000:157772
Mask: PCIe Gen3 at CEM - 800mV - for plotting.msk

Eye: All Bits
Offset: 0.001488
UIs:6000:157733; Total:6000:157733
Mask: PCIe Gen3 at CEM - 800mV - for plotting.msk



"Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals," DesignCon 2017

In-system DC-DC to SerDes interference, 2020s



Aggressor Current Loops

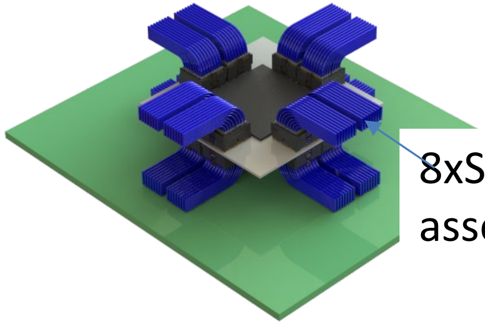
The major aggressor current loops in a buck converter

- 1: Within the inductor
- 2: Input side of switch
- 3: Output side of switch

DC-DC Converter Inductors

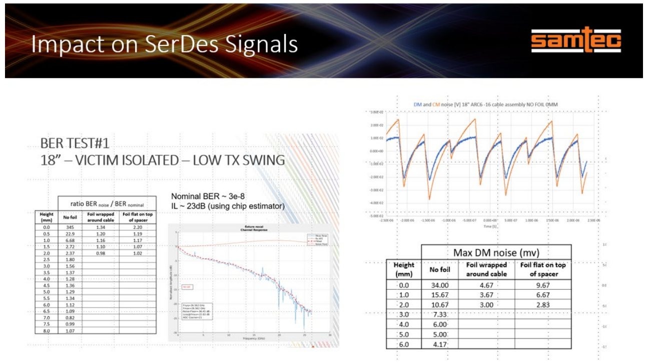
Flux in inductors with cores is the highest near the air gap

Substrate size:
Up to 100mm X 100mm



8xSerDes cable assemblies

"The Future of Power Integrity Through the Eyes of Experience," DesignCon 2023



Impact on SerDes Signals

BER TEST#1
18" – VICTIM ISOLATED – LOW TX SWING

	ratio BER noise / BER nominal		
Height (mm)	No foil	Foil wrapped around cable	Foil flat on top of spacer
0.0	345	1.34	2.20
0.5	22.9	1.20	1.19
1.0	6.68	1.16	1.17
1.5	2.72	1.10	1.07
2.0	2.37	0.98	1.02
2.5	1.80		
3.0	1.56		
3.5	1.37		
4.0	1.28		
4.5	1.36		
5.0	1.29		
5.5	1.34		
6.0	1.12		
6.5	1.09		
7.0	0.82		
7.5	0.99		
8.0	1.07		

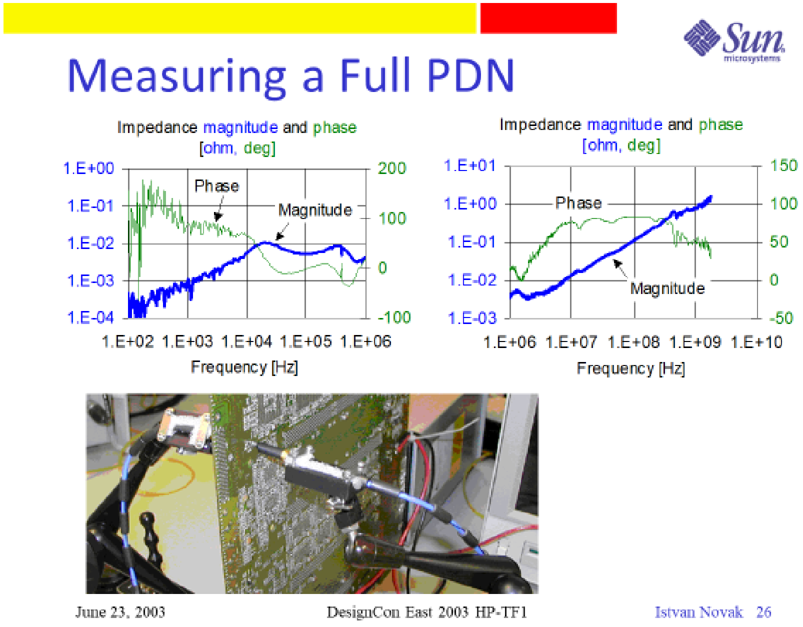
Nominal BER ~ 3e-8
IL ~ 23dB (using chip estimator)

	Max DM noise (mv)		
Height (mm)	No foil	Foil wrapped around cable	Foil flat on top of spacer
0.0	34.00	4.67	9.67
1.0	15.67	3.67	6.67
2.0	10.67	3.00	2.83
3.0	7.33		
4.0	6.00		
5.0	5.00		
6.0	4.17		

"SerDes CM Noise: How Much is Too Much?," gEEk spEEk, Samtec, May 2023

The Paradigm Shift

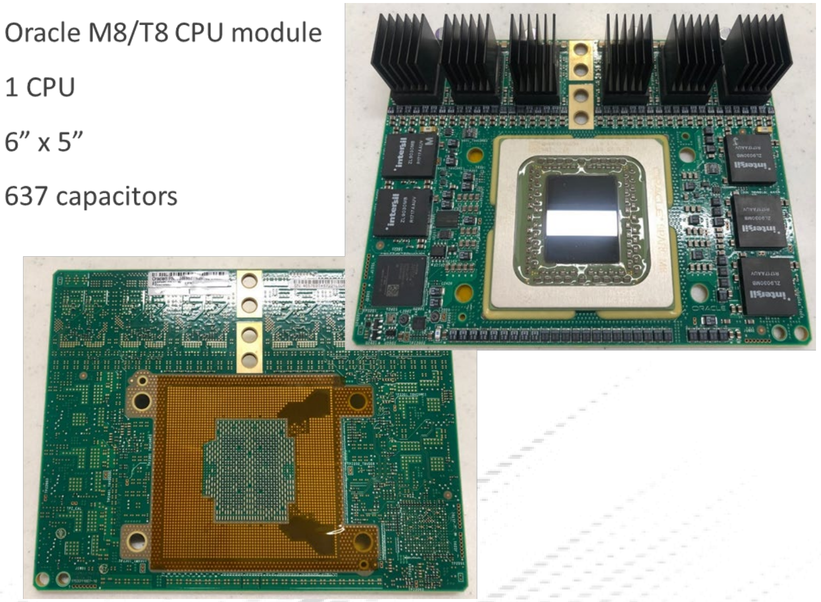
- Paradigm Shift #1: late 1990s
  - Requirements to measure milliohms
  - Frequency domain design and verification
  - Horizontal incremental impedance was relatively small
  - 3D interactions in PI measurements were small
  - **Solution: VNA with Two-port Shunt-through connection**
  - Frequency and time-domain verifications lined up
- Paradigm Shift #2: early 2020s
  - Requirements to measure microohms
  - 3D interactions in PI measurements become dominant
  - Horizontal incremental impedance becomes relatively high
  - Increasing gap between frequency and time-domain verification results
  - **Solution: ???**



Measuring a Full PDN

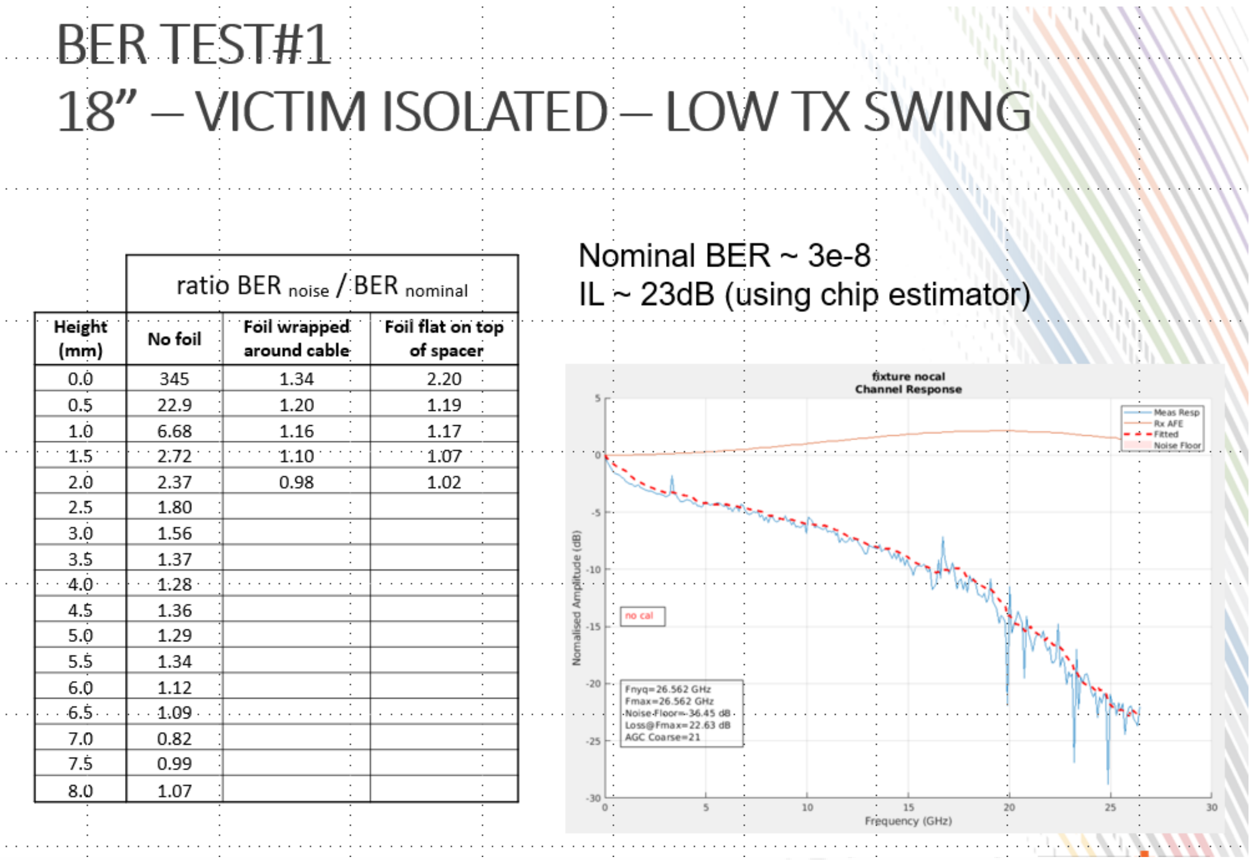
June 23, 2003 DesignCon East 2003 HP-TF1 Istvan Novak 26

- Oracle M8/T8 CPU module
- 1 CPU
- 6” x 5”
- 637 capacitors



From: Is Power Integrity the New Black Magic?
Cadence Design Forum, April 2021

EMC Impact of PDN Noise on SerDes Signals



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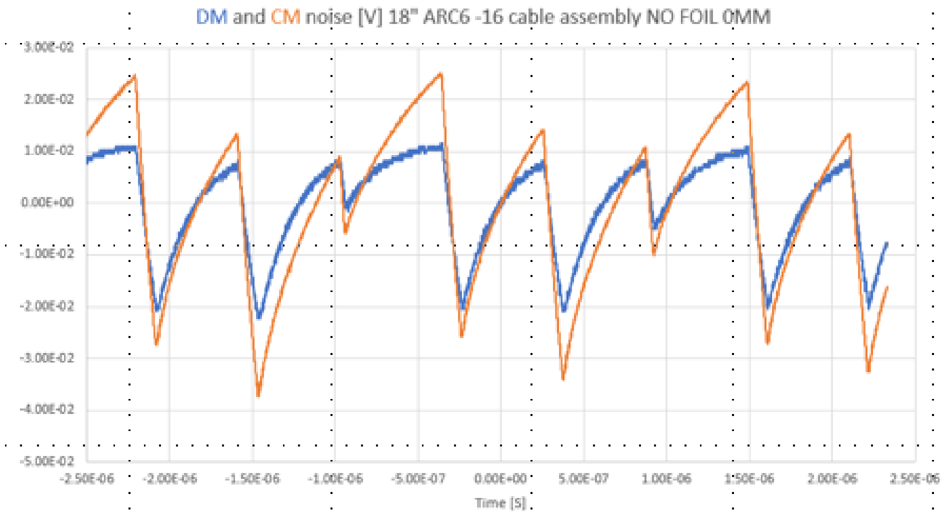

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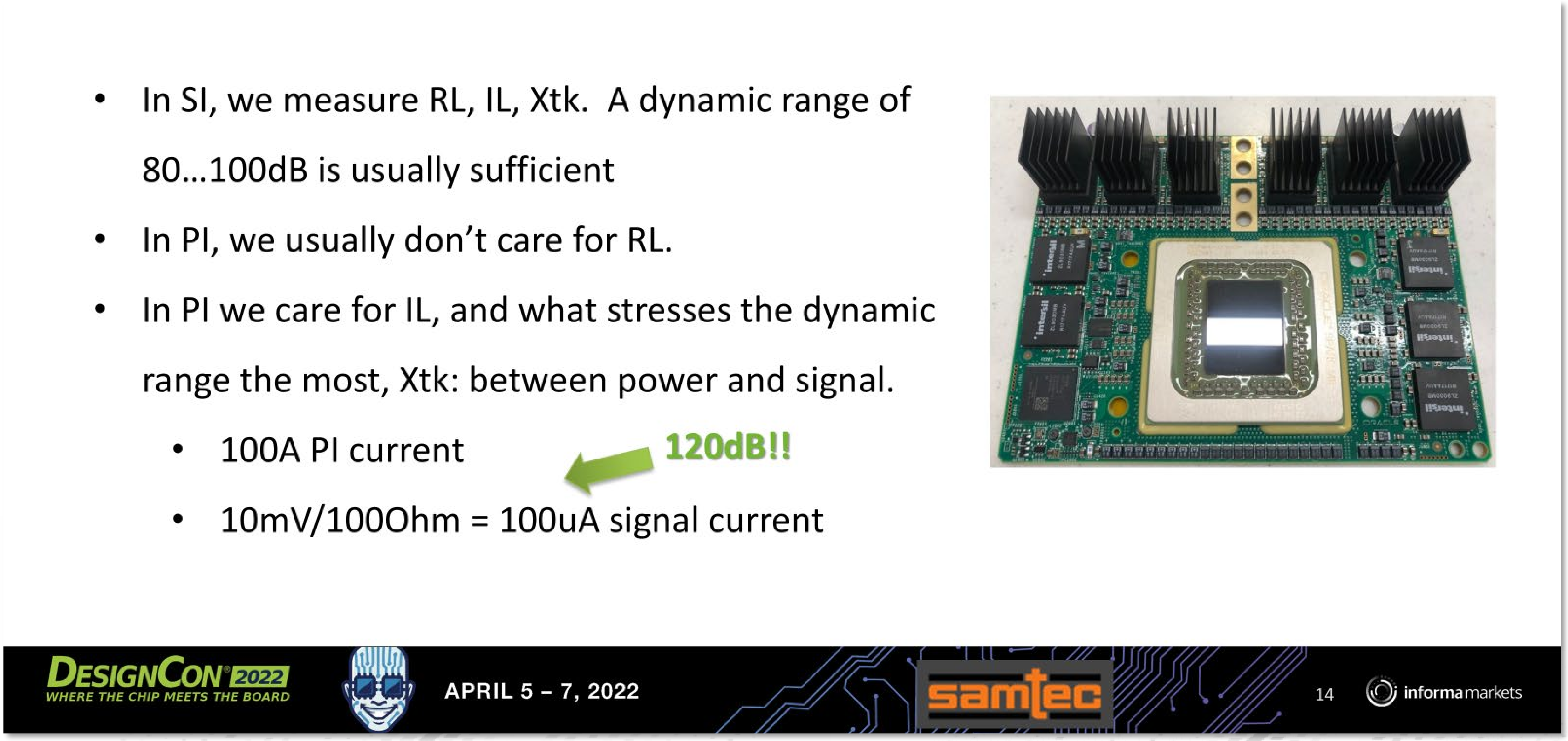
3.0	7.33		
4.0	6.00		
5.0	5.00		
6.0	4.17		

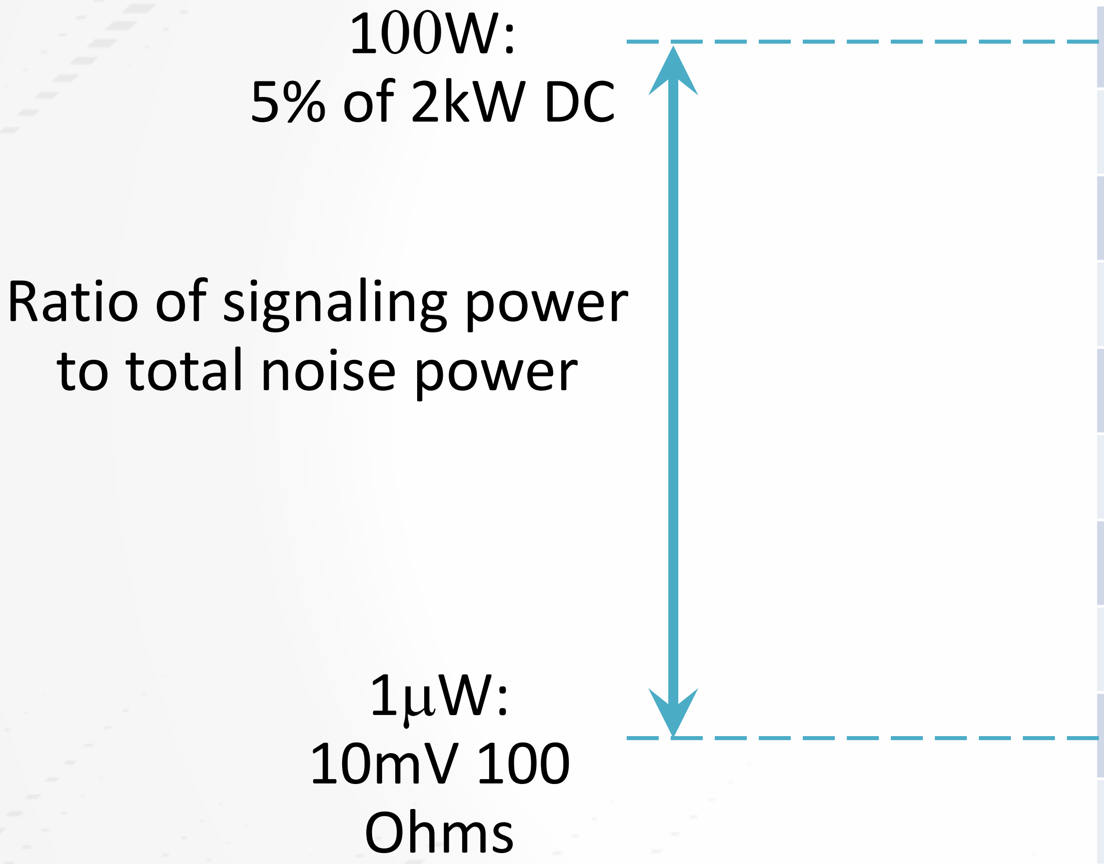
Challenge: Increased Dynamic Range



- In SI, we measure RL, IL, Xtk. A dynamic range of 80…100dB is usually sufficient
- In PI, we usually don’t care for RL.
- In PI we care for IL, and what stresses the dynamic range the most, Xtk: between power and signal.
  - 100A PI current
  - 10mV/100Ohm = 100uA signal current

120dB!!

The Source of the Challenge



100W:
5% of 2kW DC

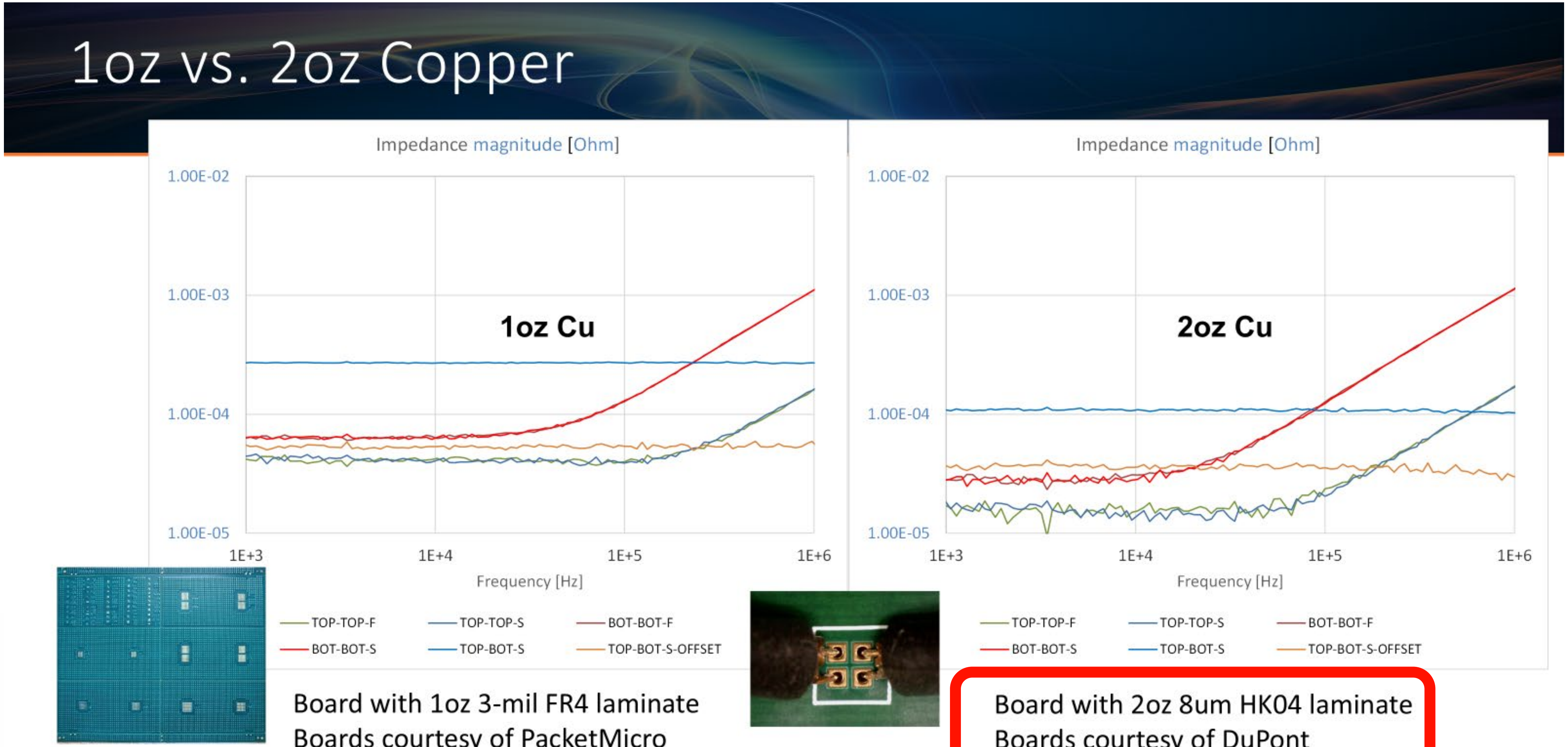
Ratio of signaling power
to total noise power

1μW:
10mV 100
Ohms

Sound sources (noise) Examples with distance	Sound pressure level dB
Threshold of discomfort	120
Airport	110
Underground train	100
Diesel truck, 10m	90
Curbside of busy road, 5m	80
Vacuum cleaner, 1m	70
Conversational speech, 1m	60
Average home	50
Quiet library	40
Quiet bedroom at night	30
Broadcast studio background	20

“Model Accuracy and Use Considerations,” DesignCon 2018

Potential Solutions: Improved Laminates

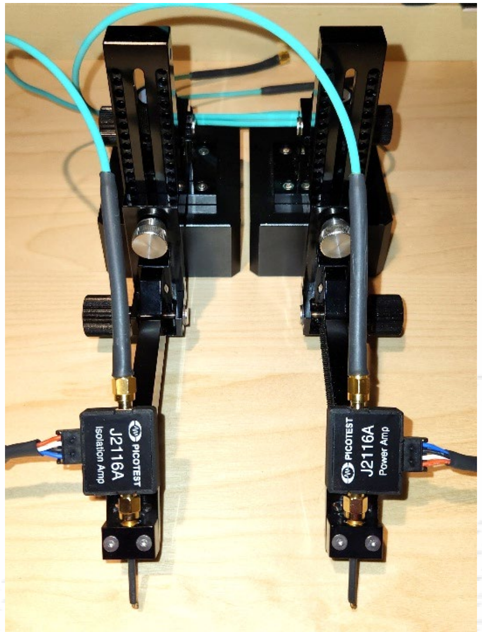


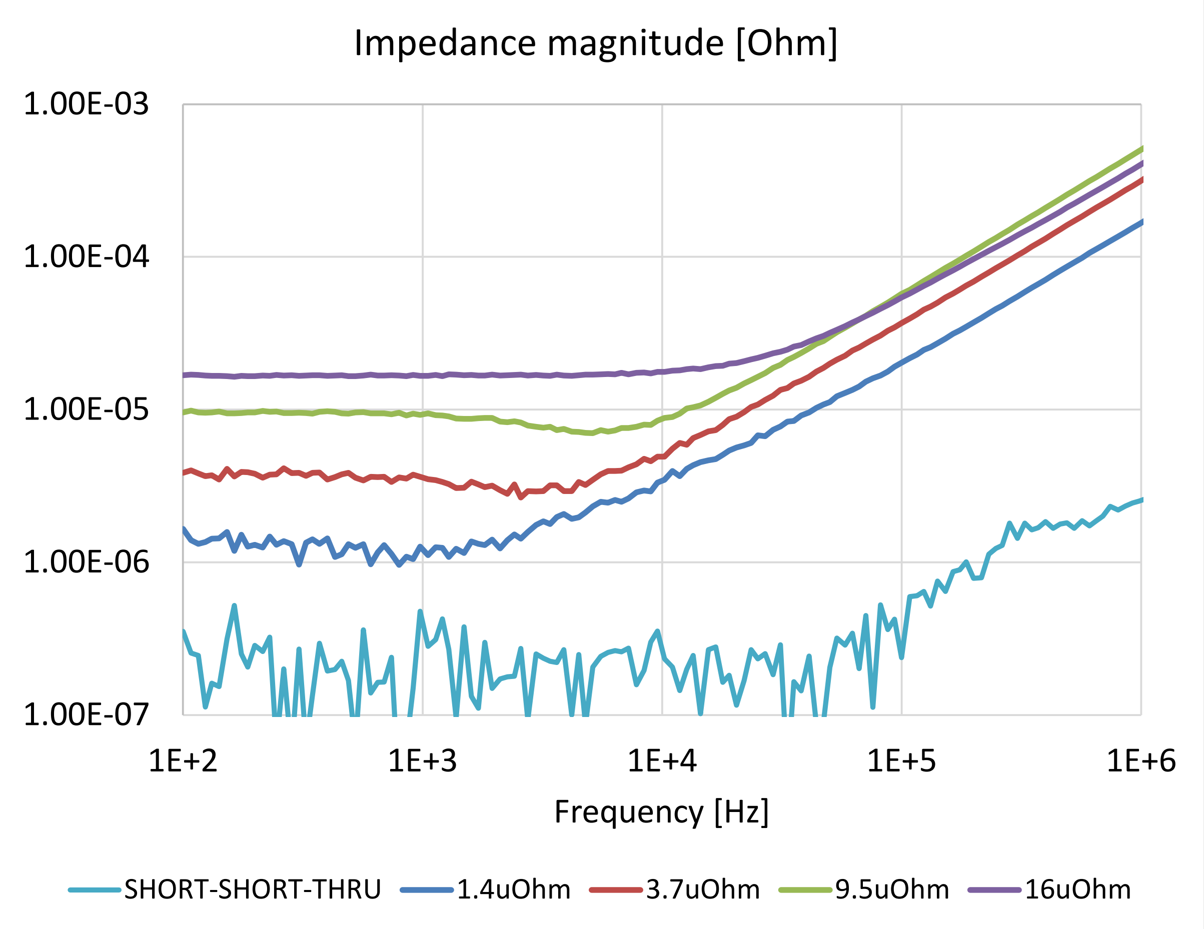
Board with 1oz 3-mil FR4 laminate
Boards courtesy of PacketMicro

Board with 2oz 8um HK04 laminate
Boards courtesy of DuPont

Potential Solutions: Improved PDN Design/Validation

- VNA: 1Hz IFBW
- 0dBm source power
- No averaging
- SOLT calibration (including Isolation)
- 20dB 20dBm power booster on Port1
- 20dB low-noise pre-amplifier on Port2





Summary, Conclusions

- Paradigm shift in PDN creates new EMC challenges
- The primary new EMC challenge: increased in-system interference
- Solution requires parallel effort in
  - PDN system design
  - Technologies
  - Design and validations

References

- “SerDes CM Noise: How Much is Too Much?,” gEEk spEEk, Samtec, May 2023
- “Model Accuracy and Use Considerations,” DesignCon 2018
- “Is Power Integrity the New Black Magic?,” Cadence Design Forum, April 2021
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- https://www.samtec.com/standards/ieee/
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