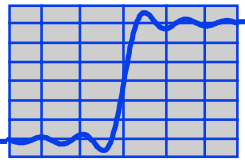
POWERING DIGITAL BOARDS

DISTRIBUTION AND PERFORMANCE

Istvan Novak, Signal Integrity Staff Engineer
SUN Microsystems, Inc.

Meeting of the Greater Boston Chapter
IPC Designer's Council
February 9, 1999



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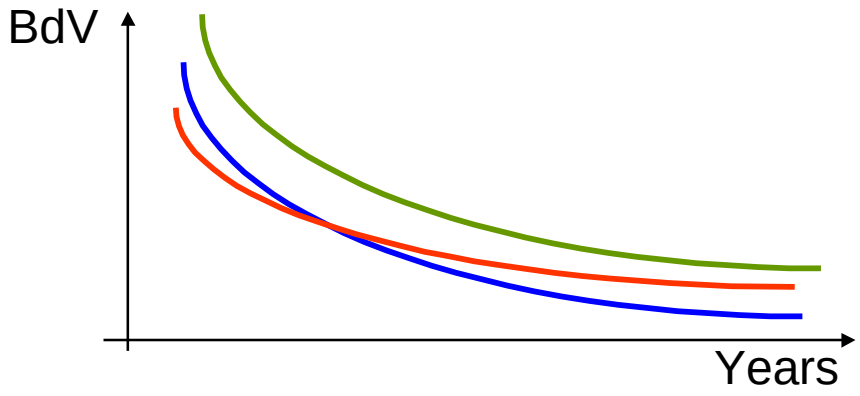
Proliferation of Supply Voltages

In CMOS devices, at every edge, power is dissipated
The power can be lowered by:

- lower capacitance
  (smaller feature size)
- lower voltage

$$E = \frac{1}{2}CV^2 \qquad P = fCV^2$$

With submicron feature sizes, the breakdown voltage is below 5 V.
Supply voltages in different circuits (core, IO, memory, etc) drop differently.



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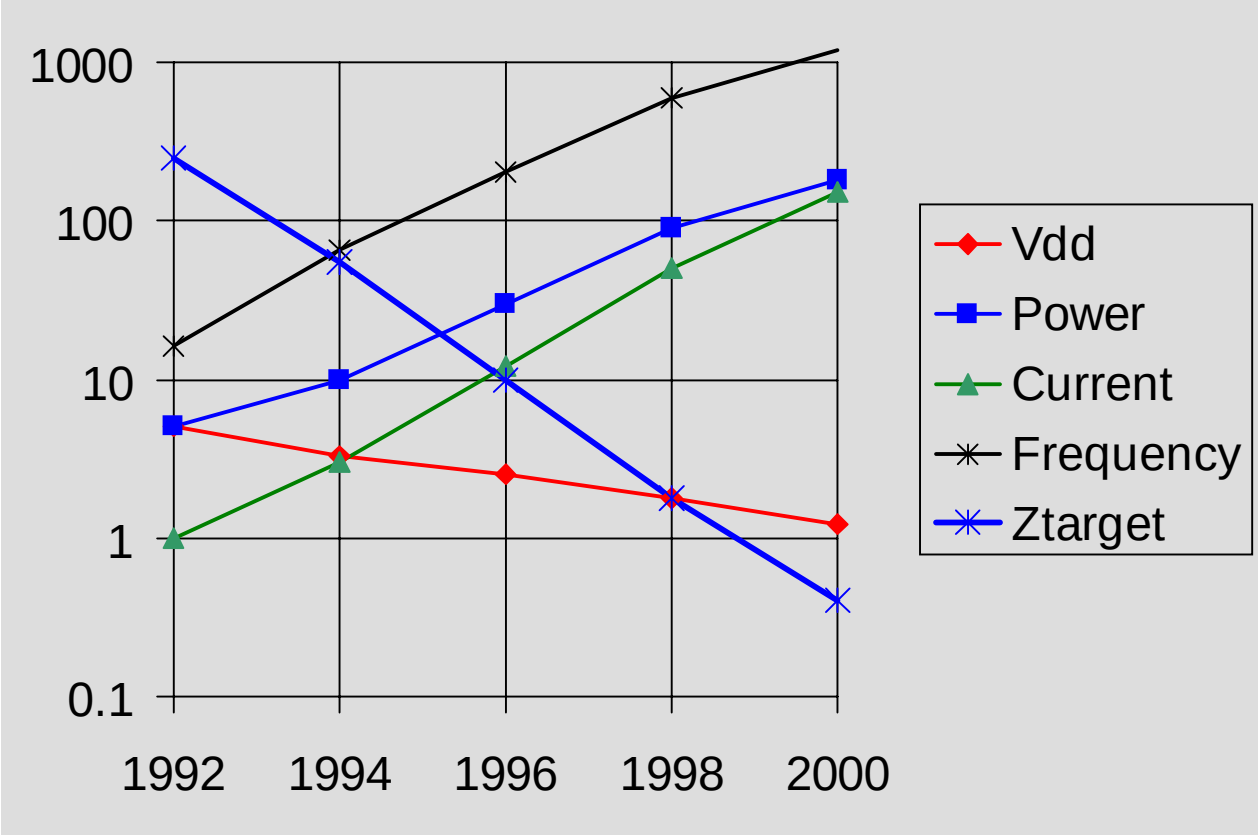
Power Distribution Requirements



Larry Smith, "Power Distribution for High Performance Systems," Conference Class 4, EPEP98, West Point, NY, October 26-28, 1998

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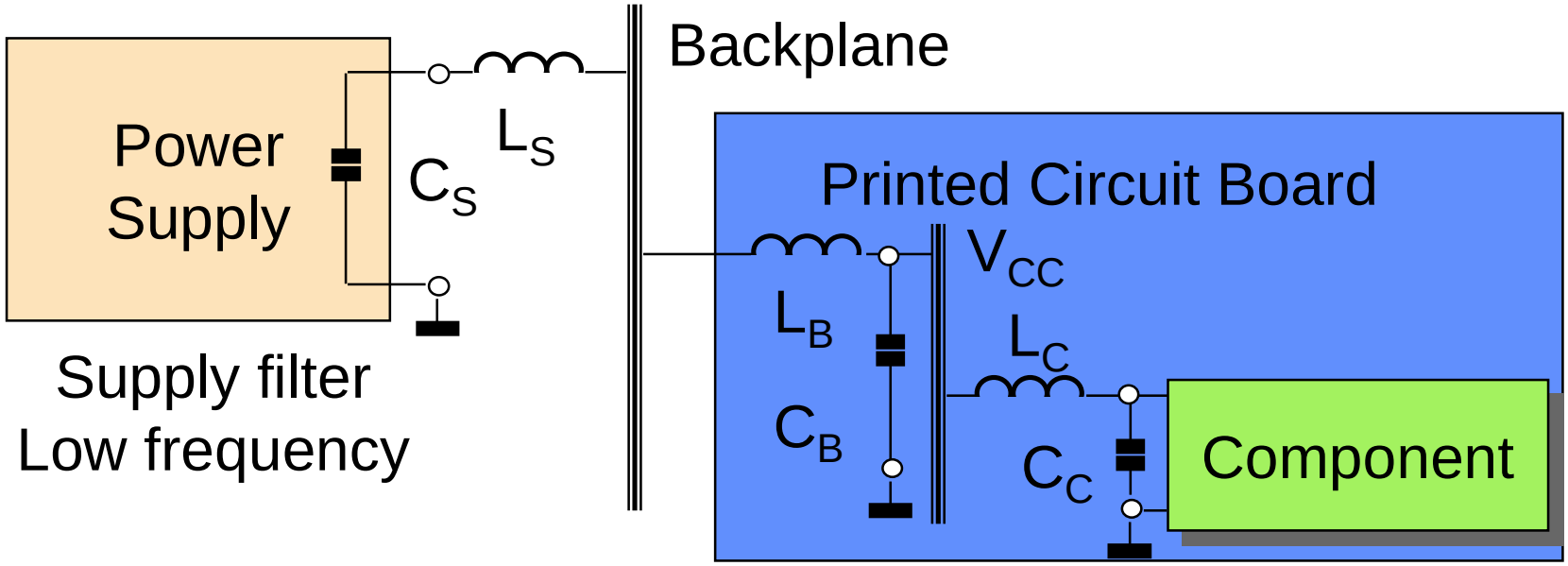
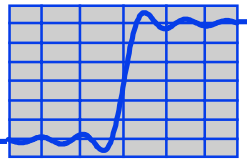
Power-Distribution Hierarchy





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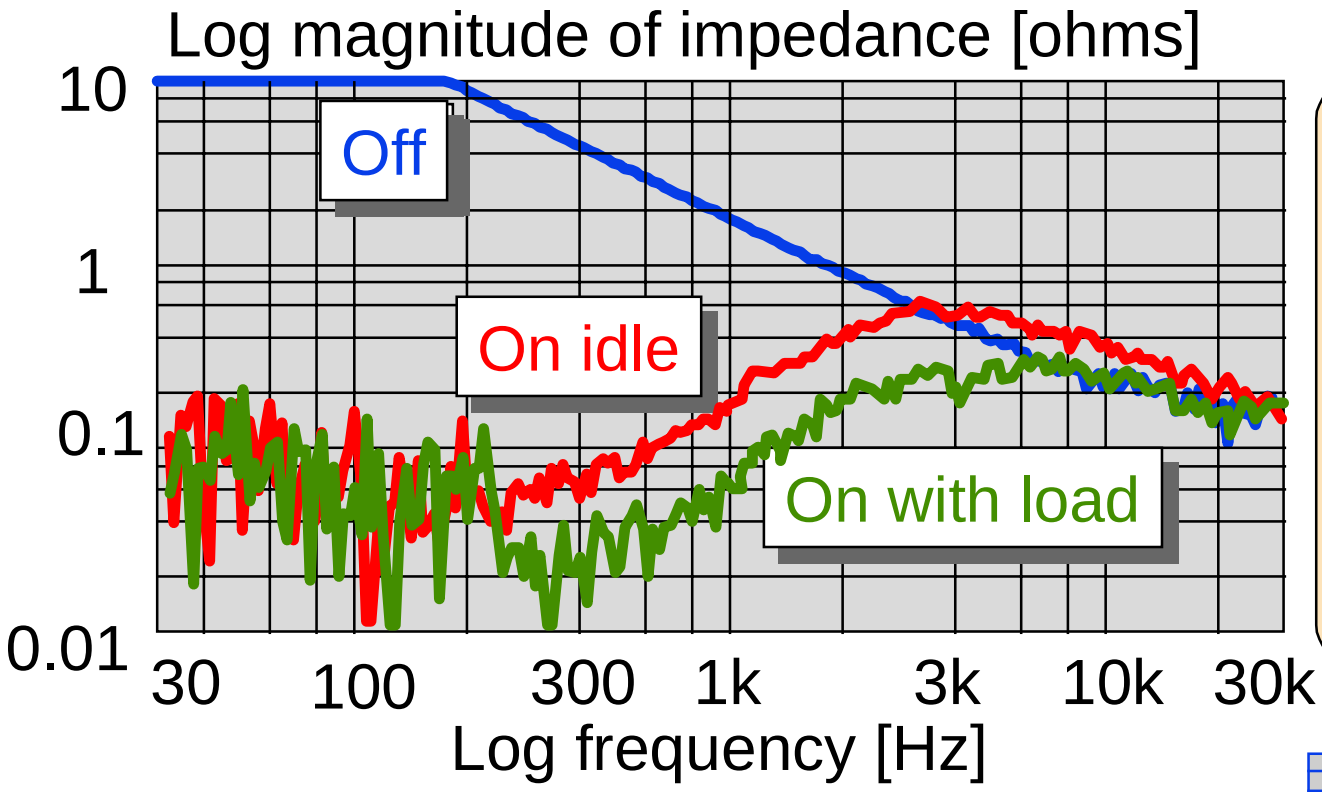
SMPS Output Impedance

Measured output impedance of a 50W SMPS



Output impedance varies with input and output conditions (V_{in}, I_{load})

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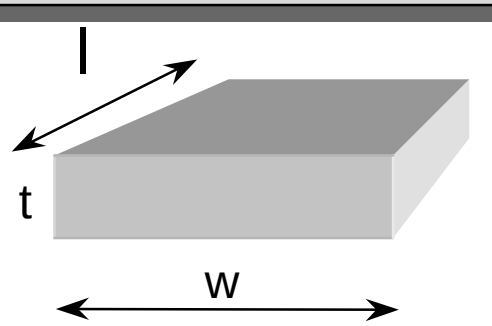
DC Resistance



Resistance of a homogeneous square conductor:

$R = \rho\, l / A\ [\Omega]$

ρ: resistivity of material [Ωm]

$R = R_{sheet}\, l/w\ [\Omega]$

R_{sheet} : sheet resistance (@ ρ, t)

l: length of conductor [unit]

w: width of conductor [unit]

t: thickness of conductor [unit]

Example:

2 ounce (2.76mil, 70μm) copper on 6" by 9" PCB:

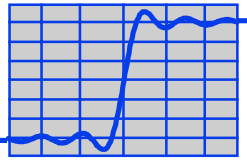
$\sigma = 5.85\ 10^7$ [S/m]

R_{DC} = 0.00037 ohms (along the 9" side)

Copper sheet resistance: $679/T_p$ [μΩ]

T_p : sheet thickness [mils]

R_{DC} = 370 microohms (along the 9" side)



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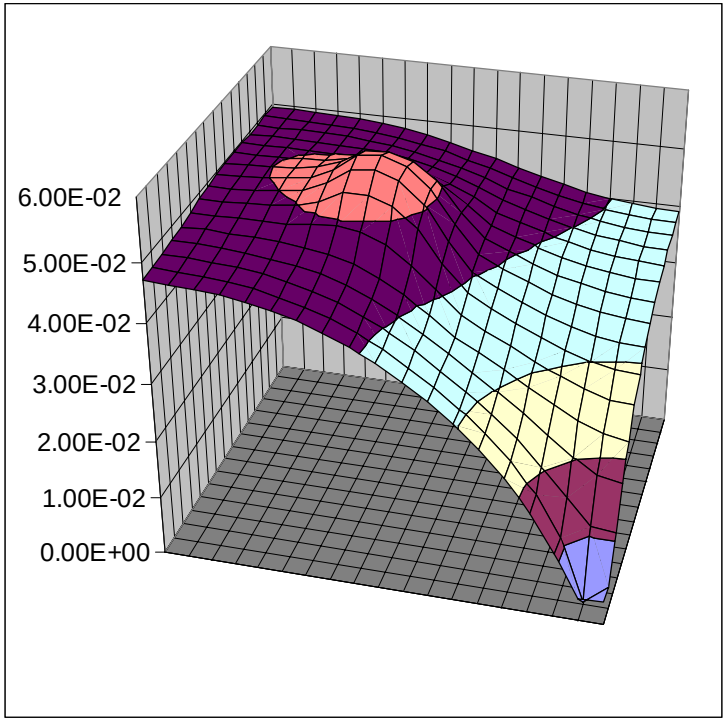
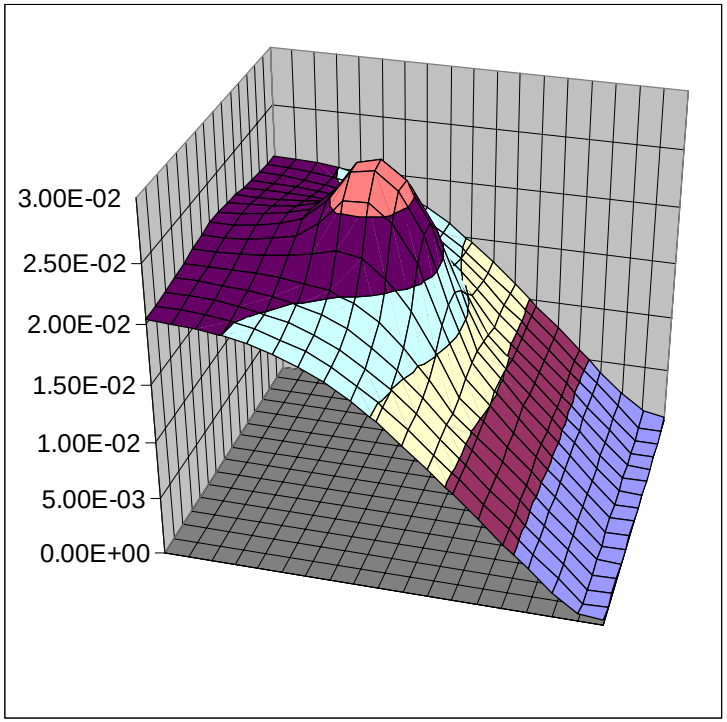
DC Drop on Planes, Connection





Simulated DC voltage drop on a pair of 3”x3.6” one ounce copper planes, with single-point feed at the front corner (left graph) and with line feed (right graph). Model: resistive grid with 0.2” grid size, 25A DC current sink at 1.5”x1.5” from upper left corner.

The floor grids of graphs represent the simulation grid.

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Inductors

Inductors in logic circuits are used for

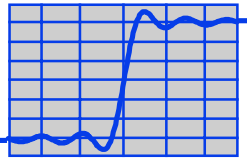
* decoupling
* EMI filtering

Inductance may appear as side effect:

* inductance of lead-frames
* inductance of connector pins
* inductance of ground returns
* inductance of component leads

There are different selection criteria for

* small-signal filtering
* high-current decoupling



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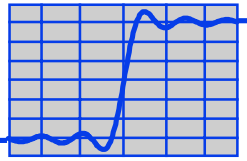
Inductor Parameters

* Nominal inductance
* Tolerance of inductance
* Rated AC and DC current
* Temperature dependence (TC)
* Loss factor
* Packaging, parasitics

Magnetic materials with high μ are nonlinear, unstable.

For decoupling and EMI filtering applications, lossy inductors are preferable.



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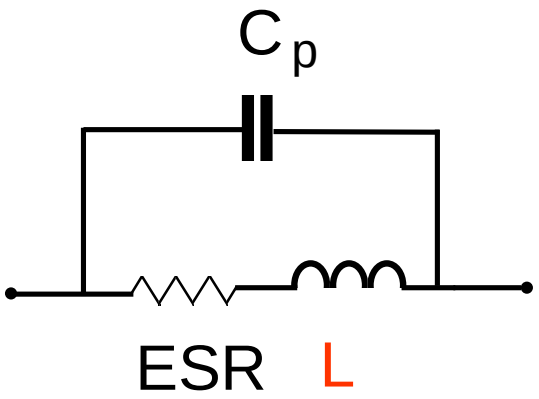
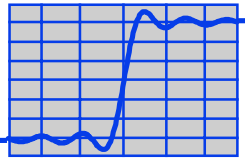
Inductor Equivalent Circuit

Linearized model:



* ESR: Effective series resistance
* L: Nominal inductance
* C_p: Equivalent parallel capacitance

Components in the equivalent circuit are nonlinear.



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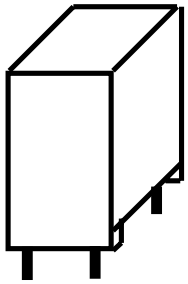
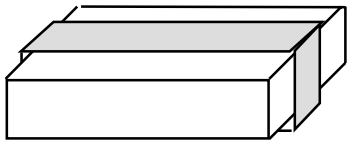
Inductor Parasitics, Decoupling

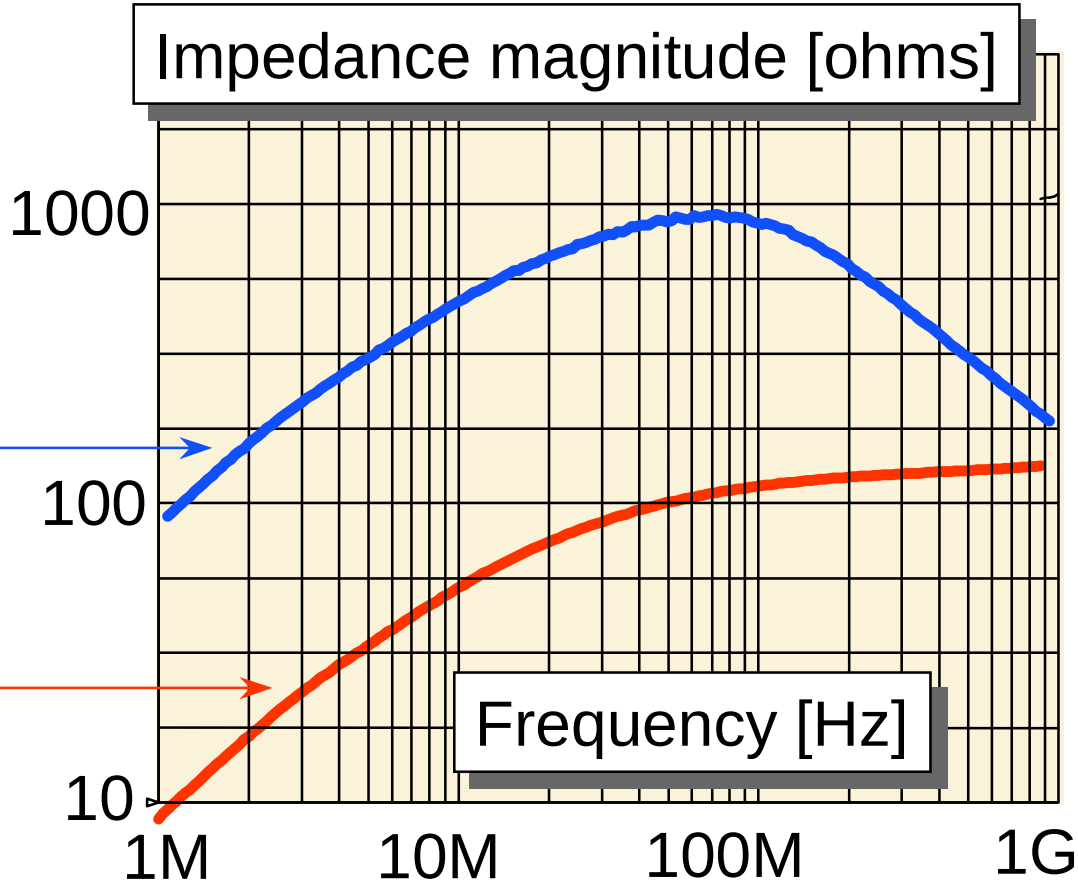
Fair-Rite lossy inductors:

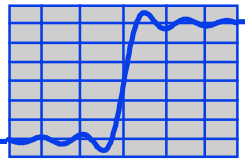
three half turns



single-turn SMD







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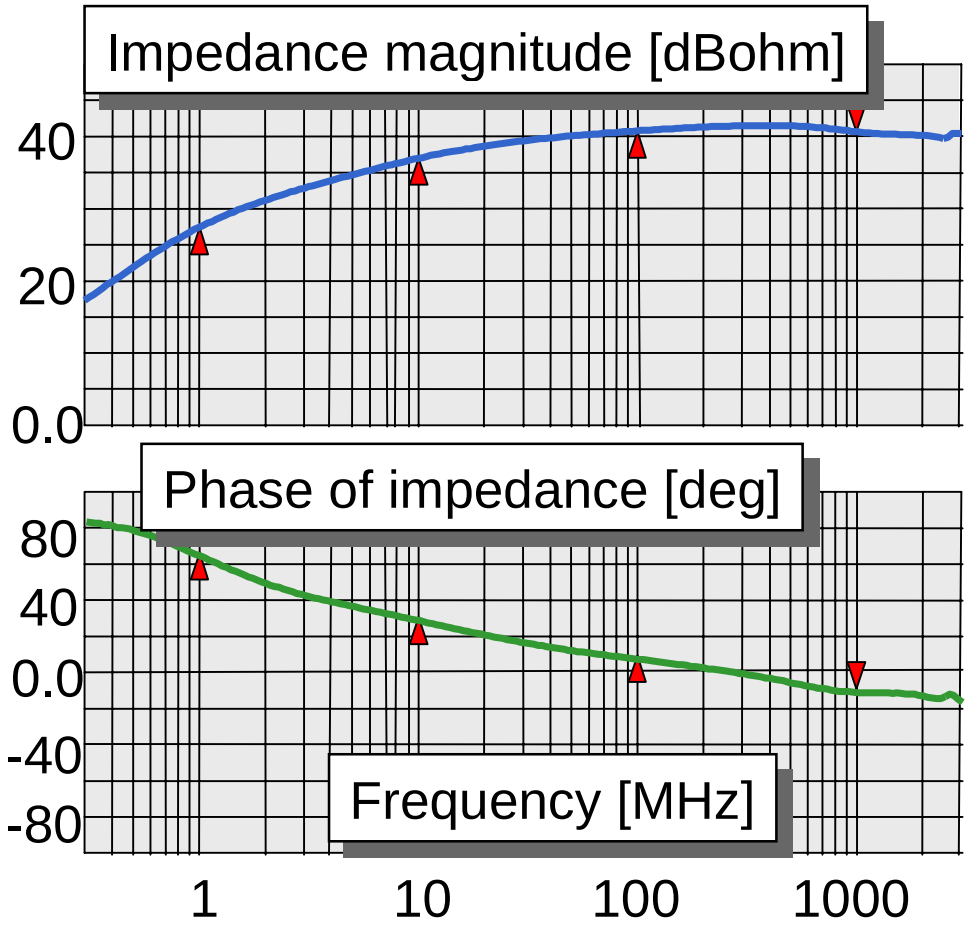
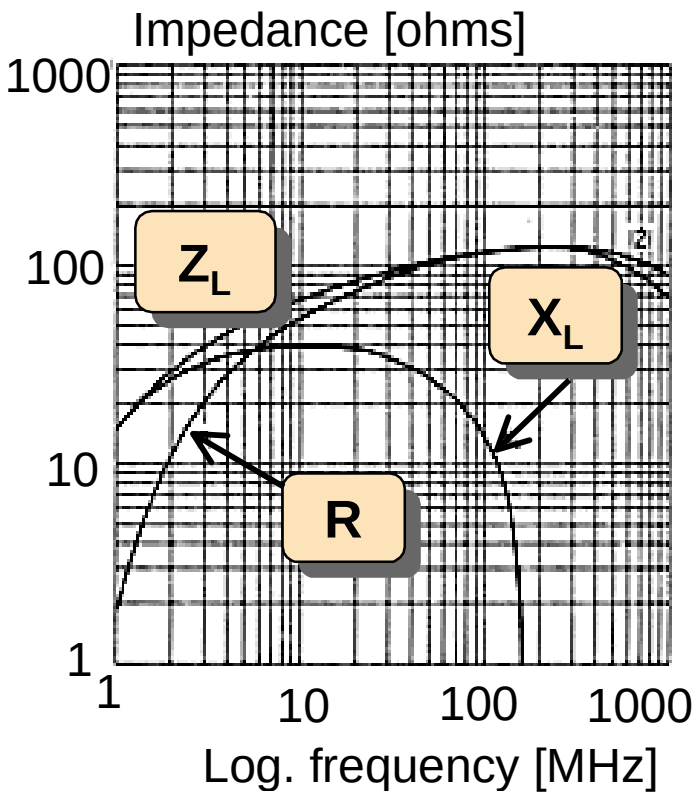
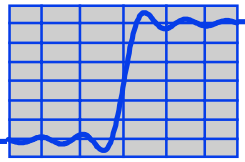
TDK 70ACC453215T SMD L

Measured:



Specification:





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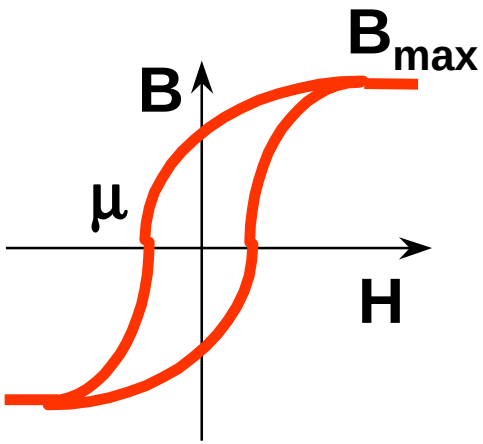
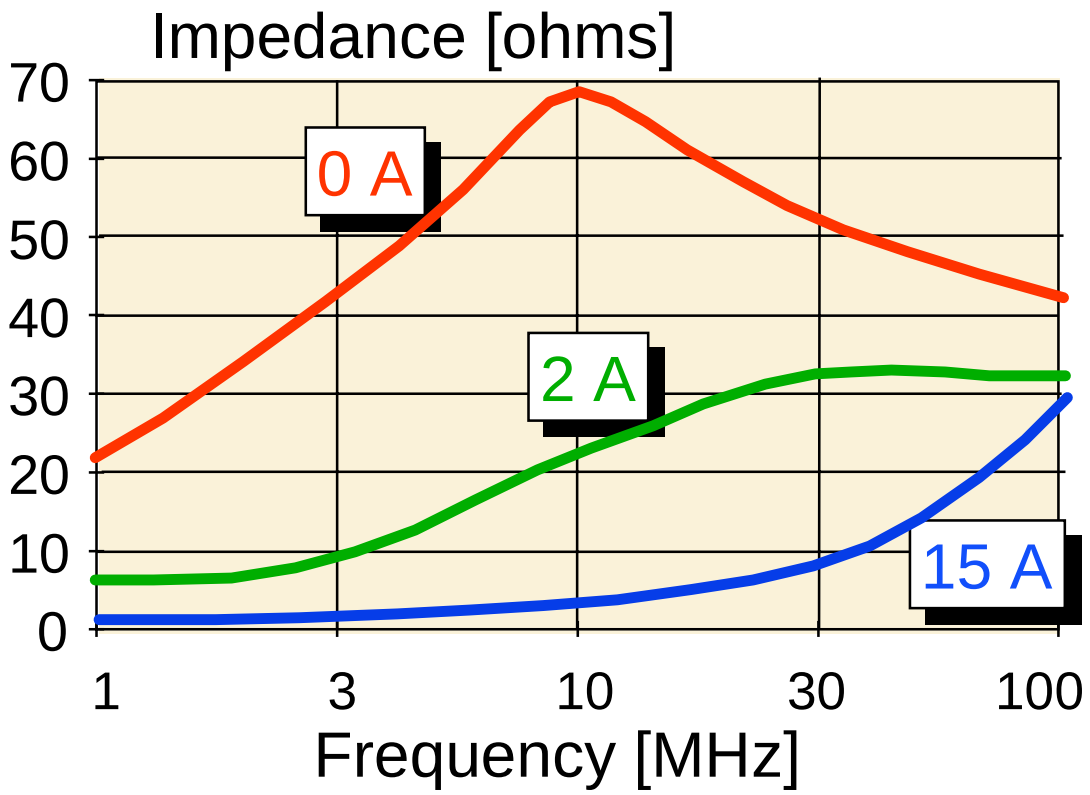
DC Bias, Saturation

Variation of total impedance with DC bias and frequency of a Fair-Rite bead.





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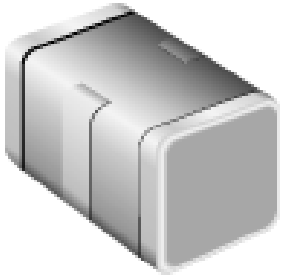
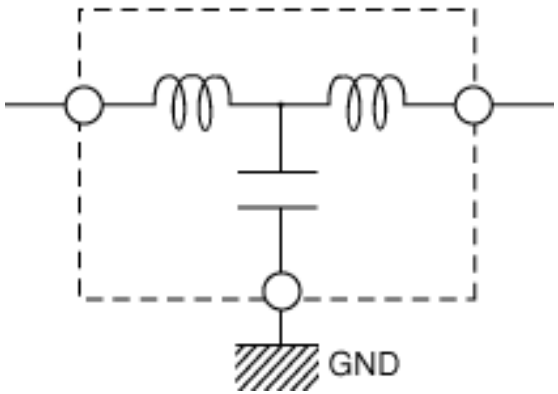
EMI T-Filters



Equivalent Circuit

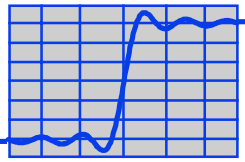


http://www.tdk.com

Three-node EMI T filters are optimized for 50-ohm operation.

Using EMI T filters in low-Z high-Z bypassing/decoupling may result in peaky response.

Use lossy ferrites instead.



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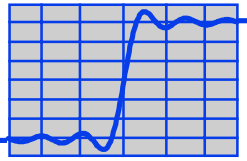
Capacitor Parameters

* Nominal capacitance
* Tolerance of capacitance
* Rated DC voltage (polarization)
* Quality factor, loss
* Packaging, parasitics

Dielectric materials with high ε_r have several drawbacks. The capacitance is a function of:

* frequency
* DC and AC voltage
* temperature (TC)
* time (long-term stability)



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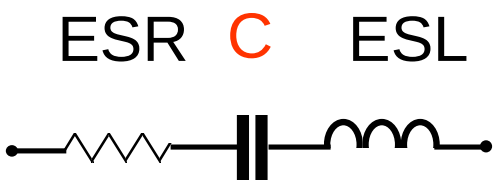
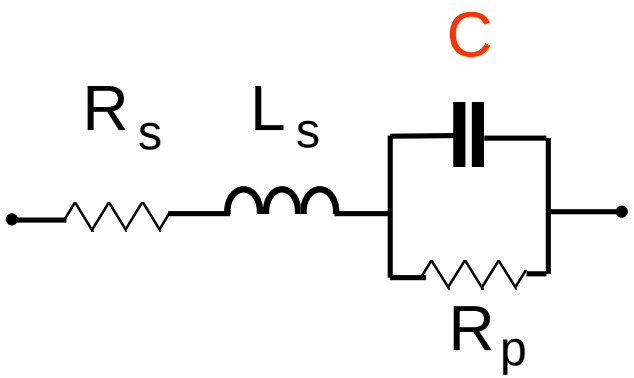
Capacitor Equivalent Circuit

Simple model:



Extended model:



C: Nominal capacitance

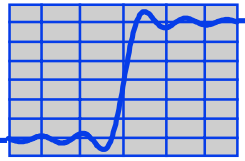
ESR: Effective series resistance

L_S : Effective series inductance (ESL)

R_S : Equivalent series resistance

R_P : Equivalent parallel resistance

Components in the equivalent circuit may be frequency dependent and/or nonlinear.



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Capacitor Parasitics

1: 1nF chip

ESR= 1Ω ESL= 1.6nH

2: 100nF chip

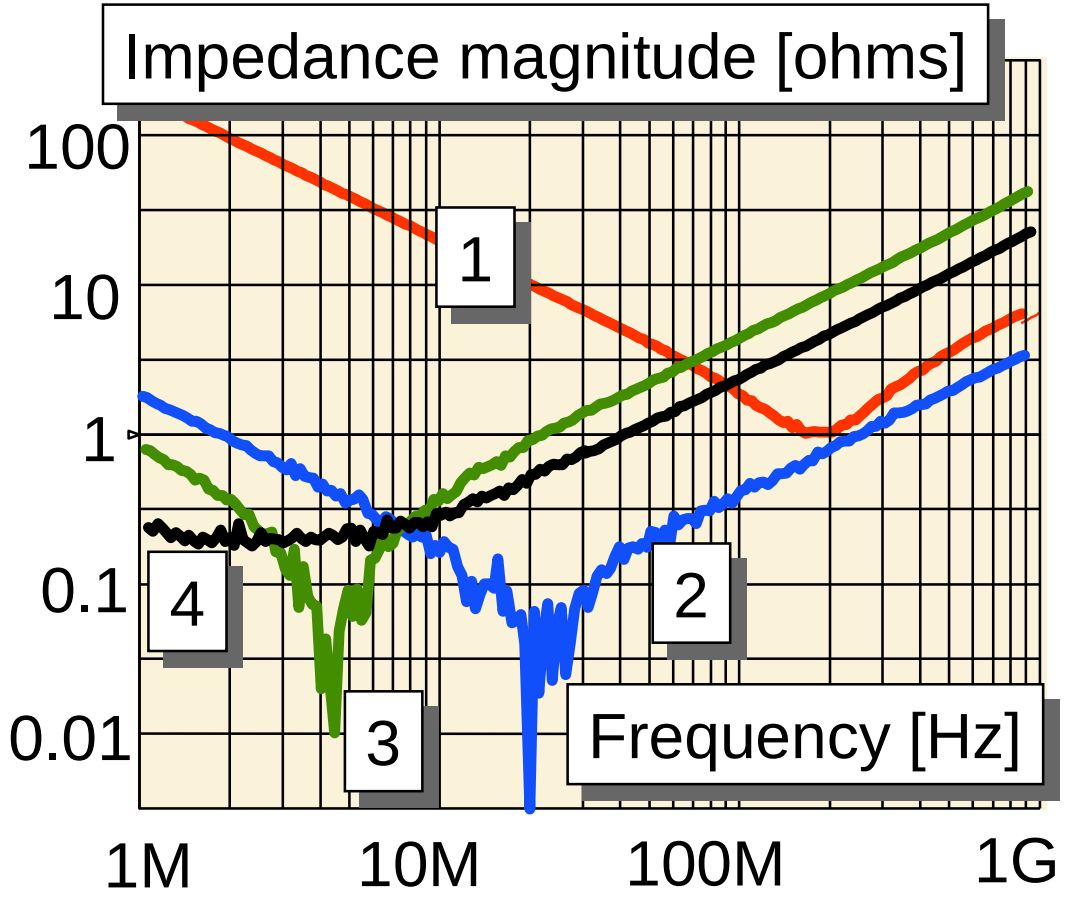
ESR= 10mΩ ESL=1nH

3: 220nF foil

ESR=10mΩ ESL=8nH

4: 10μF tantalum bead

ESR= 0.2Ω ESL=6nH



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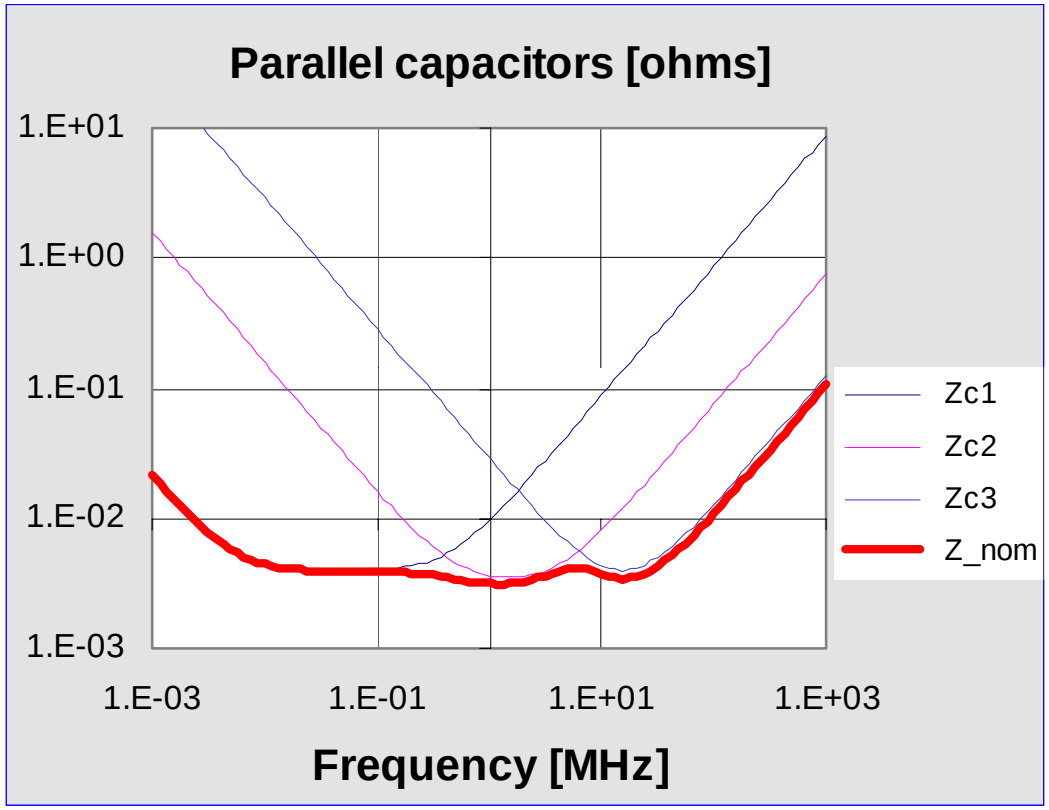
Capacitor Banks



5 x 1500uF 0.02 ohm 7nH

10 x 10uF 0.035 ohm 1.2nH

25 x 0.22uF 0.1 ohm 0.5nH

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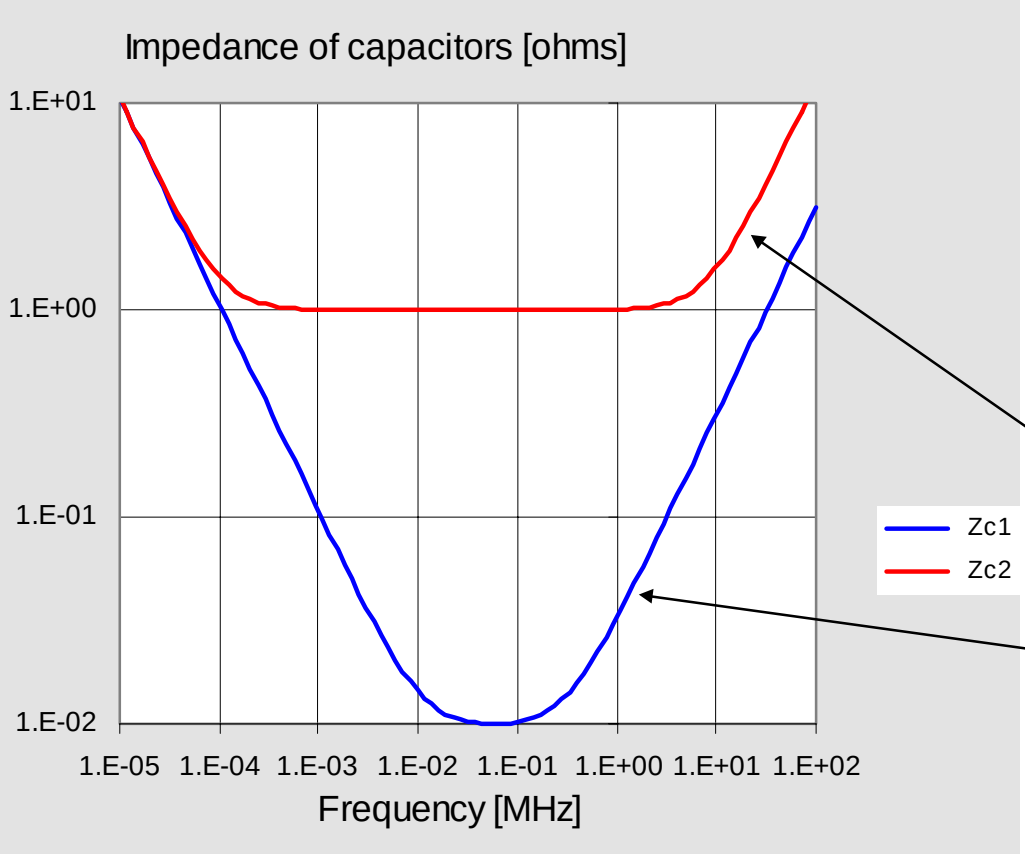
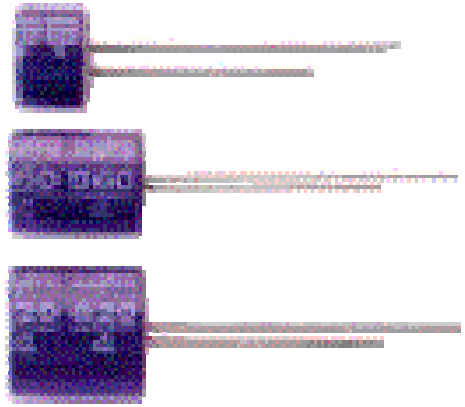
OSCON Bulk Capacitors





Standard aluminium:
1500uF 1ohm 20nH

OSCON SP Series:
1500uF 10mohm 5nH

http://134.180.49.67/compo/os-con/index_e.html

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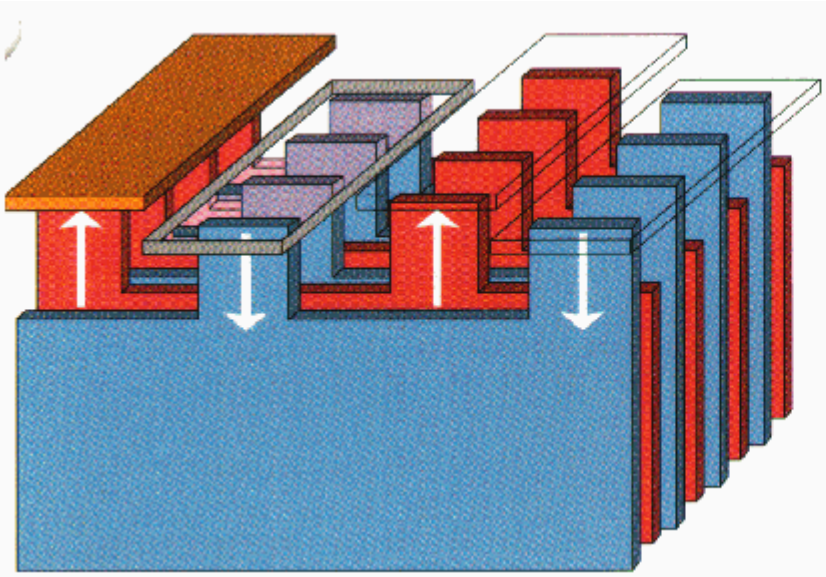
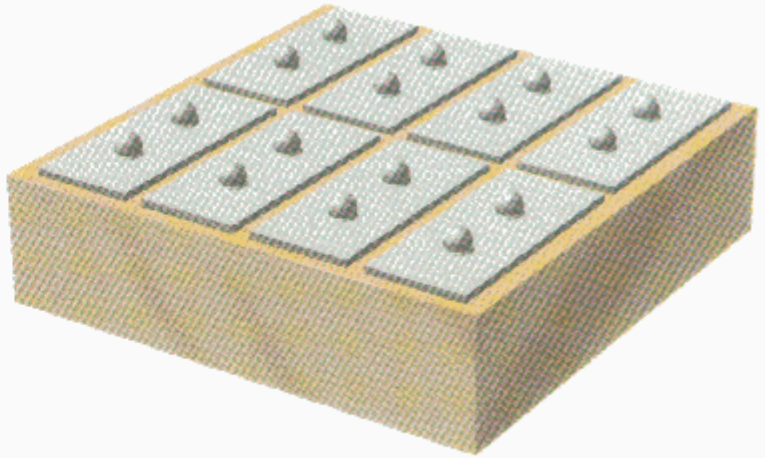
AVX Low Inductance Capacitance LICA

Internal construction:



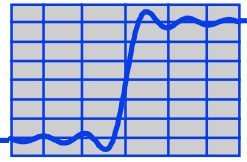
View of BGA connections:



Interleaved matrix connections

ESL = 100 pH

AVX Corporation: Low Inductance Capacitors, S-LICC5M396-C brochure, 1996.



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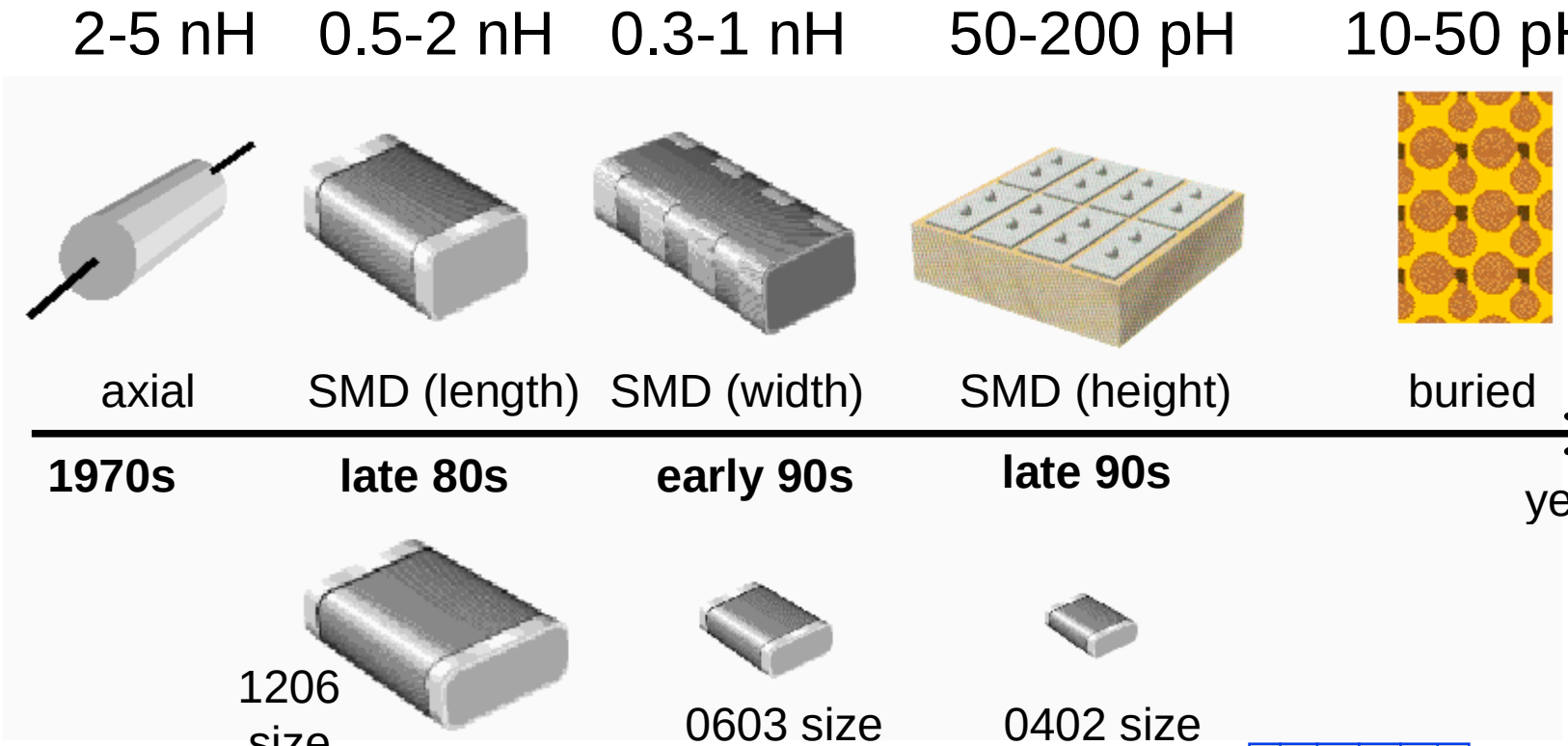
Technology Trend in Packaging of RLC Components (ESL)



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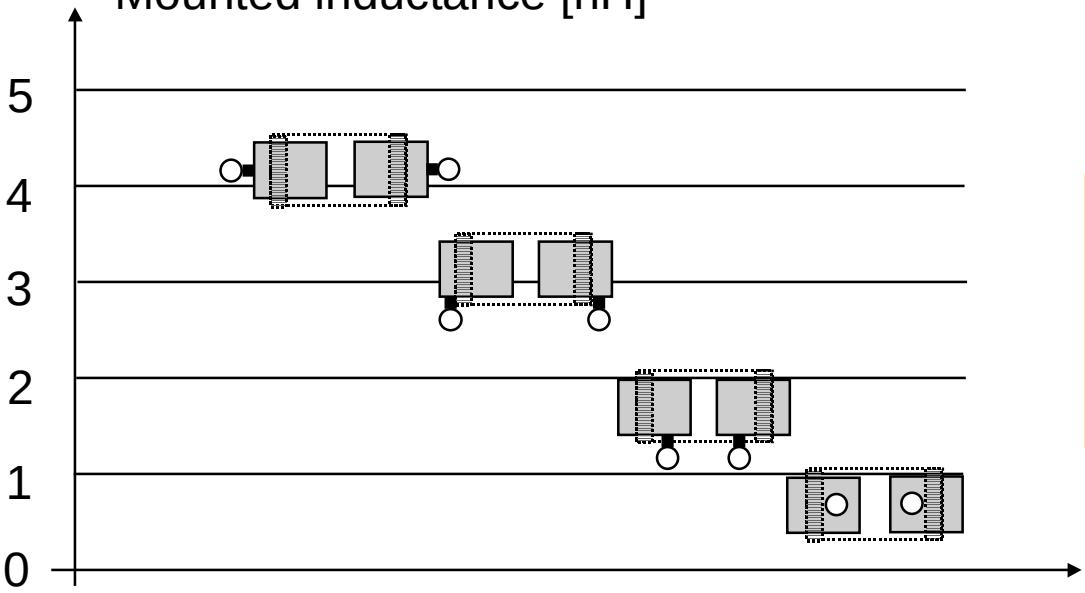
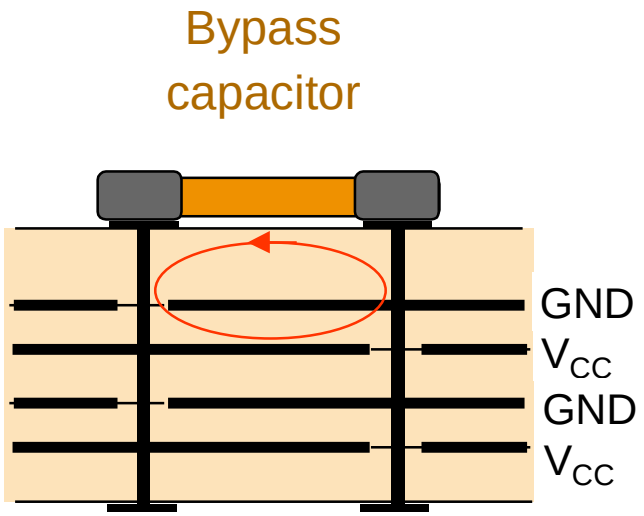
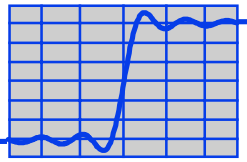
Mounted Inductance





Tanmoy Roy, Larry Smith, “ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications,” Proceedings of 1998 EPEP, West Point, New York, October 26-28, 1998, pp. 213-216.



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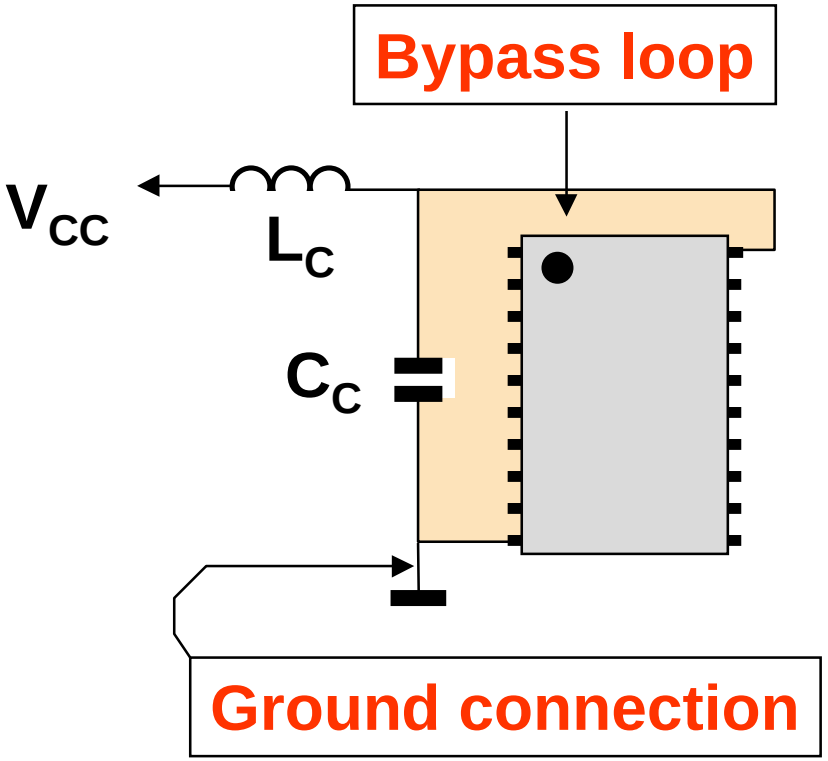
Location of Device Filter

* Bypass loop must be small
* Ground connection must be short
* VCC connection should be inductive and/or lossy (thin trace, ferrite bead)



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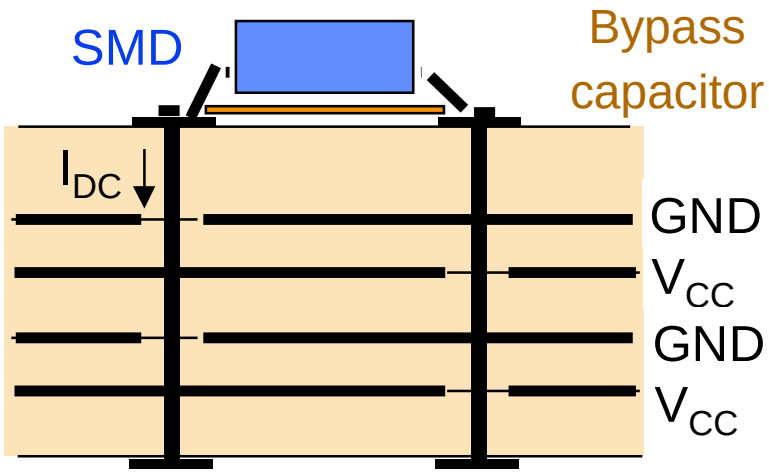
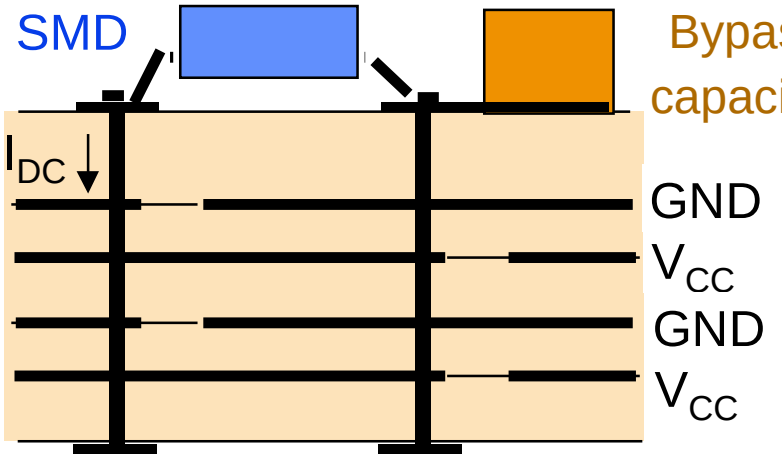
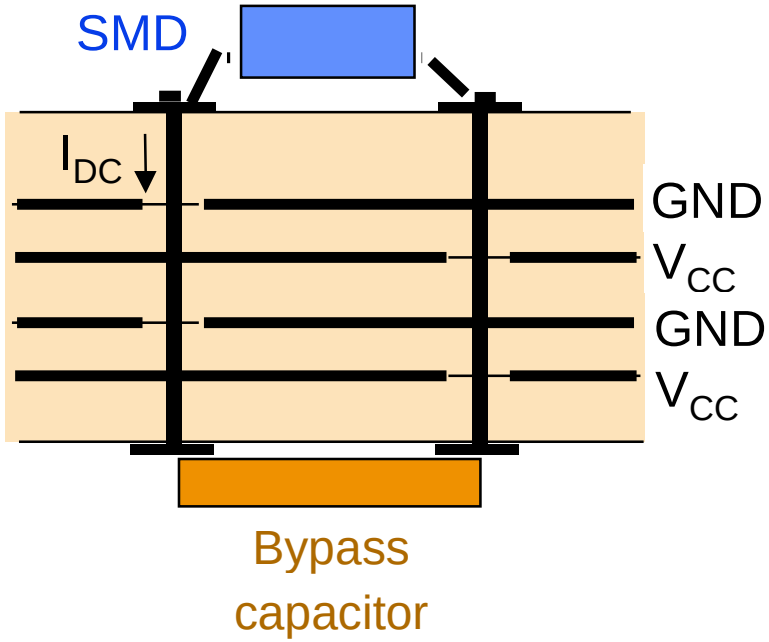
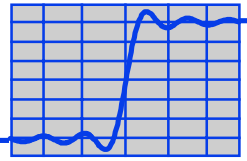
Location of Bypass Capacitor









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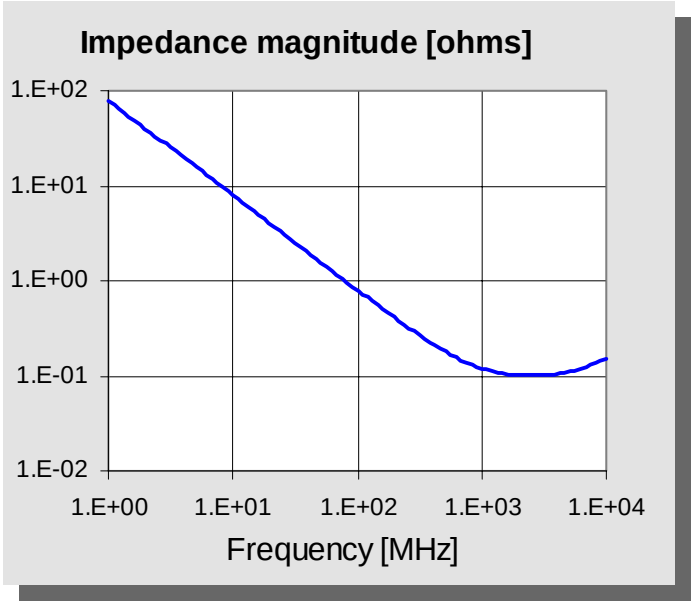
Integrated Capacitors

Available technologies:

- thin FR4-like cores
- ceramic-filled cores
- TaO thin-film structures



HADCO:

EmCap™

Dk: 20-50
thickness: >=4mil
capacitance: 2.5nF/inch^2

http:\\www.hadco.com

Dk: 25
thickness: 0.02mil
capacitance: 2.5nF

K.Y. Chen, W.D. Brown, L. Schaper, "Modeling and Simulation of Thin Film Decoupling Capacitors," Proceedings of the EPEP Conference, October 26-28, 1998, West Point, NY, pp/ 205-208.

http:\\www.hidec.engr.uark.edu

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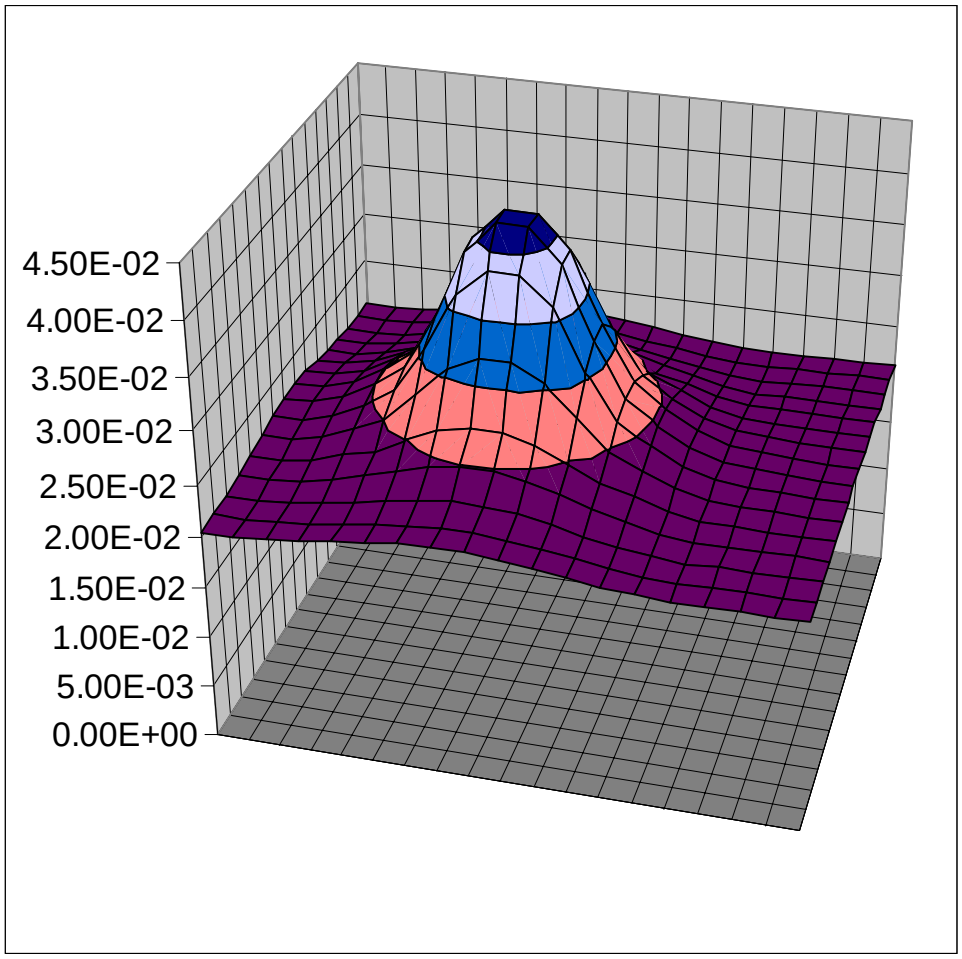
Inductance of Planes



Simulated inductive voltage drop (mV) on a pair of 3”x3.6” copper planes with 1mil separation. Model: Tline grid with 0.2” grid size, 2A/nsec PWL current sink at 1.5”x1.5” from upper left corner.
The floor grids of graphs represent the simulation grid.

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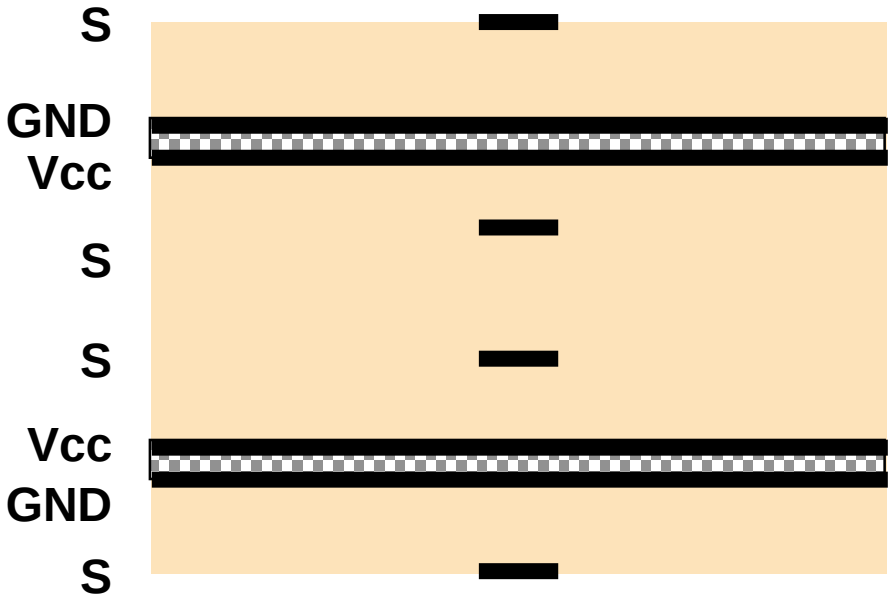
Buried Capacitance ™

Developed and licenced by Unysis, Zycon.

Multilayer board

* h = 2 mils = 51 microns
* ε_r = 4.5 (FR4)
* Low inductance ~ pH
* No signal trace between
* Layer count increases by two

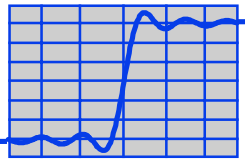


$C_i = \varepsilon_o \varepsilon_r A/d =$

$= 78.4\ pF/cm^2$

URL=http://www.automata.com/news/papers/zycon/toc.htm

R. Evans, M. Tsuk, "Modeling and Measurement of a High-Performance Computer Power Distribution System," IEEE Trans. on Components, Packaging, and Manufacturing Technology - Part B, Vol. 17, No. 4, Nov. 1994, pp. 467-471.



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Innerlayer Capacitance of Large PCB

Multilayer backplane

h = 0.95 mm

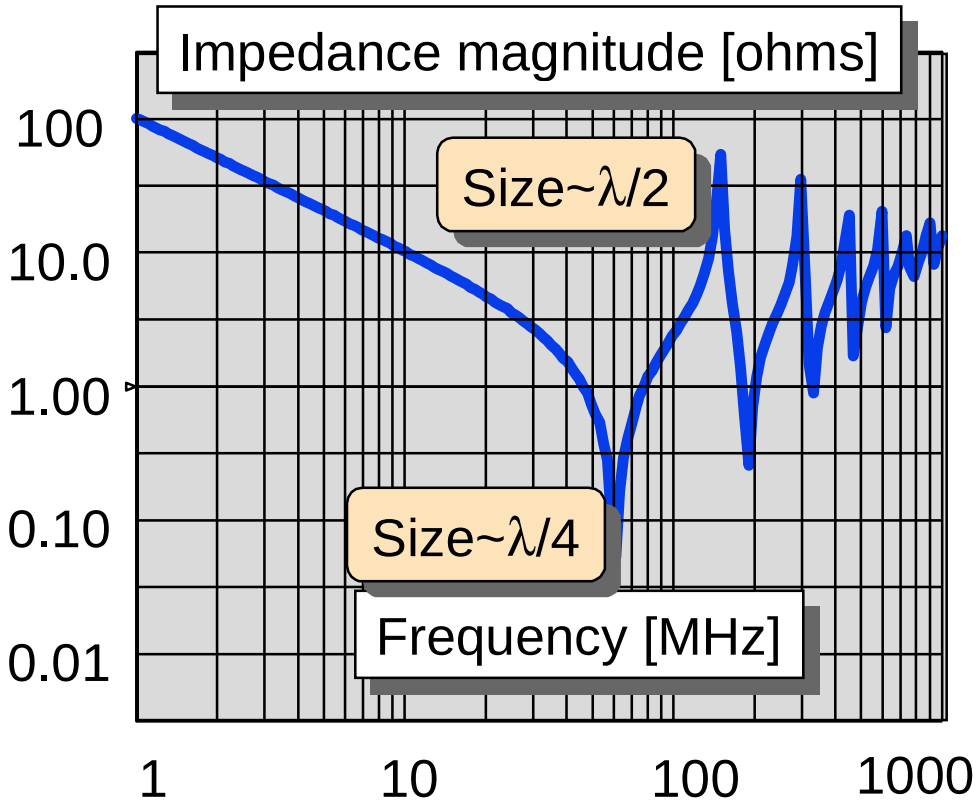
ε_r = 4.7 (FR4)

$C_i = \varepsilon_o \varepsilon_r A/d =$

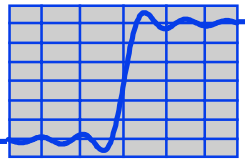
$= 4.3\ pF/cm^2$

Correction with pad clearances is needed

480 x 110 x 1.5 mm FR4 PCB



M. P. Goetz, "Time and Frequency Domain Analysis of Integral Decoupling Capacitors," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B: Advanced Packaging, Vol. 19, August 1996, No.3, pp. 518-522.



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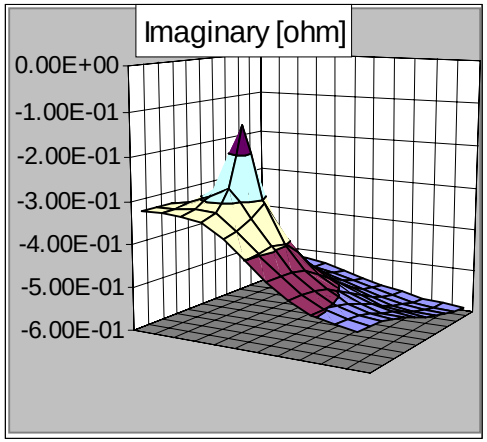
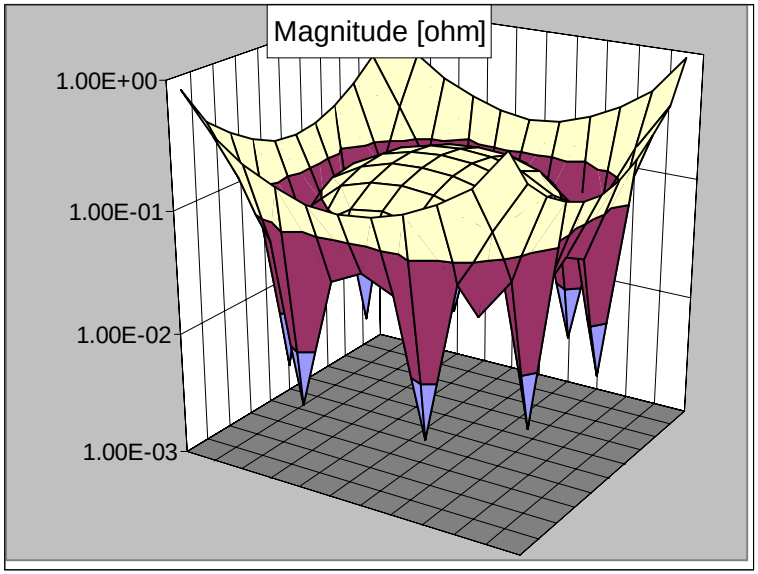
Plane Resonances

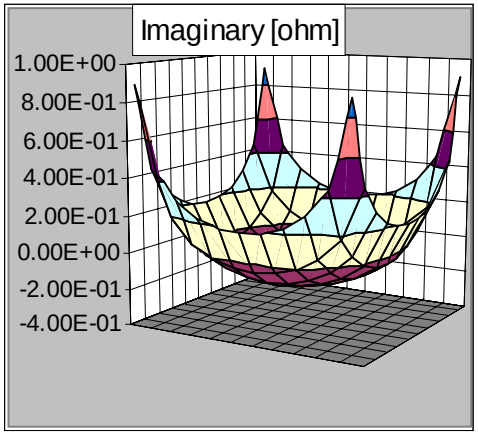
10”x10”x31mil FR4 planes at 100MHz

Transfer impedance from Node 4,4



Magnitude and imaginary self impedances





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Feb. 1999
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Reducing Plane Resonances

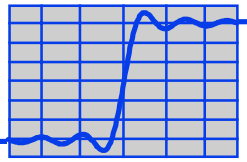
Resonances can be suppressed by

* series DC loss (no good)
* series AC loss
* parallel AC loss [1]
* capacitive damping at selected locations [2]
* dissipative edge termination [3]

[1] J. Bandyopadhyay, P. Chahal, M. Swaminathan, "Importance of damping and resonance in thin-film integrated decoupling capacitance design," Proceedings of the 6th Topical Meeting on the Electrical Performance of Electrical Packaging, October 27-29, 1997, pp. 31-34.

[2] C. B. O'Sullivan, L. D. Smith, D. W. Forehand, "Developing a Decoupling Methodology with SPICE for Multilayer Printed Circuit Boards," proceedings of the 1998 International Symposium on Electromagnetic Compatibility, Aug 1998, Denver, CO.

[3] I. Novak, "Reducing Simultaneous Switching Noise on Power Planes by Dissipative Edge Termination," EPEP'98, October 25-27, 1998, West Point, NY.



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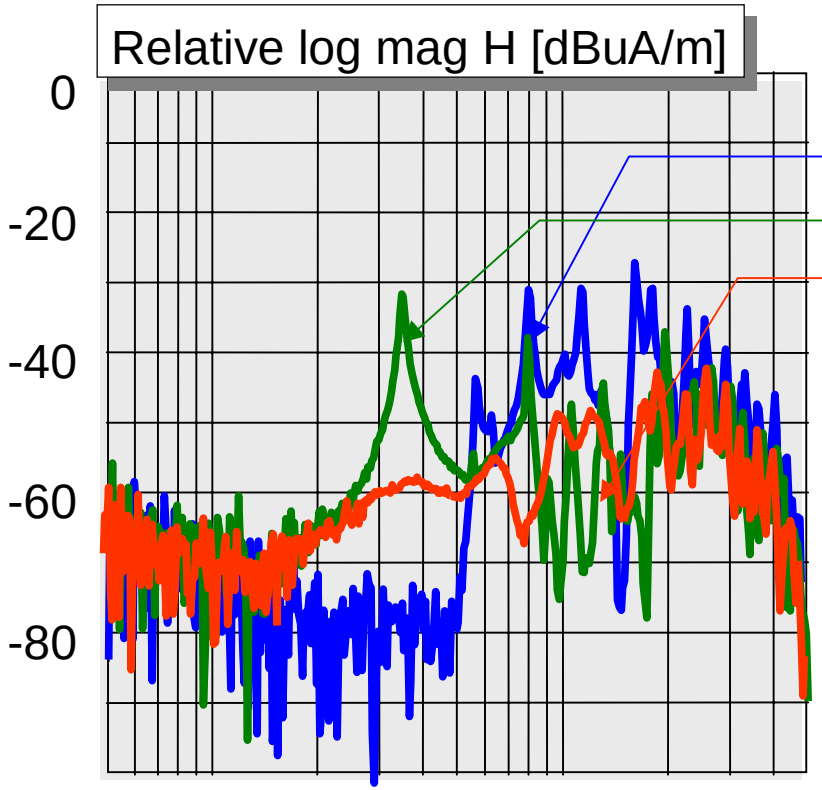
Reducing EMI by DET

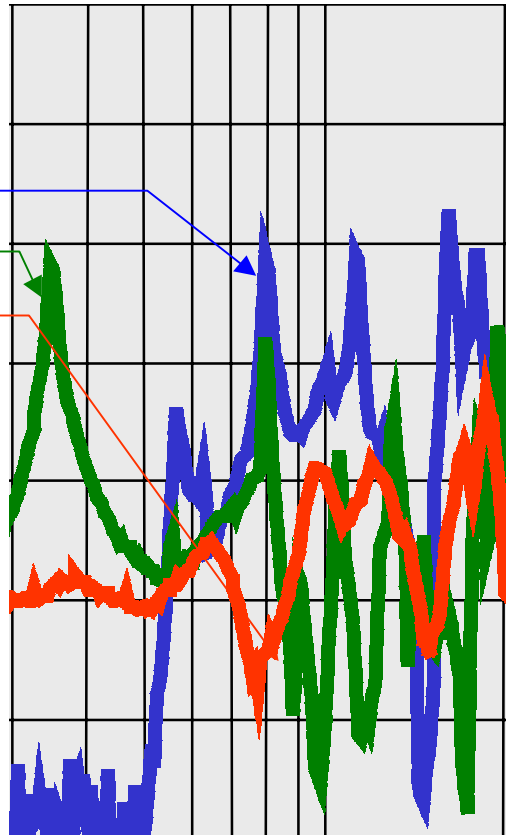


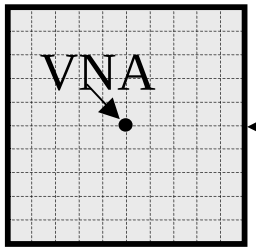
Open

Short

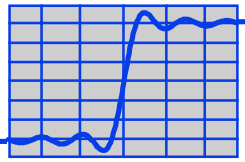
Terminated

Zoomed:





Probe



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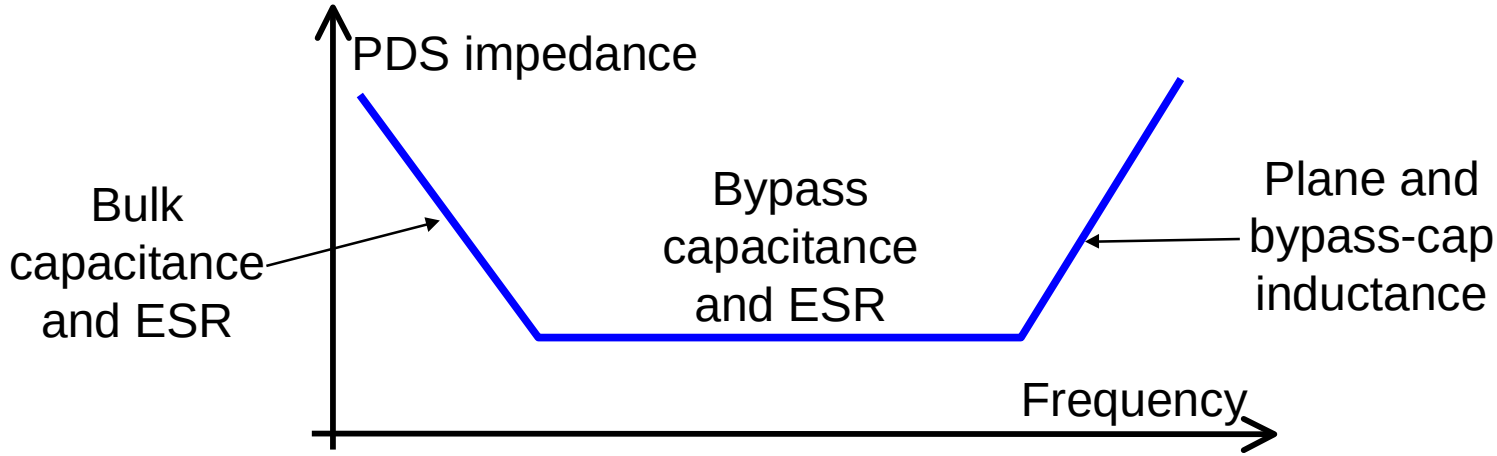
First-cut Lumped Bypass Methodology

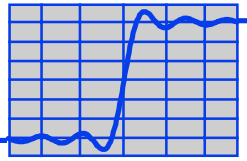
Identify target impedance/bandwidth >> bypass capacitance & ESR

Identify dI/dt load, V_{noise_max} >> plane and bypass-cap inductance

Identify power-supply response >> bulk capacitance & ESR



For detailed analysis, use SPICE with plane, package, and silicon models.



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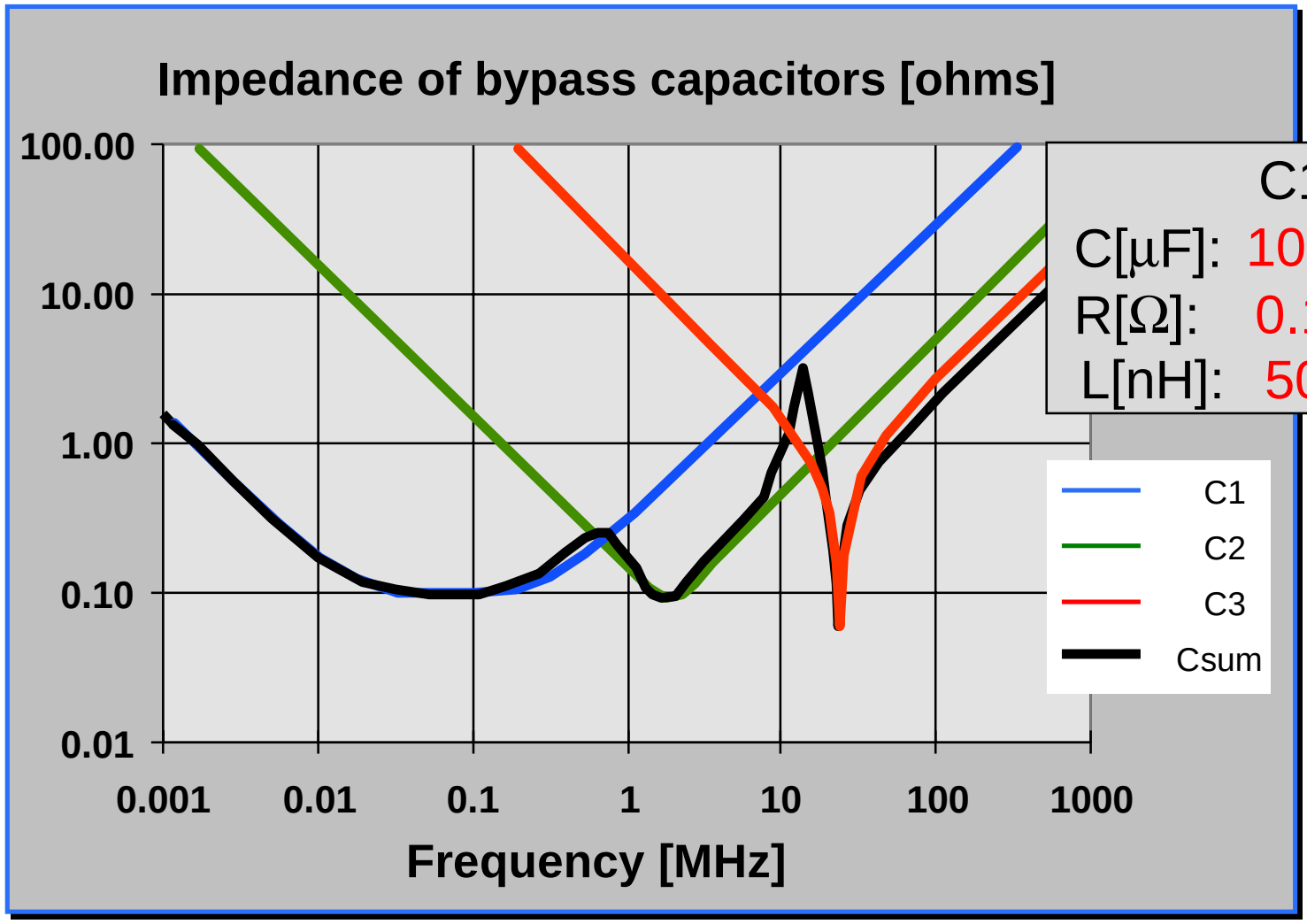
Parallel-C: Resonance



	C1	C2	C3
C[µF]:	100	1	0.01
R[Ω]:	0.1	0.1	0.05
L[nH]:	50	10	5

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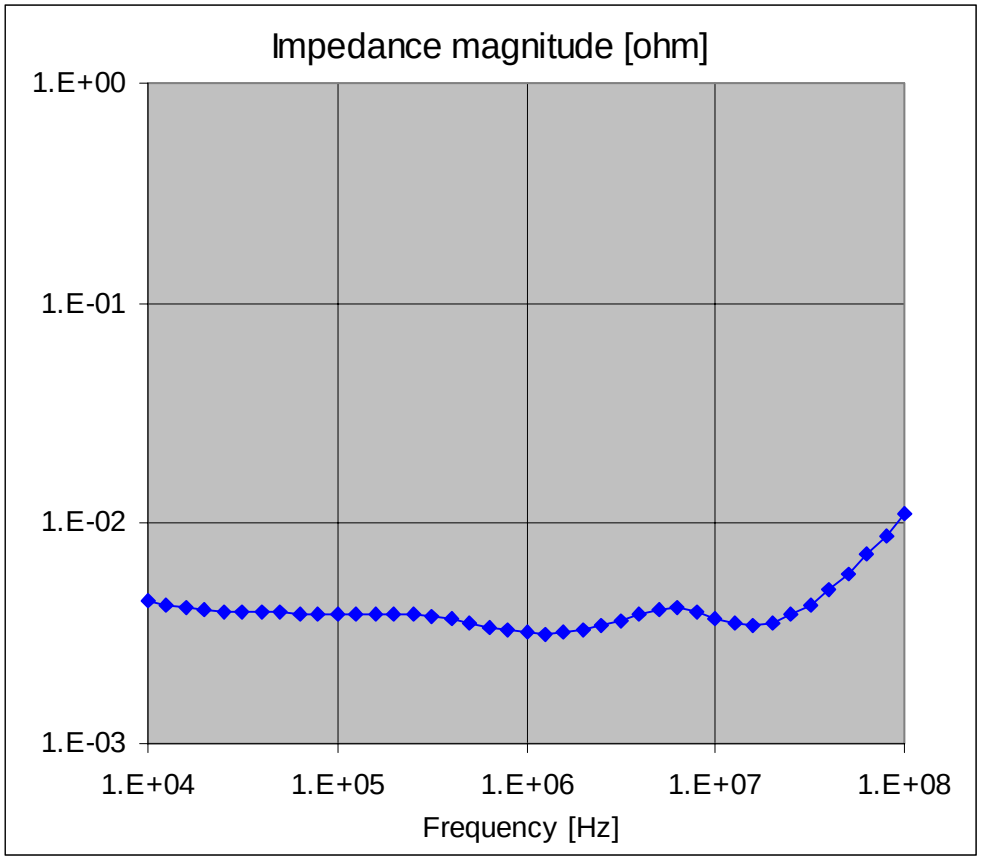
Correct Frequency Response



Target: 5mohm 10kHz-30MHz

5 x 1500uF 0.02 ohm 7nH

10 x 10uF 0.035 ohm 1.2nH

25 x 0.22uF 0.1 ohm 0.5nH

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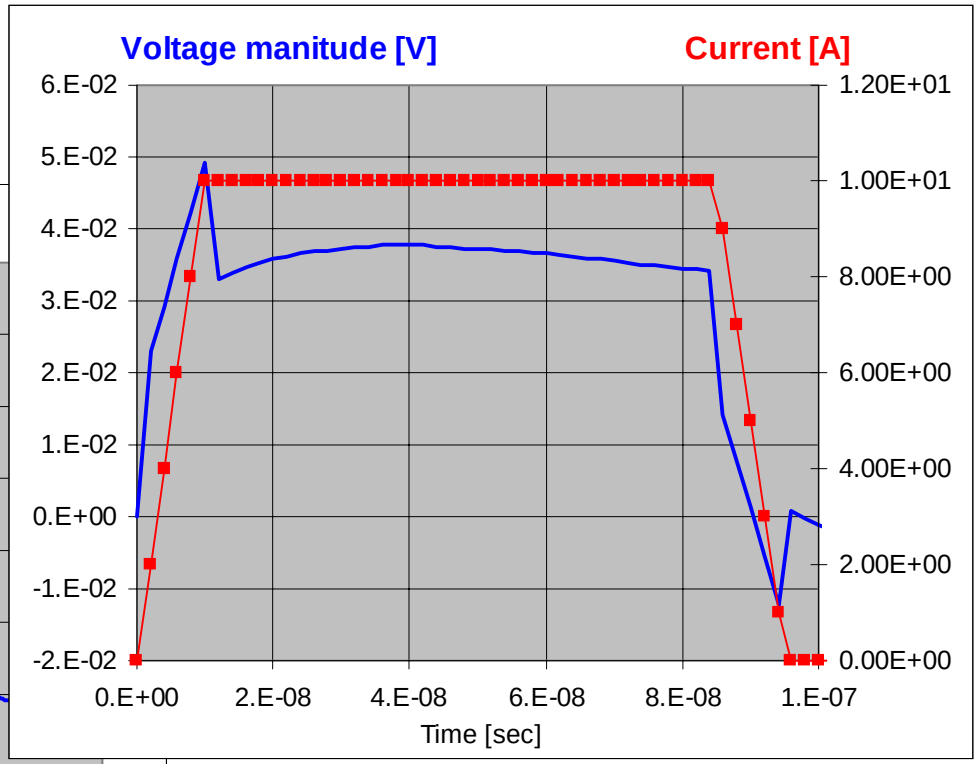
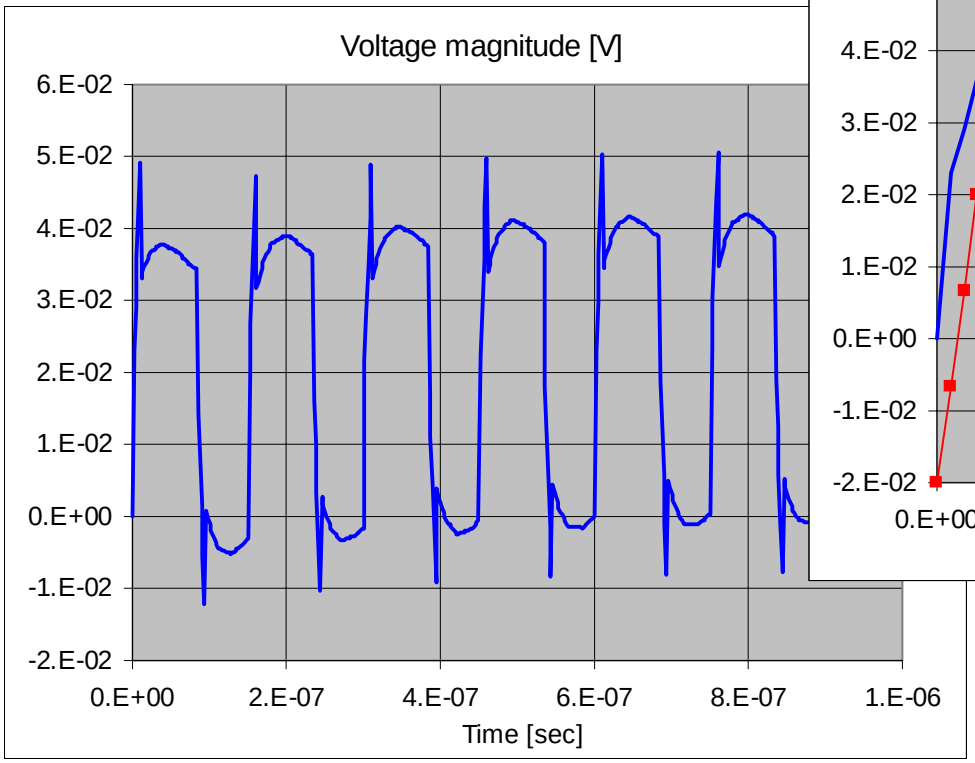
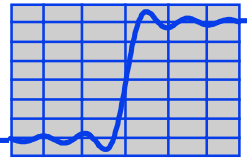
Correct Time Response

10A 10nsec PWL square current source
Lumped capacitors with ESR & ESL







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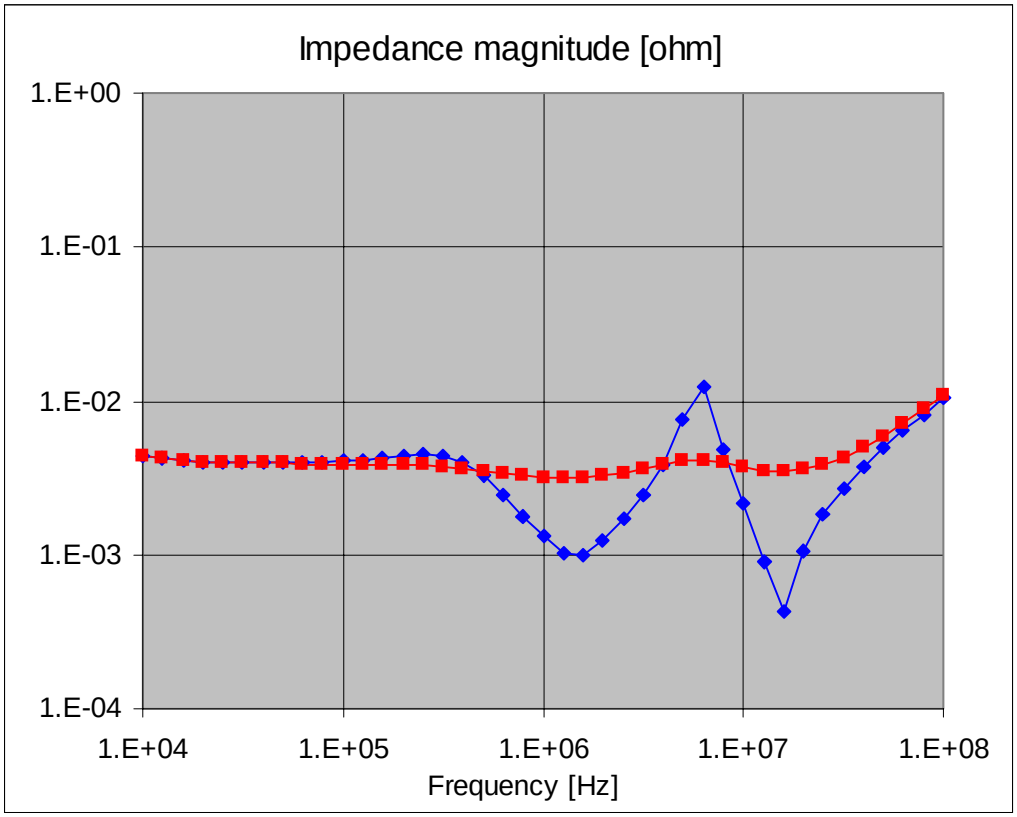
Low-ESR, Frequency Response



Target: 5mohm 10kHz-30MHz

5 x 1500uF 0.02 ohm 7nH

10 x 10uF **0.01** ohm 1.2nH

25 x 0.22uF **0.01** ohm 0.5nH

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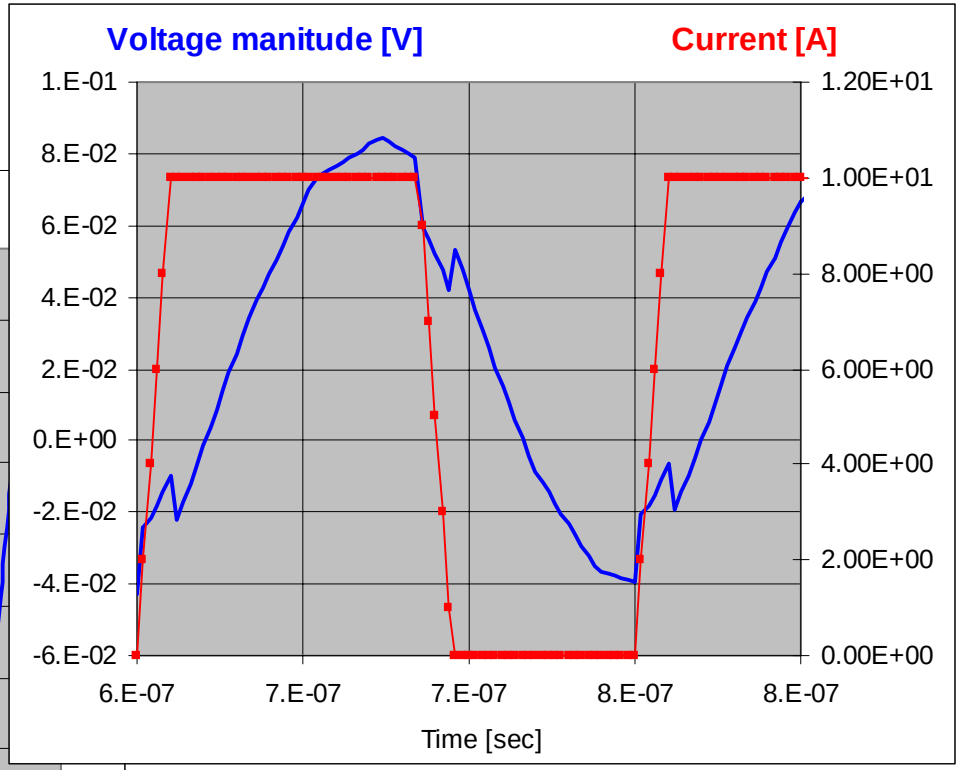
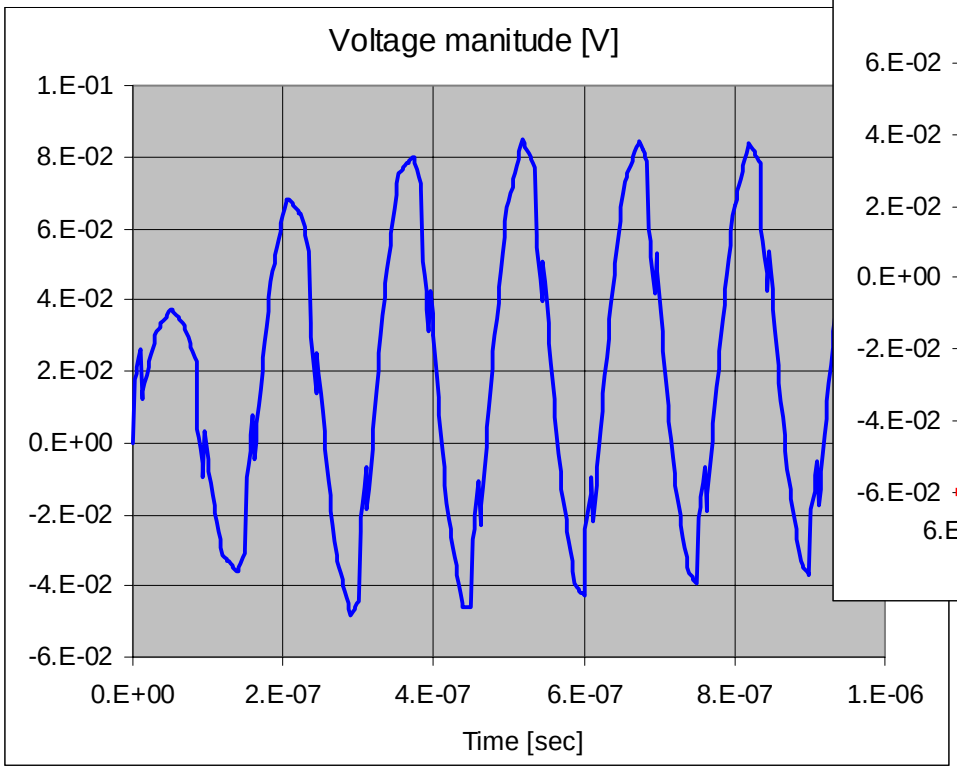
Low-ESR, Time Response

10A 10nsec PWL square current source
Lumped capacitors with ESR & ESL





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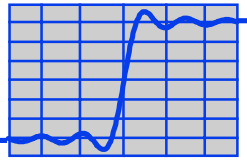
Summary

* Target impedance is in the mohm range
* Plane DC resistance analysis should be multi point
* Bypass capacitor ESL must be low
* Low-ESR capacitors may resonate
* Power planes have specific resonant frequencies
* Lumped models may be suitable for first-cut PDS design
* Detailed PDS design must include
  - component parasitics (ESL, ESR)
  - detailed plane model
  - power supply and package/silicon models are optional



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