Modeling of Plane Discontinuities for Power Distributions Networks

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Outline

- Introduction
- Modeling Vias
- Loop Inductance
- Partial Inductance Formulas
- Case Studies
- Via Measurements
- Summary

Introduction

- Accurate modeling of PCBs require models for:
  - Planes including cutouts
  - Discontinuties (vias and antipads)
- Proper modeling of discontinuities is important for several reasons:
  - Vertical inductance can exceed the plane contribution
  - Accurate impedance and resonance profiles
  - Realistic current return paths

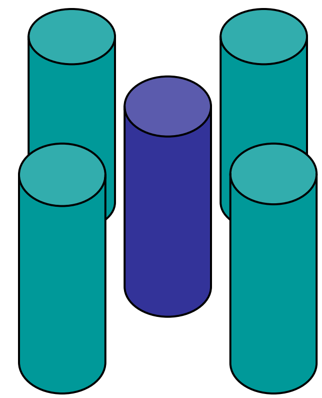
Modeling Vias

- Closed loop PCB current paths are hard to define.
- **Approach 1:** Capture all partial and mutual terms from L matrix. Huge computational penalty (e.g. 10 vias requires 55 unique elements), but accurate.
- **Approach 2:** Capture all partial self L and assess the inaccuracy introduced by ignoring the partial mutual L terms.
- Error in loop L from ignoring M for just two vias:

$$\mathbf{L_{loop} = L11 + L22 - M12 - M21}$$
$$\mathbf{L22 = L11,\ M21 = M12}$$
$$\mathbf{L_{loop} = 2{*}L11{*}(1 - M12/L11)}$$

Loop Inductance

- **Example:** Loop L for 4 return vias.



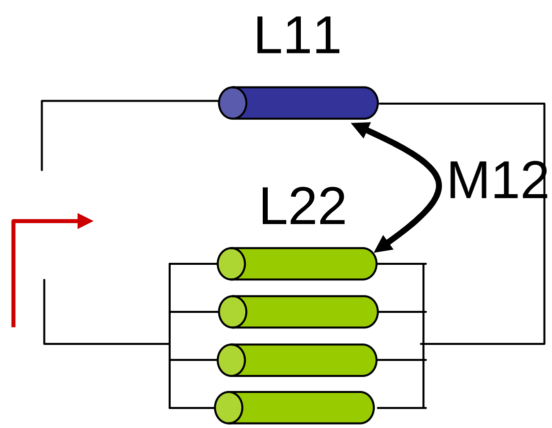
- Solving simultaneous voltage loop equations with symmetry simplifications leads to:

$$\mathbf{L_{loop} = 5/4^* (L11 - M12)}$$

- Generalizing:

$$\mathbf{L_{loop} = (n + 1)/n^*(L11 – M12)}$$

where n is the number of return vias



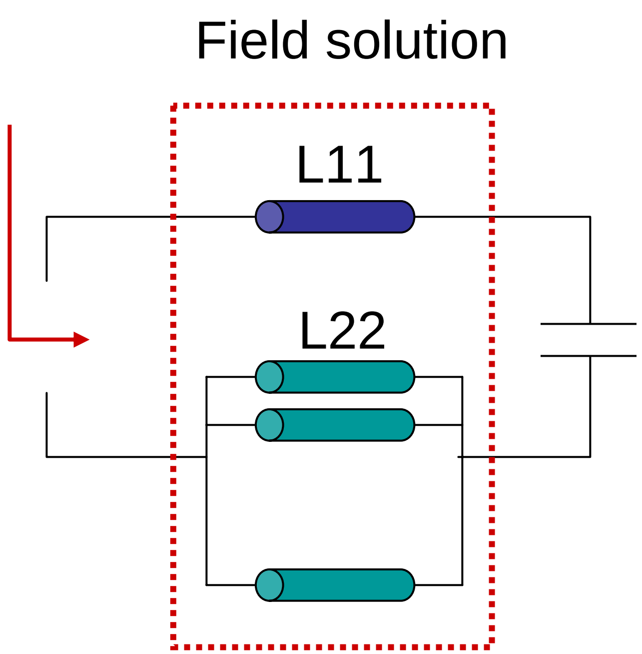
L11=L22=L33=L44=L55

- Error in loop L from ignoring M:

$$\mathbf{L_{loop} = (n+1)/n^*L11^*(1 - \color{red}{M12/L11})}$$

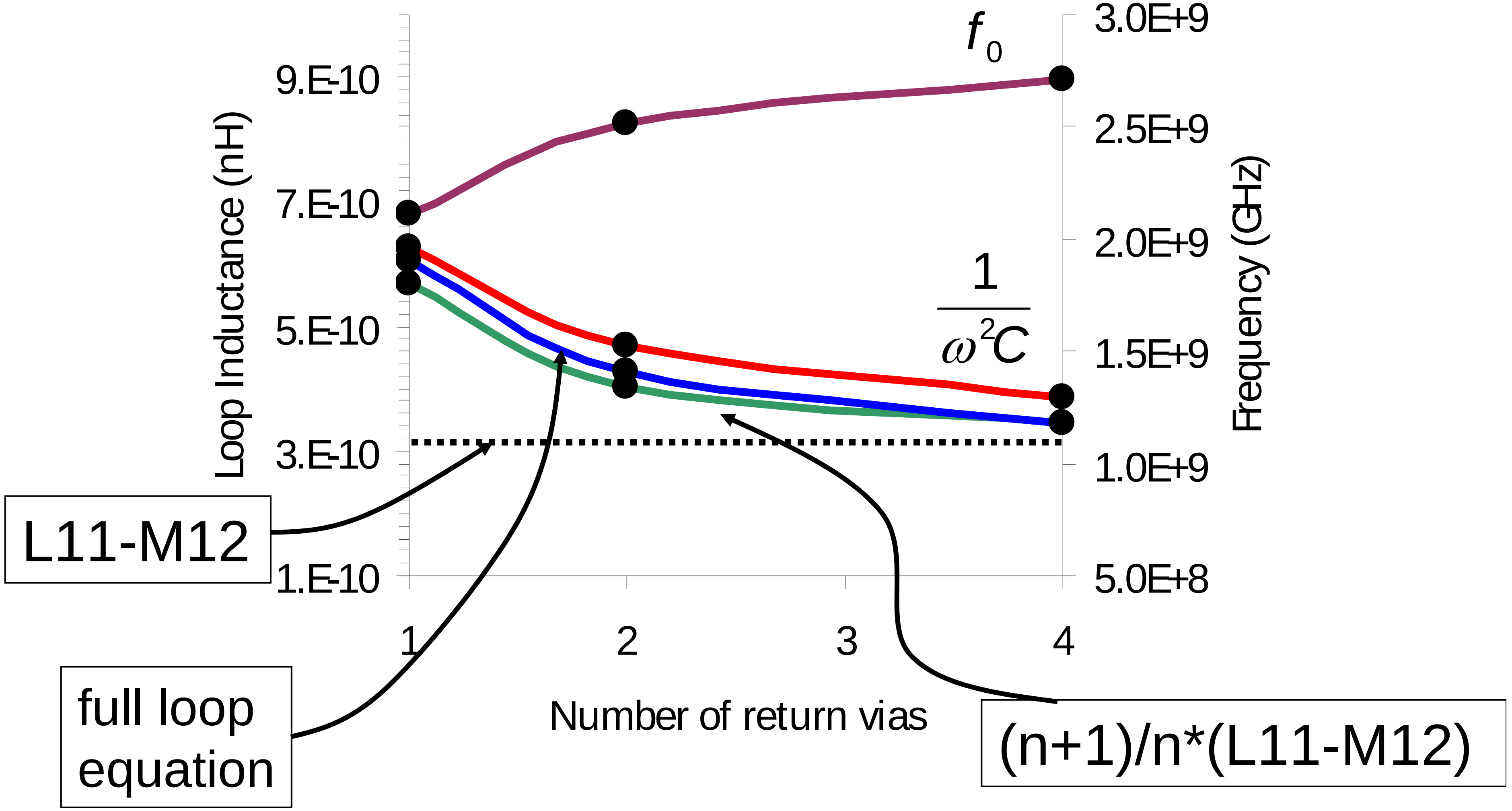
Loop Inductance (2)

- Solve for circuit model of multiple return vias (n=1,2,4)
- Calculate and compare loop L using:
    1) f_0 with fixed C
    2) Full loop equation from L matrix
    3) Simplified loop from L matrix



C = 10pF

Loop Inductance (3)

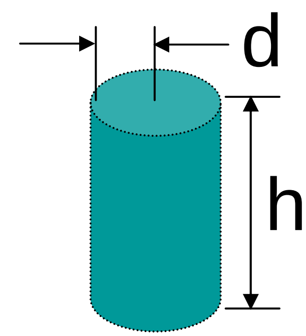


Via Partial Inductance

- Rosa[1] showed that the partial mutual L of two infinitely thin parallel wires is:

$$L = 5.08h\left[\ln\left(\left(\frac{h}{d}\right)+\sqrt{\left(1+\left(\frac{h}{d}\right)^{2}\right)}\right)-\sqrt{\left(1+\left(\frac{d}{h}\right)^{2}\right)}+\left(\frac{d}{h}\right)\right]$$

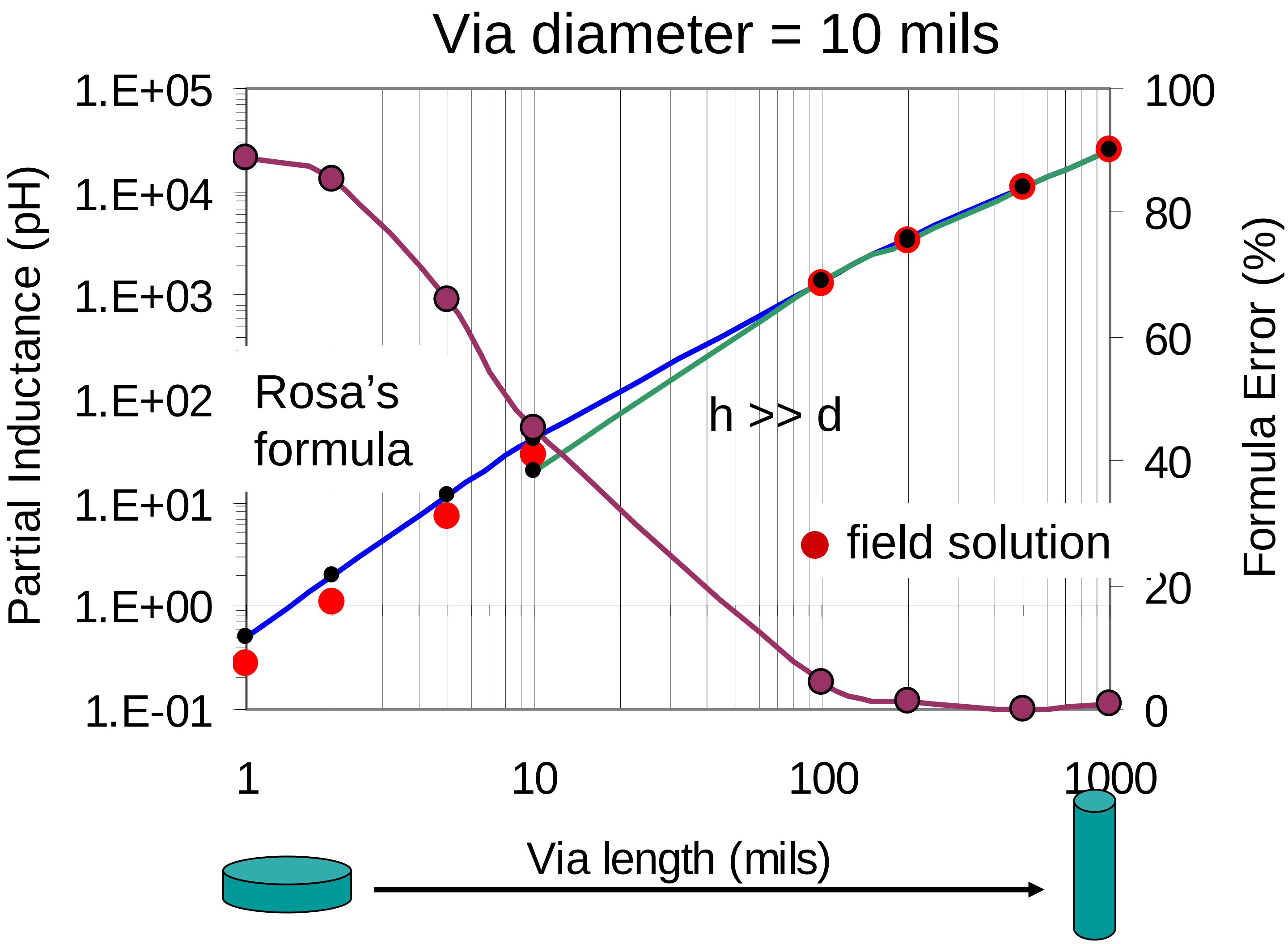
- This is equivalent to calculating the partial self L of a single wire with d=radius.
- For very long wires compared to their diameter (or separation) this simplifies to:



$$L = 5.08h\left[\ln\left(\frac{2h}{d}\right)-1\right]$$

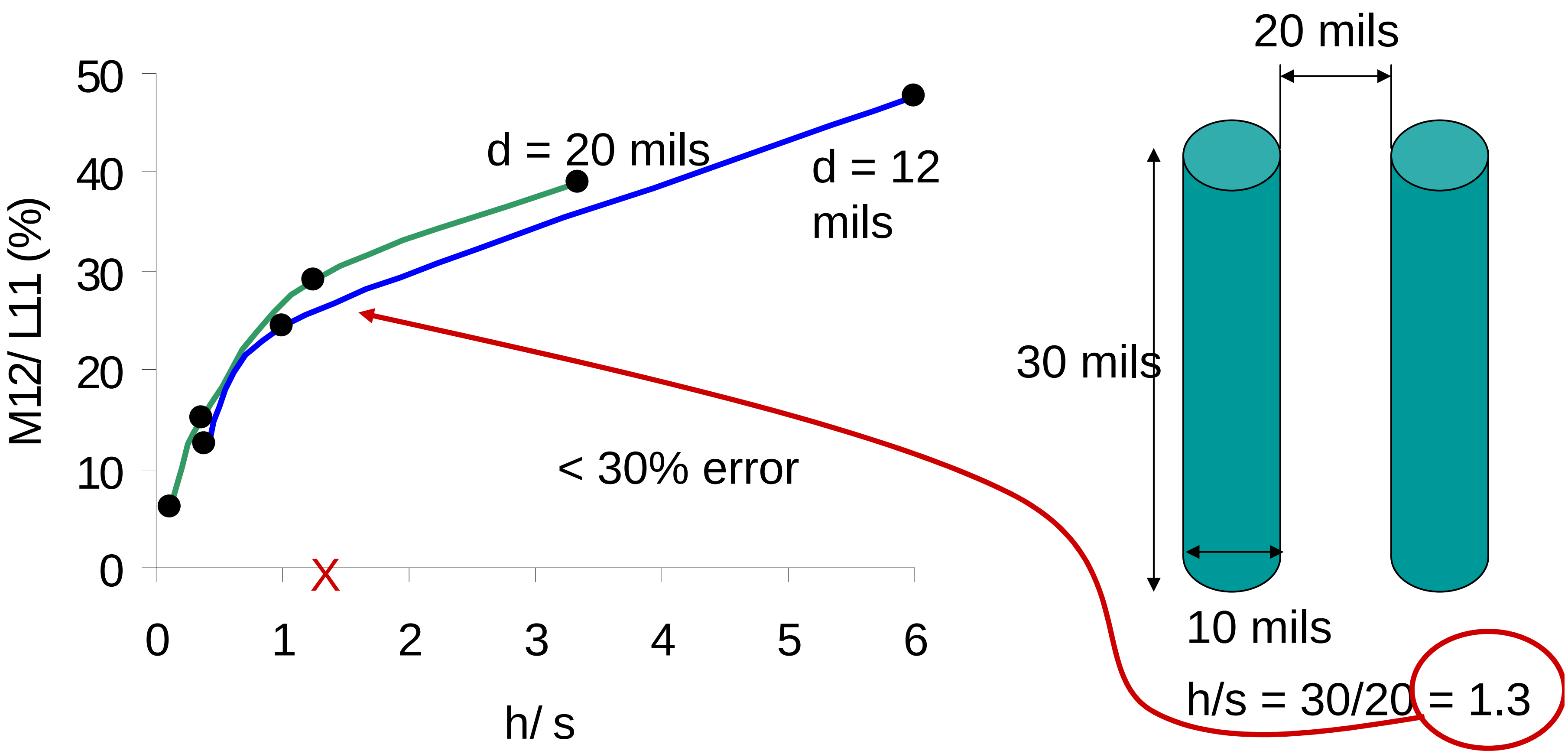
1. E. B. Rosa, *B. of S. Bull.* **4**, 301 (1907).

Via Partial Inductance (2)



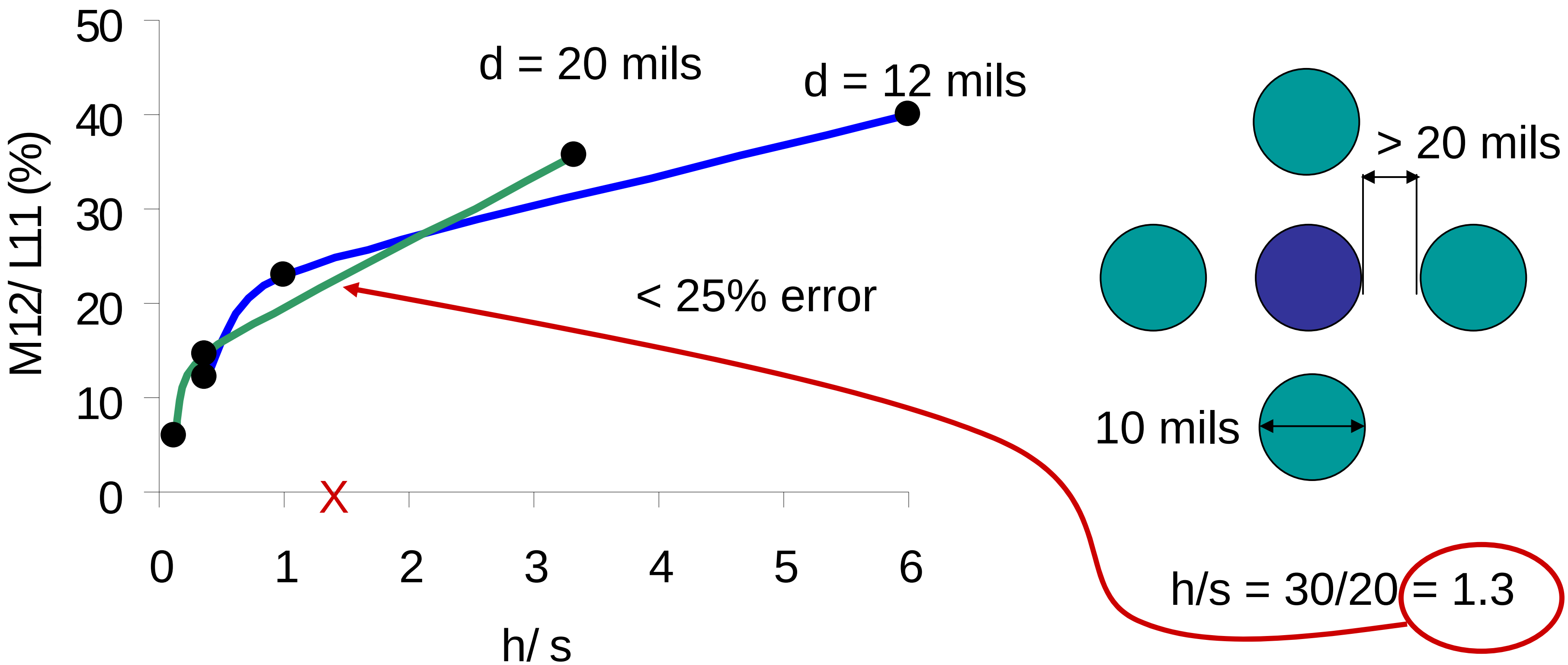
Case Study (1)

- Contribution of M to loop L for different length/separation ratios with 1 return via.



Case Study (2)

- Contribution of M to loop L for different length/separation ratios with 4 return vias.

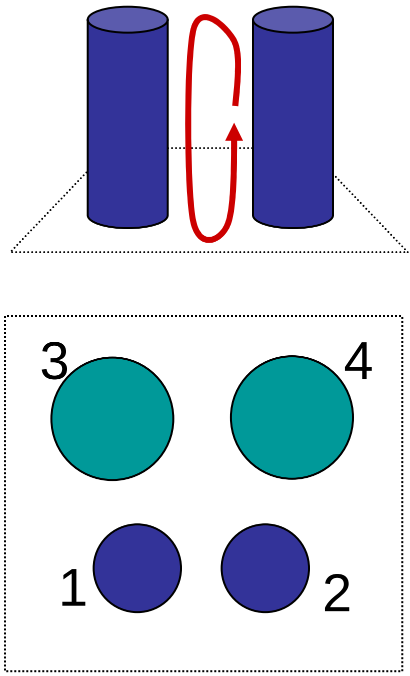


Via Measurements

•Test board consists of two via pairs on common plane

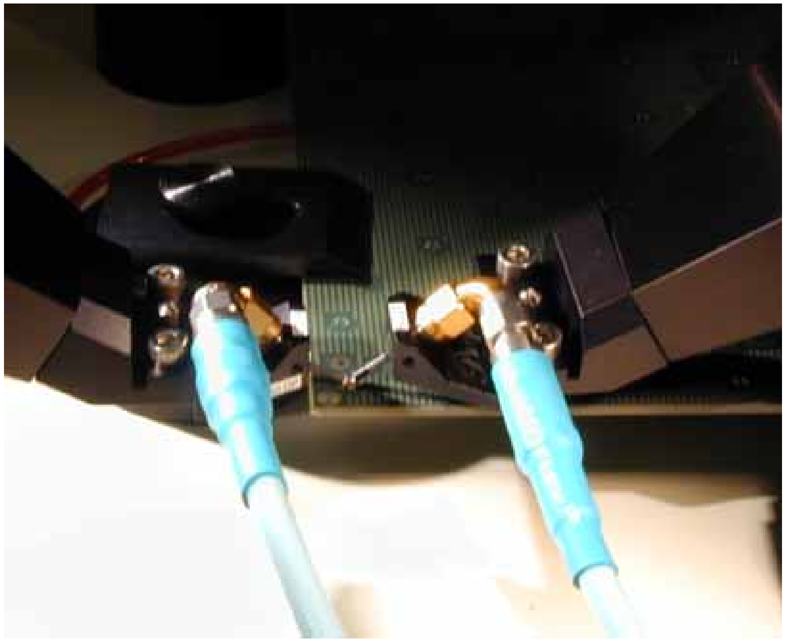
Side view:

Top view:



d=31 mils
s=70 mils

d=22 mils
s=54 mils

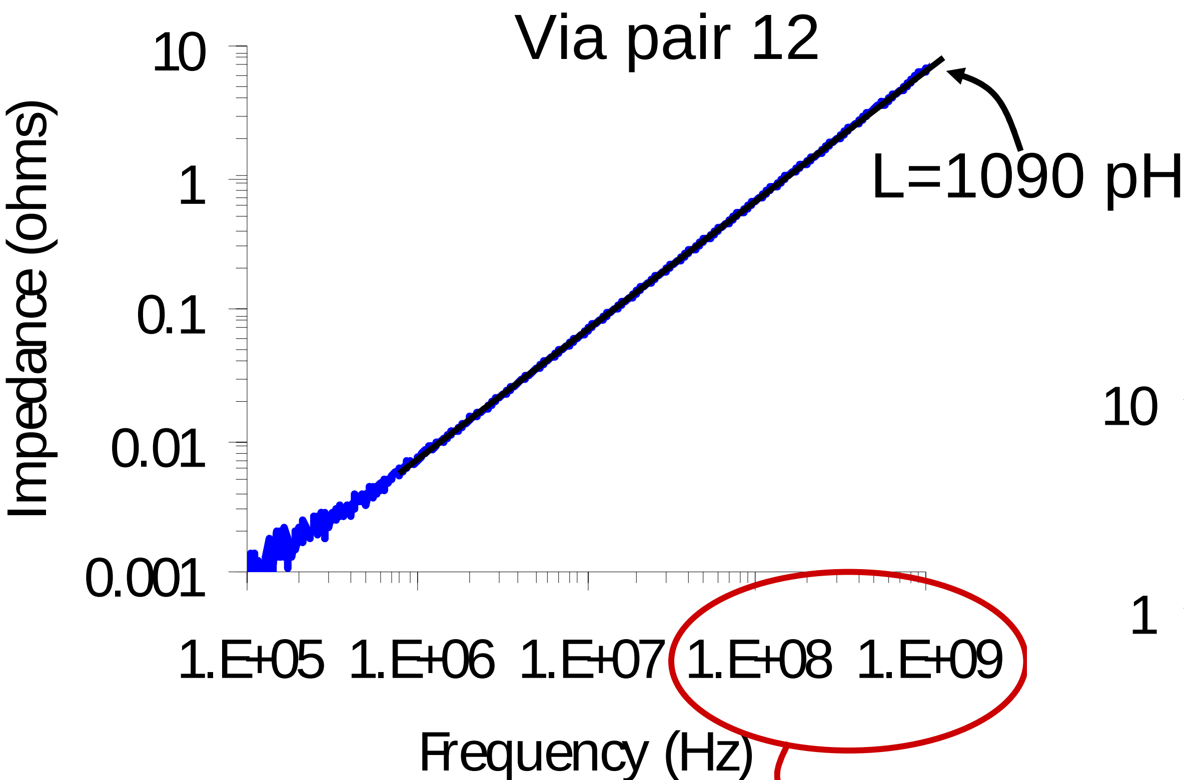


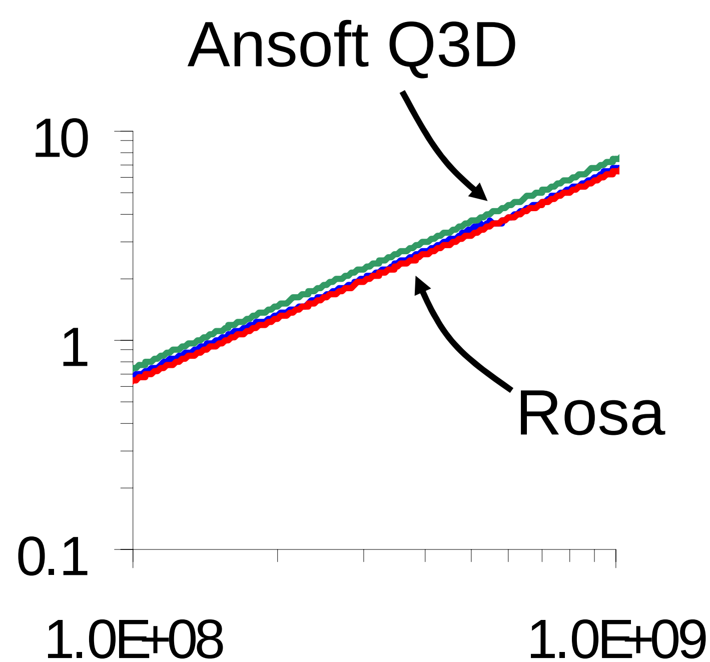
- Measurement setup: HP 4396B VNA

Via Measurements (2)

Via Pair	Measure (pH)	Ansoft Q3D (pH)	Rosa (pH)	Delta (%)
12	1090	1170	1018	6.6
34	1090	1333	878	19
24	920	1106	853	7.3
32	1370	1593	1134	17

Via Measurements (3)





Summary

- An approach to modeling vias for PCB applications was presented.
- A simple method for estimating the accuracy of the via model for a particular application was developed.
- Closed form expressions were presented for calculating the partial self L.
- These expressions were found to be accurate compared to 3D field solutions and lab measurements.

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Backup Slides

Calculating Loop Inductance

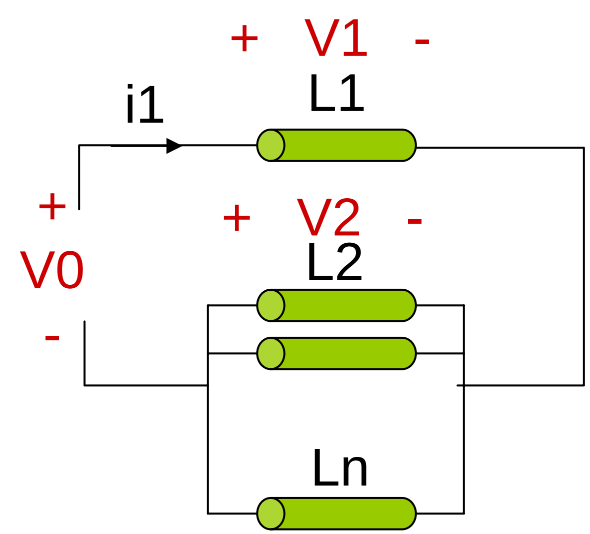
- Kirchoff's law around loop:

$$(1)\quad v1 = L1\frac{di1}{dt} - M12\frac{di2}{dt} - \ldots - M1n\frac{din}{dt}$$

$$(2)\quad v2 = -M21\frac{di1}{dt} + L2\frac{di2}{dt} - \ldots - M2n\frac{din}{dt}$$

$$(3)\quad V0 = L0\frac{di}{dt} = V1 + V2$$

$$(4)\quad i1 = I2 + i3 + \ldots + In$$

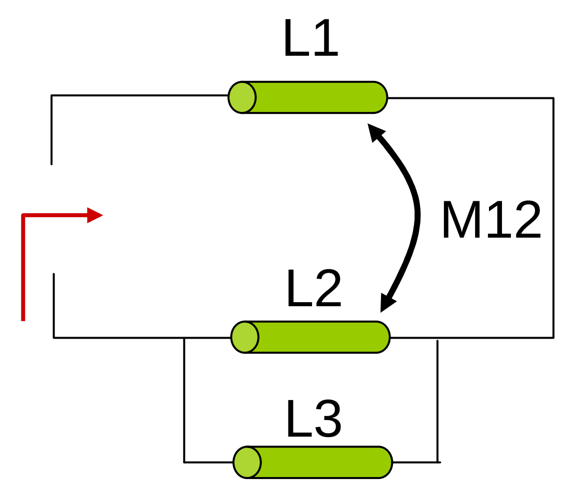


- Solve simultaneous equations

Calculating Loop Inductance (2)

- **Example:** Loop L for two return vias
- Solve simultaneous equations assuming:
  - L=L1=L2=L3
  - M12=M13

$$L0 = \frac{1}{2}\left(3 * L - 4 * M12 + M23\right)$$



- Further simplifying:
  - M=M12=M23

$$L0 = \frac{3}{2}\left(L - M\right) = (n+1)/n * (L - M)$$

Measuring Inductance

(1) $$S12 = 20 * \mathrm{Log}\left[\frac{2 * V2}{V1}\right]$$

(2) $$\frac{2 * V2}{V1} = \left(\frac{2 * \dfrac{Z_{dut} * 50}{Z_{dut} + 50}}{\dfrac{Z_{dut} * 50}{Z_{dut} + 50} + 50} \right) = \frac{Z_{dut}}{Z_{dut} + 25}$$

(3) $$S12 = a + bi \qquad Z_{dut} = c + di$$

(4) $$\mathrm{Im}[Z_{dut}] = \frac{25 * b}{1 - 2a + a^2 + b^2}$$

(5) $$\mathrm{L} = \frac{\mathrm{Im}[Z_{dut}]}{\omega}$$