
samtec
Spatial, Frequency, and Loading Effects on PDN Target Impedance
INNOVATIVE TECHNOLOGIES • SUDDEN SERVICE • GLOBAL REACH

SPEAKER

Ethan Koether

Sr. Signal and Power Integrity Engineer, Amazon Project Kuiper

Koether@amazon.com

Ethan Koether is a Sr. Signal and Power Integrity engineer with Amazon's Project Kuiper. He earned his master's degree in EECS in 2014 from the Massachusetts Institute of Technology. Ethan also spent seven years as a Hardware Engineer at Oracle. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

CO-AUTHORS

Kristoffer Skytte

Application Engineer Architect, Cadence

kskytte@cadence.com

Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. His recent efforts are on examining differences between measurement and simulation. He holds an M.Sc.EE. degree from the Technical University of Denmark.

Shirin Farrahi

Sr. Principal Software Engineer, Cadence

shirinf@cadence.com

Shirin Farrahi is working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

Mario Rotigni

Retired

mario.rotigni@ieee.org

Mario retried after a 45-year career in R&D working on micro-controllers and EMC for automotive applications. He has co-authored 22 papers about EMC of Integrated Circuits and is a member of the IEEE & IEEE EMC Society.

John Phillips

Sr. Principal Application Engineer, Cadence

phillips@cadence.com

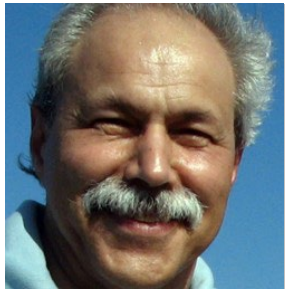
John has 30+ years experience working on SI, PI, and EMC challenges at the chip, board, and system level in applications including high-end computing and mil-aero. He holds an MSc. from Bolton University, UK. His current interests are SI/PI co-simulation and modelling for high-speed interfaces.

Abe Hartman

Principal Hardware Engineer, Oracle

abe.hartman@oracle.com

Abe works on system SI/PI at Oracle and has worked at Amphenol TCS, Juniper Networks, Enterasys, and GM. Abe holds a MS in EE from UMass-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, and a BS in both ME and EE from Kettering University in Flint, MI.



Istvan Novak

Principal SI/PI Engineer, Samtec

istvan.novak@samtec.com

Istvan works on advanced SI/PI designs at Samtec and was previously a Distinguished Engineer at SUN later Oracle. He introduced the first 25µm power-ground laminates for large rigid PCBs and worked to create a series of low inductance, controlled-ESR capacitors. He is a Life Fellow of the IEEE with 25 patents, author of two books on PI, teaches SI/PI courses, and maintains a popular SI/PI website. He was named Engineer of the Year at DesignCon 2020.

GOALS

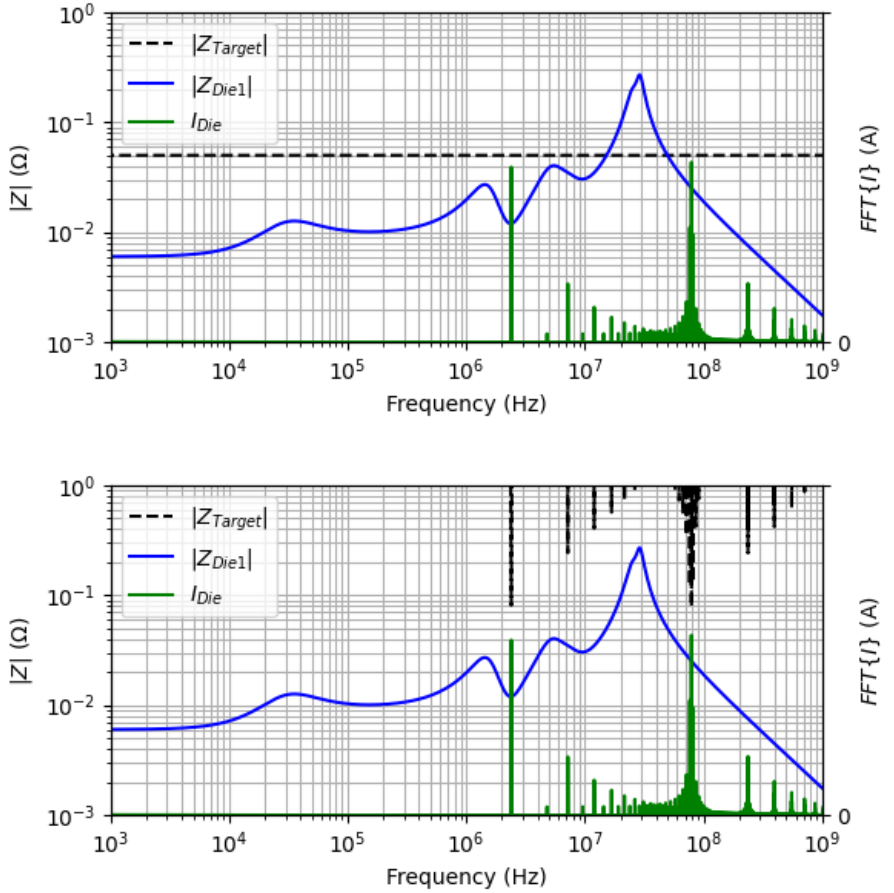
- Compare single point-of-load PDNs and PDNs feeding multiple parallel loads
- Correlate bandwidth changes from the DC source pads to IC pads on the PCB
- Present guidelines to avoid over-designing PDNs
- Understand considerations for complex, multi-load power delivery designs
- Update PDN target impedance methodology to be a function of frequency and spatial position

TARGET IMPEDANCE

- PI design target for systems:

$$|Z_{PDN}| \leq \Delta V_{tol}/\Delta I_{max} \text{ for } 0 \leq f \leq f_{max}$$

- Different flavors of “target impedance” metric [1]
- Assumes minimum-phase, LTI system [2]
- Can meet target impedance but see voltage fluctuation generated outside of spec [3] [4][5][6]
- Not clearly extendable for multi-load or multi-power domain PDN
- Can be unrealistic target to meet over entire frequency range

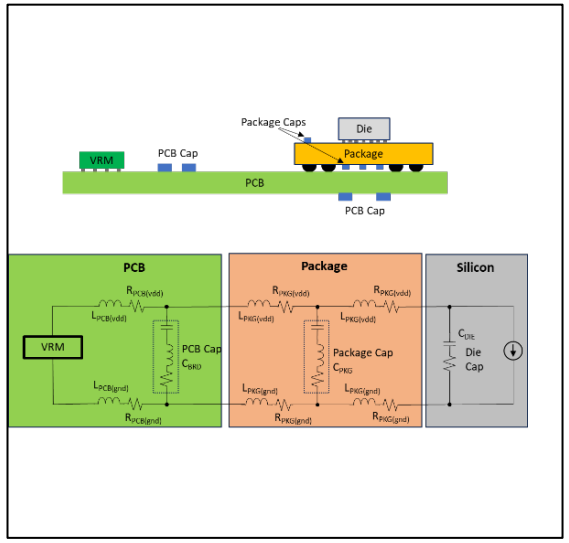


[1] Improved Methodology to Accurately Perform System Level Power Integrity Analysis Including an ASIC Die (DesignCon 2022)
[2] Frequency-Domain Power Distribution Measurements - An Overview (DesignCon 2003)
[3] Aperiodic Resonant Excitation of Microprocessor Power Distribution Systems and the Reverse Pulse Technique (IEEE 2002)
[4] Target Impedance is not Enough (SIJ 2019)
[5] Target Impedance Limitations and Rogue Wave Assessments on PDN Performance (DesignCon 2015)
[6] Systematic Estimation of Worst-Case PDN Noise: Target Impedance and Rogue Waves (Quietpower 2015)

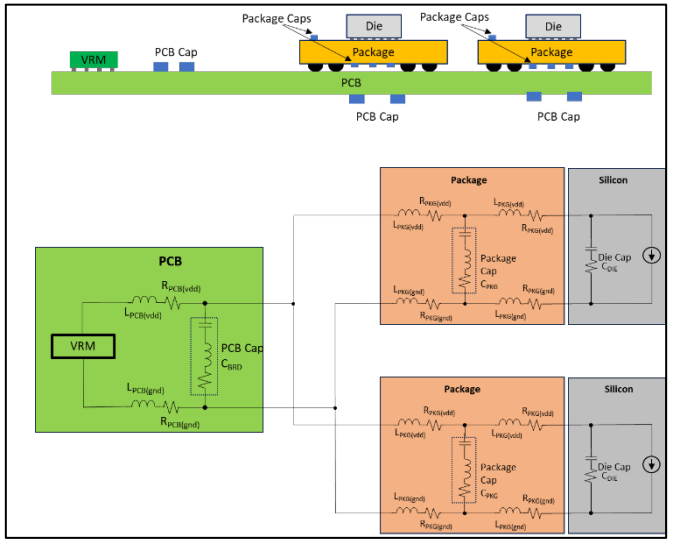
POL AND MULTI-LOAD PDN LADDER MODELS

- POL PDN and two-load PDN
- Transient current at die-level of PDN (Cadence SystemPI®) is filtered by die-package resonances and PCB impedance before appearing on the board or at neighboring die

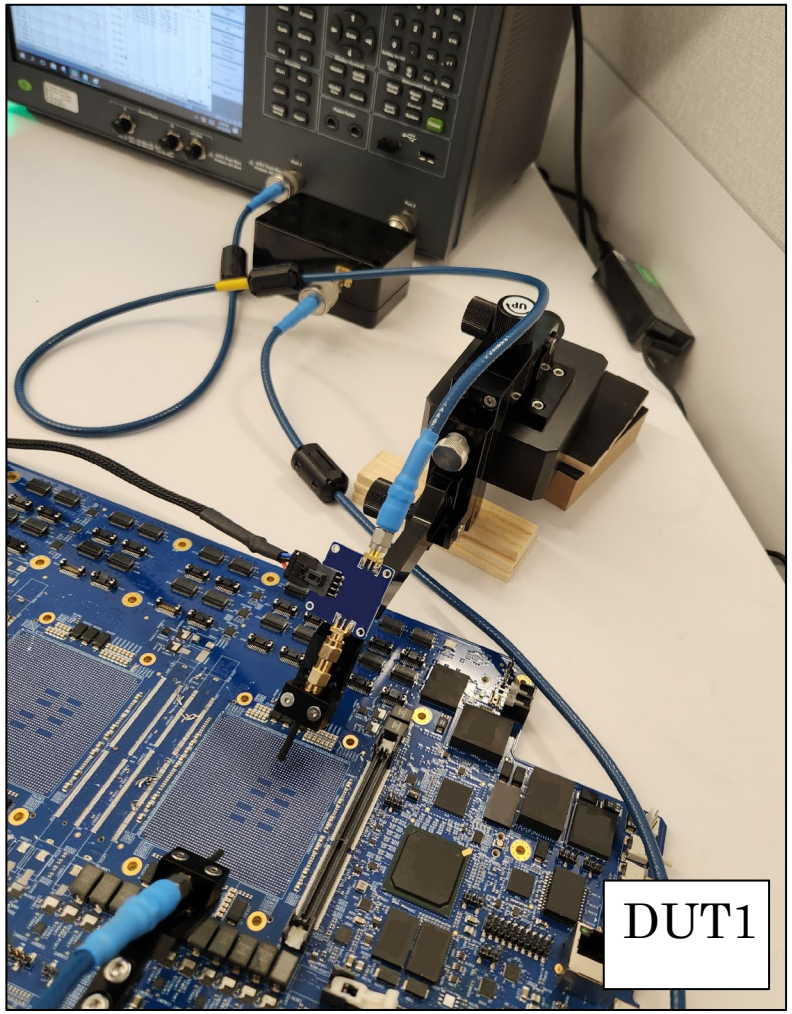
POL (Single-Load PDN)

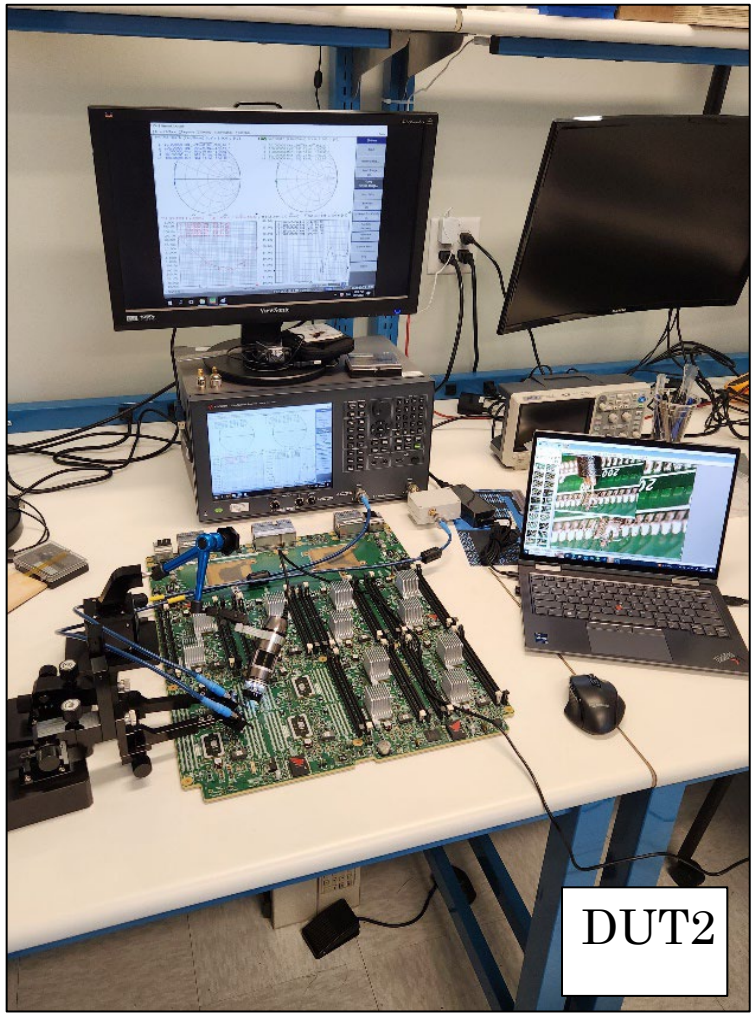


Multi-Load PDN



SETUP



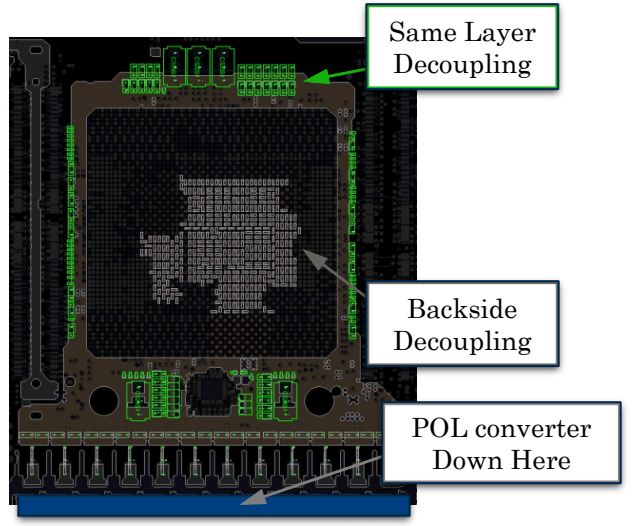


DEVICES UNDER TEST

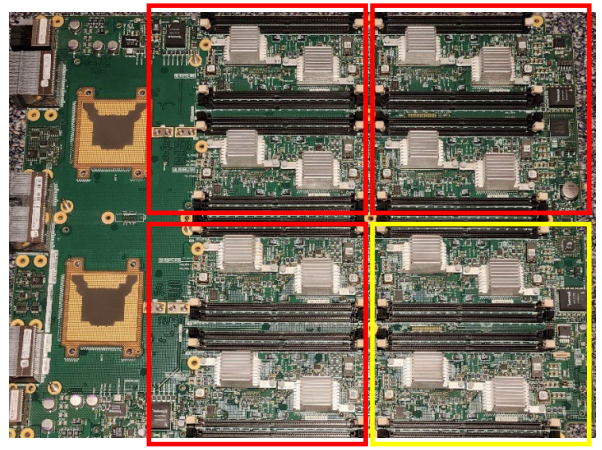
- DUT1: POL, 250A AI application
- 30-layer stackup, 3 power layers, half of layers GND
- BGA: 430 pwr pins, 1400 GND pins
- 500 decoupling caps, 5 different values
- <0.25nH net inductance seen by IC
- <1mOhm impedance 10kHz - 3MHz (seen looking into pcb BGA)

- DUT2: Multi-load, high-computing application
- 32 DIMM sockets driven by 16 memory driver chips, split into 4 power planes, each with 80A DCDC converter
- 28-layer stackup multiple 2oz power layers
- 8x 1000uF, 27x 330uF by VR
- 40x 47uF near DIMM sockets
- 238x 4.7uF near memory controllers

DUT1



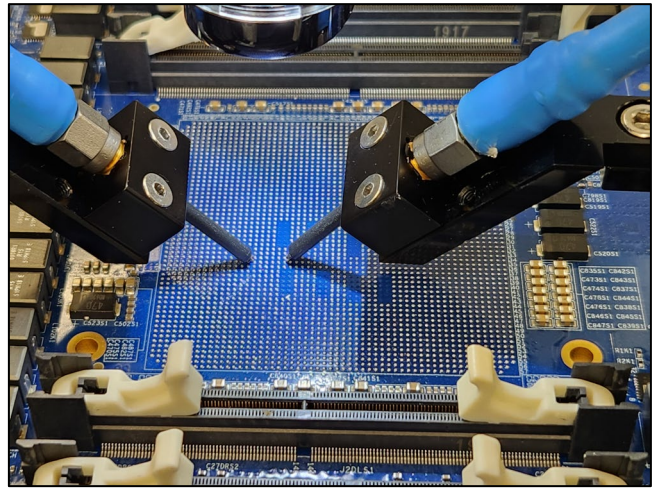
DUT2

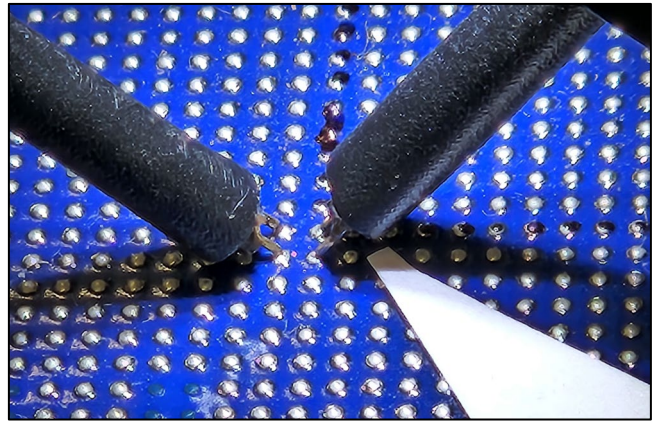


	VRM	Decoupling	ASICs
DUT1	Mounted, not powered	Mounted	Not mounted
DUT2	Mounted, not powered	Mounted	Mounted

MEASUREMENT SETUP

- Keysight E5061B VNA, 2-port shunt thru measurement configuration
- PacketMicro RP-GR-121510 probes and positioner
- Microscope
- Common mode choke toroid for use up to 10MHz
- SOLT calibration (including Isolation) to end of cables.
- Landing probes not de-embedded
  - +/-40pH - 50pH mutual probe-tip loop inductance @1MHz @1mm
  - Negligible phase rotation from probes in this frequency range [7]
- 5Hz IFBW
- 10dBm source power

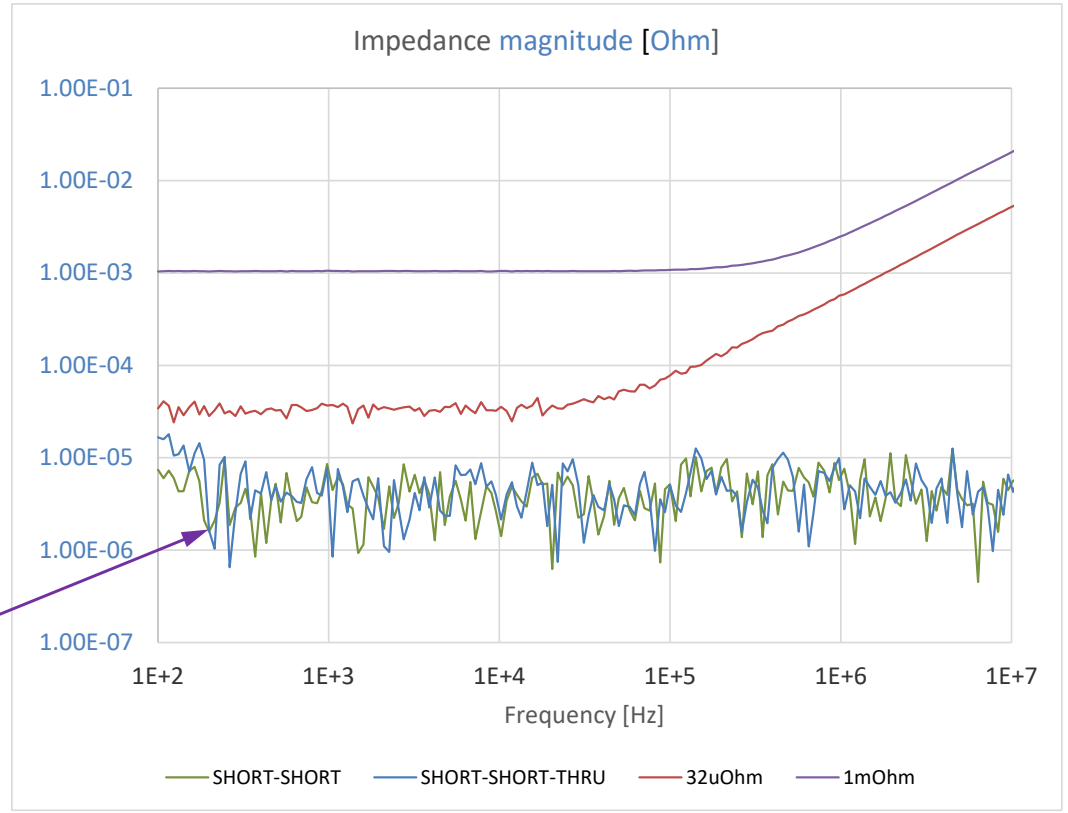




[7] Impact of Finite Interconnect Impedance including Spatial and Domain Comparison of PDN Characterization (DesignCon 2024)

NOISE FLOOR INVESTIGATION

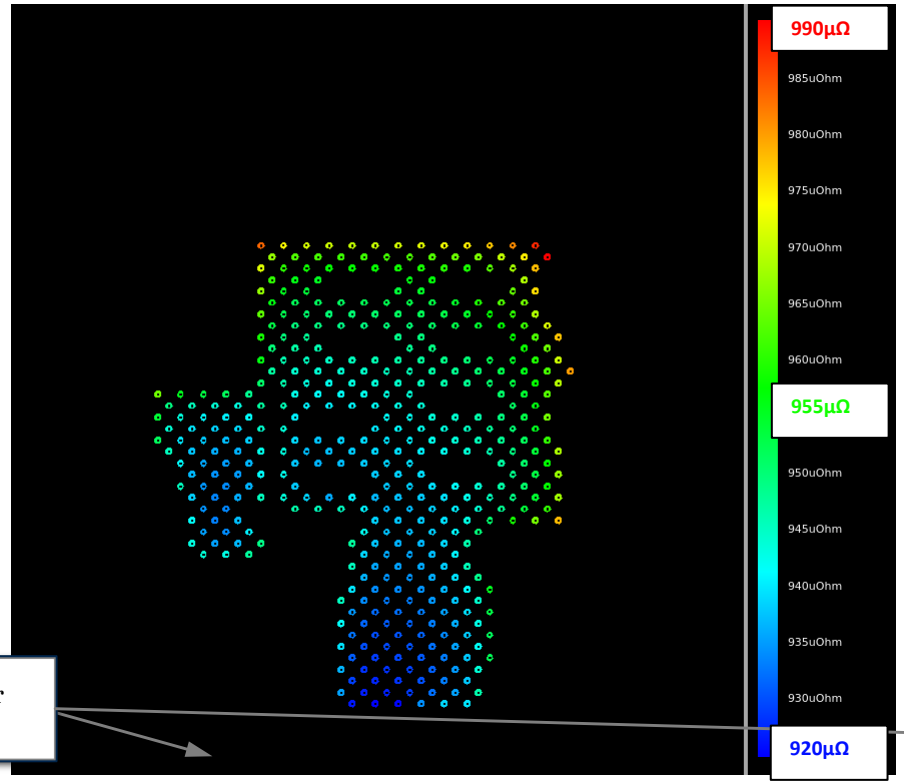
- 5Hz IFBW
- 10dBm source power
- No averaging
- SOLT calibration (including Isolation)
- No external active device
- DUT data shown in this paper used this setup
- **<1μΩ noise floor achievable!**



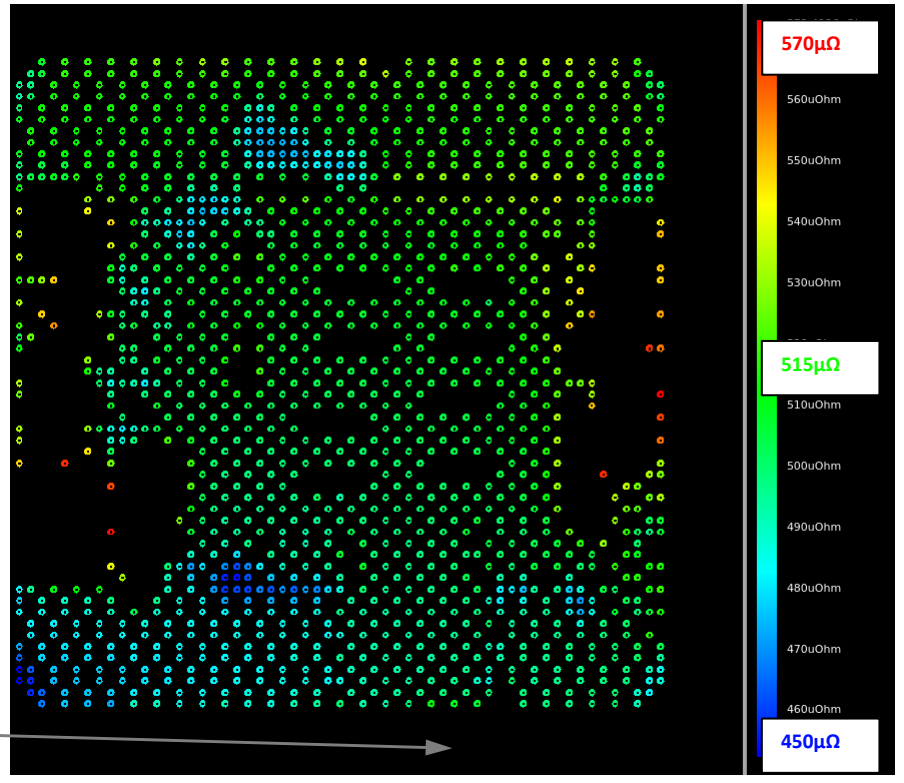
< 10μΩ noise floor

CADENCE POWERDC®

- Conductivity per pin pair
- Top: Power domain pins see variable resistance path to POL due to variation in geometric distance
- Bottom: Variation in GND BGA pin resistance



POL converter Down Here

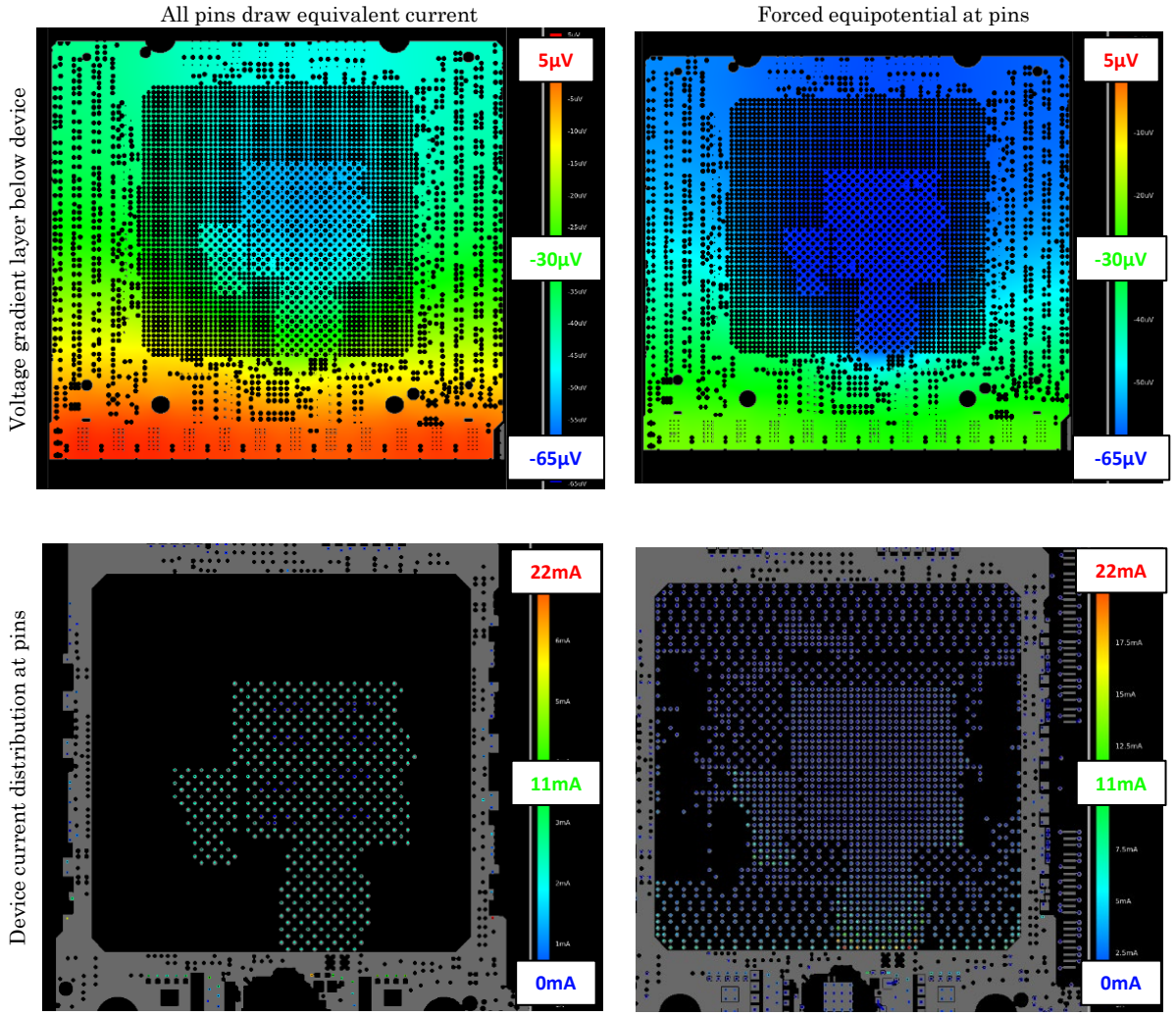


CADENCE POWERDC®

Investigations into spatial filtering:

- Equipotential Load vs. Equivalent Current Distribution

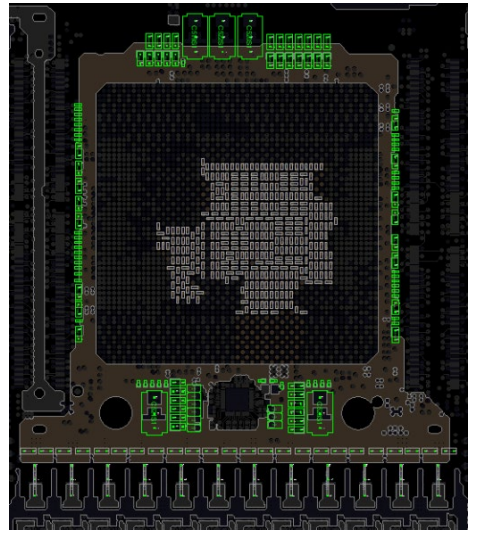
- All power pins draw equivalent amount of current
- Ideal forced equipotential on BGA power pins
- Uniform voltage supplied at BGA
- Current is purely function of path resistance
- 3x increase in max current per pin nearest POL

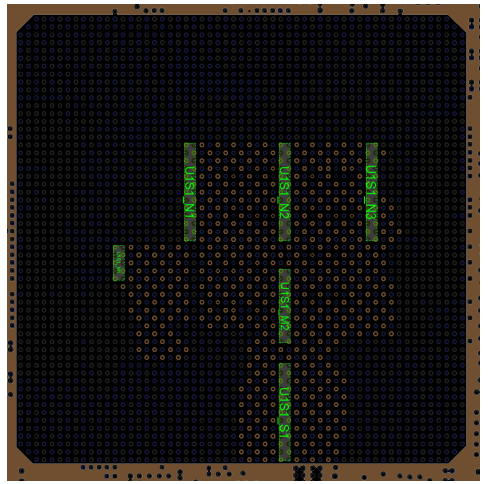


CADENCE POWERSI®

Simulation Setup:

- Hybrid solver
  - Wanted to see what quality correlation achievable with this faster simulator versus full 3D simulator used in [7].
- Capacitor modeling:
  - S-parameter models used where available from vendors
  - R-L-C models used where satisfactory vendor s-parameter models were not available

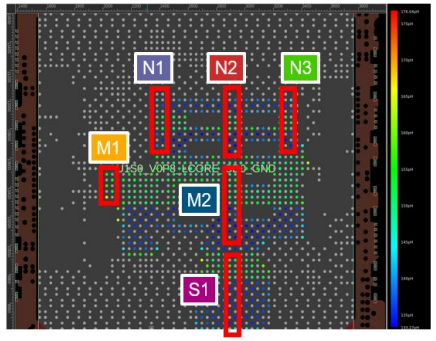


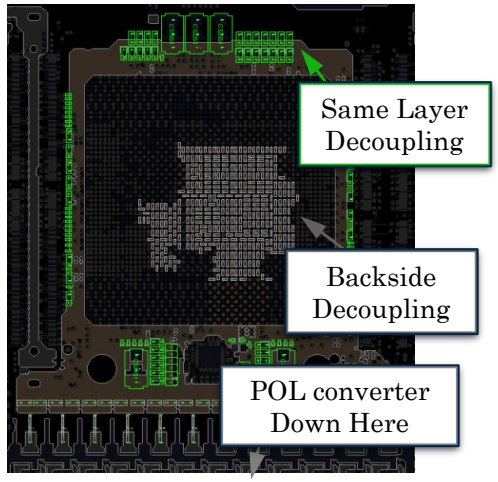


[7] Impact of Finite Interconnect Impedance including Spatial and Domain Comparison of PDN Characterization (DesignCon 2024)

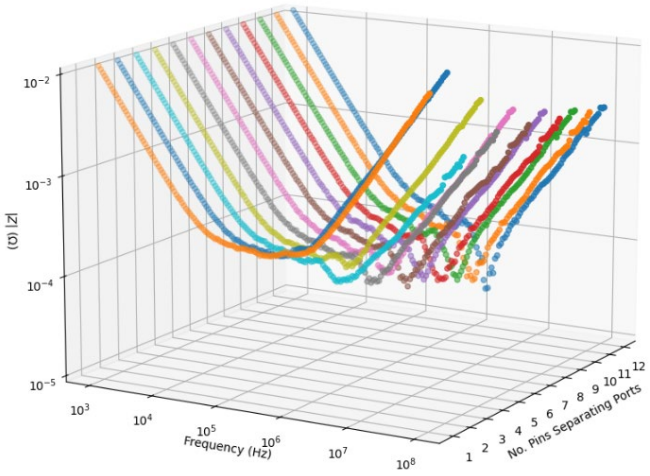
MEASUREMENT TO POWERSI SIMULATION CORRELATION

- Self-impedance – to – transfer impedance
- N2 region simulations and measurements as pin spacing between probe landings is increased [8]
- As probes separate: Capacitance (no change), resistance (↓), inductance (↓)

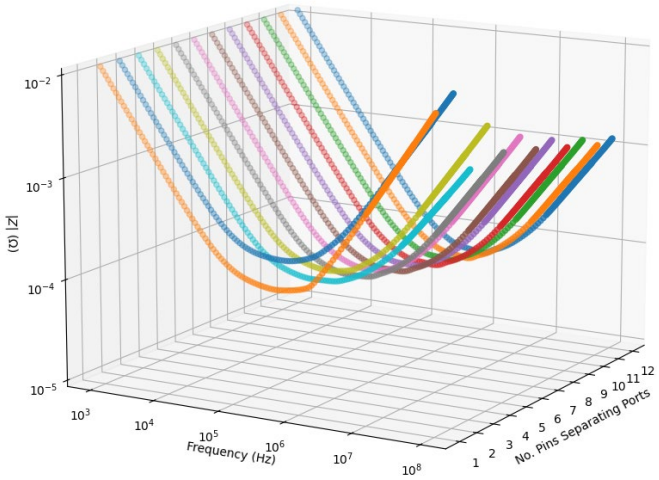




Measured Data:



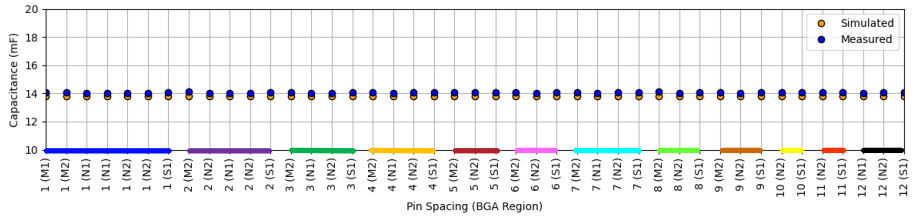
Simulated Data:

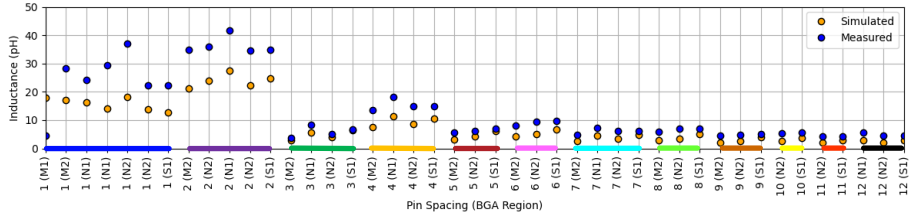


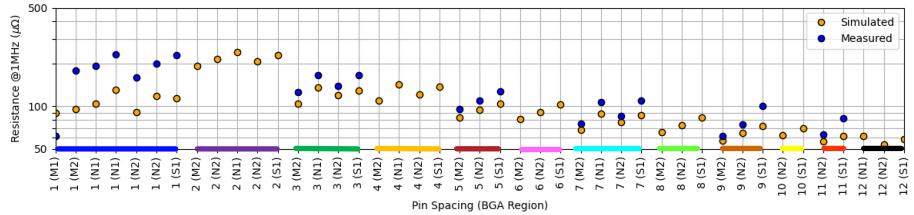
[8] Determining the Requirements, Die vs. Package vs. Board: Multi-level PDN Design (DesignCon 2025)

POWERSI SIMULATION CORRELATION

- Capacitance: consistent between all datasets
  - No variation expected or seen due to variation of observer
- Inductance:
  - Highest in self-impedance cases
  - Larger disagreement between simulated and measured data due to probe tip coupling
  - Probe tip coupling falls off as probes separate
  - Little difference between the different self-impedance cases, likely due to decoupling on the opposite side of the BGA
- Resistance:
  - Highest in self-impedance cases
  - Trends lower as probe landings separate [9]







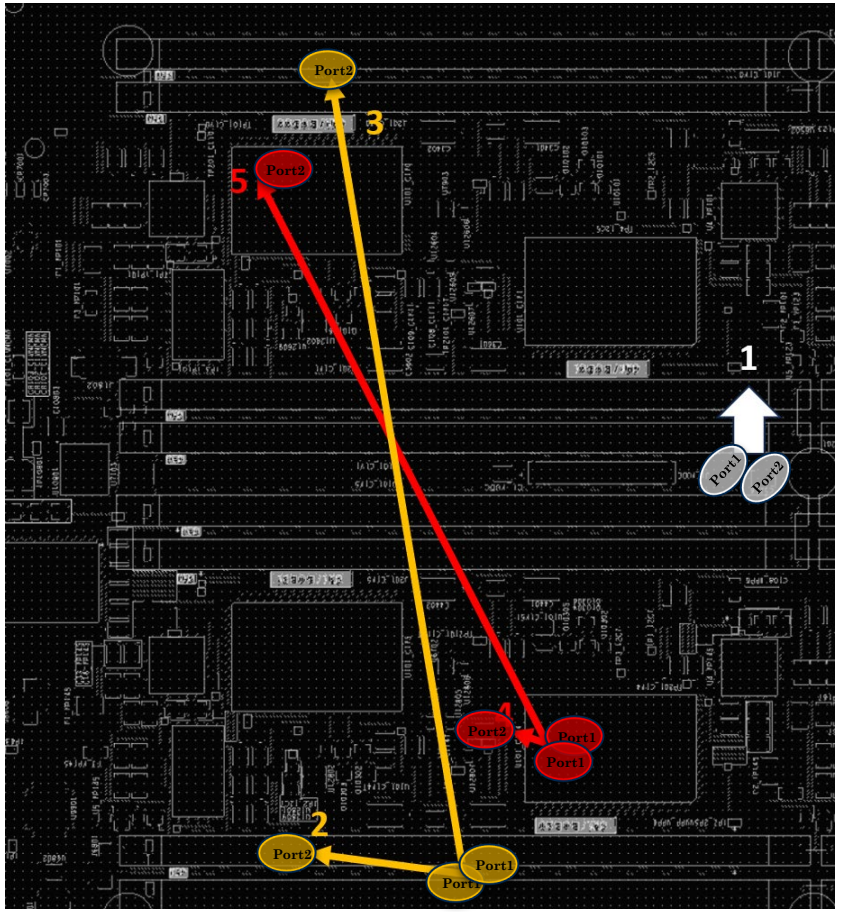
[9] 3D Connection Artifacts in PDN Measurements (DesignCon 2023)

PDN SPATIAL FILTERING SETUP

- DUT2: Multi-load, high-computing application
- 32 DIMM sockets driven by 16 memory driver chips, split into 4 power planes, each with 80A DCDC converter
- 283-layer stackup multiple 2oz power layers
- 8x 1000uF, 27x 330uF by VR
- 40x 47uF near DIMM sockets
- 238x 4.7uF near memory controllers

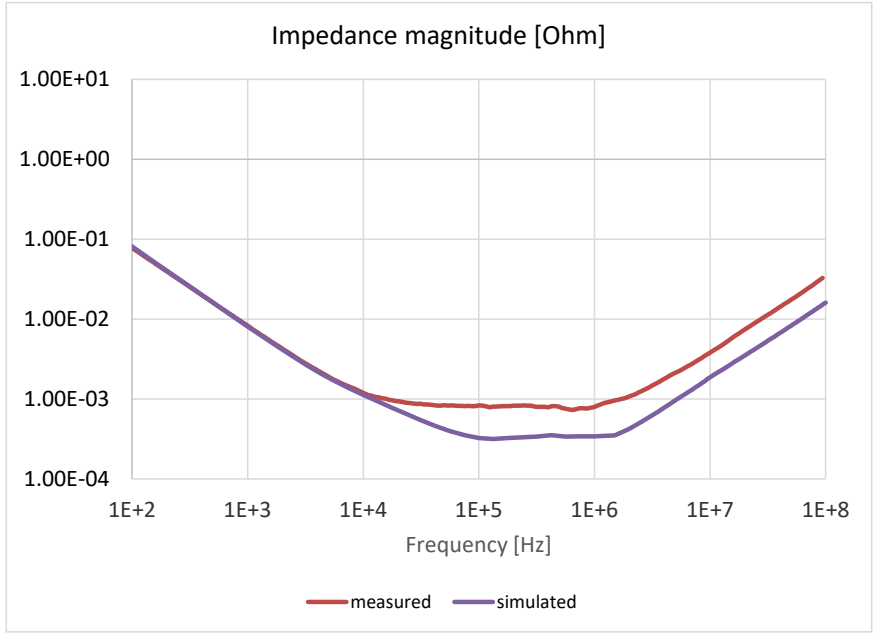
- Measurement locations:

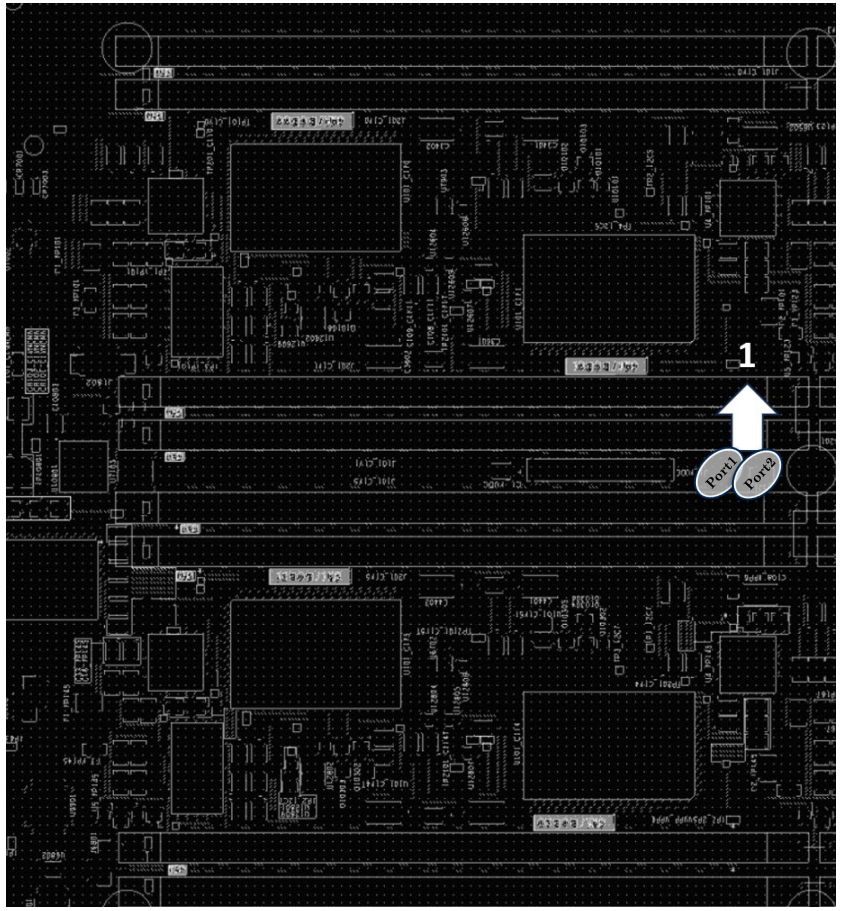
1. Core vias for top-bottom self-impedance probing
2. Top-side DIMM sites for “near” transfer-impedance probing
3. Top-side DIMM sites for “far” transfer-impedance probing
4. Bottom-side Memory Driver sites for “near” transfer impedance probing
5. Bottom-side Memory Driver sites for “far” transfer impedance probing



SELF IMPEDANCE MEASURED AND SIMULATED

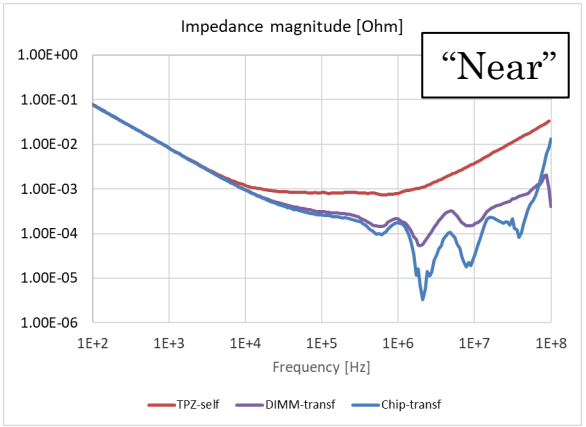
- Low frequency capacitive region correlates
- > 10kHz: expected deviation between measurement and correlation due to hybrid PowerSI solver

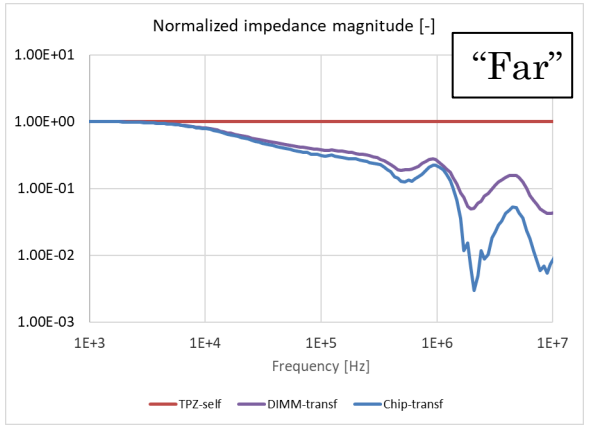


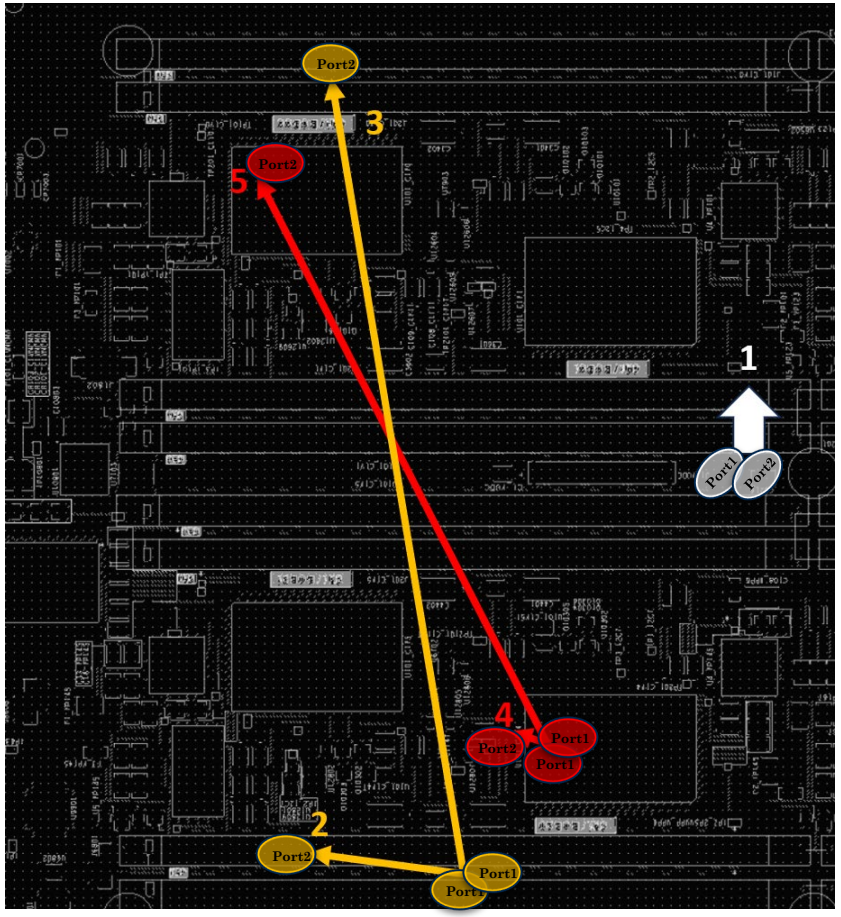


SPATIAL FILTERING MEASUREMENTS AND SIMULATIONS

- Normalized transfer-impedance to self-impedance to estimate filtering transfer function: $\frac{Z_{21}}{Z_{11}} \sim \left(\frac{v_2}{i_1}\right) \cdot \left(\frac{i_1}{v_1}\right) = \frac{v_2}{v_1}$
- Cut-off frequency ~10kHz for both DIMMs and Memory Drivers
- < 10kHz: little deviation showing effective "lumped" region. Filtering here due to DC resistance of planes
- 10 kHz – 1 MHz: RC filtering region due to plane's DC and 'skin' resistances and net capacitance on plane
- Transfer function slope ~10dB/dec, $\propto\sqrt{f}$, (skin resistance)
- SRF of 47µF and 4.7µF MLCCs visible







CONCLUSIONS

- Good simulation/measurement correlation for two high-power DUTs
- Achieved 10μΩ noise floor with two port shunt-thru impedance setup with crosstalk calibration (isolation)

  Noise floor can be reduced to 1μΩ with longer collection times

- Showed spatial filtering effects of the passive PDN and their physical roots
- Low frequency RC cutoff due to net capacitance and plane resistance in ~10kHz range
- SRF of PCB and package-level MLCCs appear in high frequency ranges of the self and transfer impedances seen from the PCB
- Target impedance methodology can be adapted and optimized for individual applications as we consider the different noise sources and filters in a complex system PDN

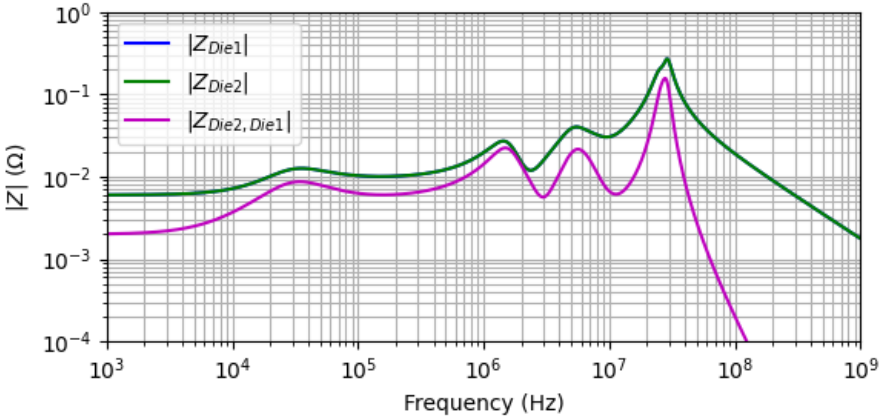
THANK YOU

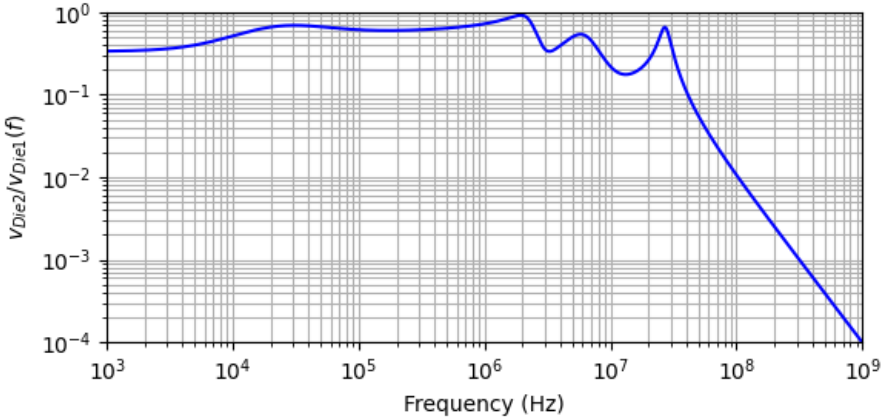
QUESTIONS?

KOETHER@AMAZON.COM, KSKYTTE@CADENCE.COM, PHILLIPS@CADENCE.COM, SHIRINF@CADENCE.COM, ABE.HARTMAN@ORACLE.COM, MARIO.ROTIGNI@IEEE.ORG, ISTVAN.NOVAK@SAMTEC.COM

FILTERING BETWEEN DIES IN MULTI-LOAD PDN

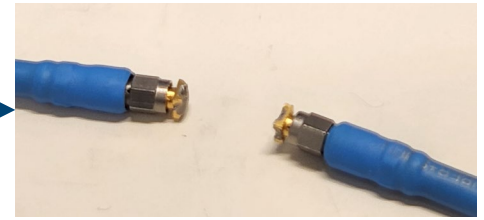
- Noise between dies attenuated due to low-pass filtering
- Noise coupled between dies:
  - Content above package-die resonance highly attenuated
  - Content in package-dominated PDN frequency range less attenuated
  - Content in frequency ranges where PDN is PCB-dominated or VR-dominated sees little attenuation

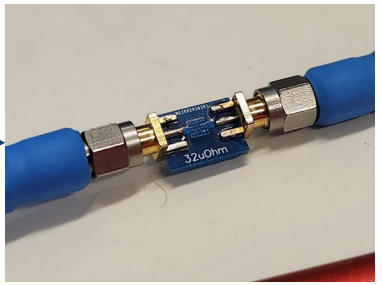


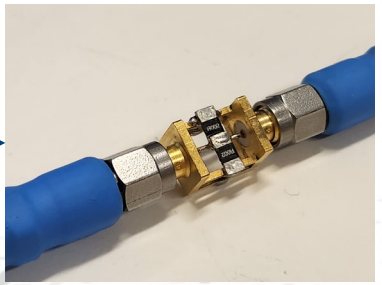


NOISE FLOOR INVESTIGATION

- Aimed to see how far noise floor could be reduced using E5061B VNA
- SOLT calibration (including Isolation) to end of coax cables
- Some of the reference pieces
  - SMA-SMA SHORT
  - SMA-SMA SHORT-THRU
  - 32uOhm
  - 1mOhm
- Setup variations
  - No external active device
  - 20dB low-noise preamplifier Port2
  - 20dBm power booster Port1
  - 20dBm power booster Port1. 20dB low-noise preamplifier Port2

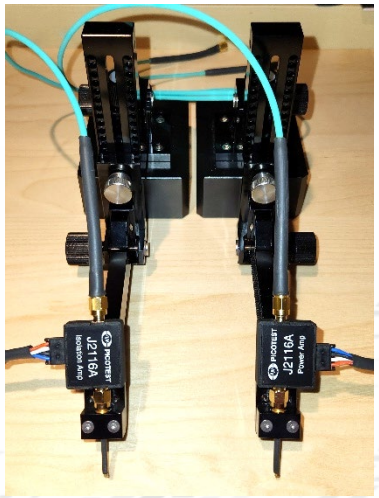


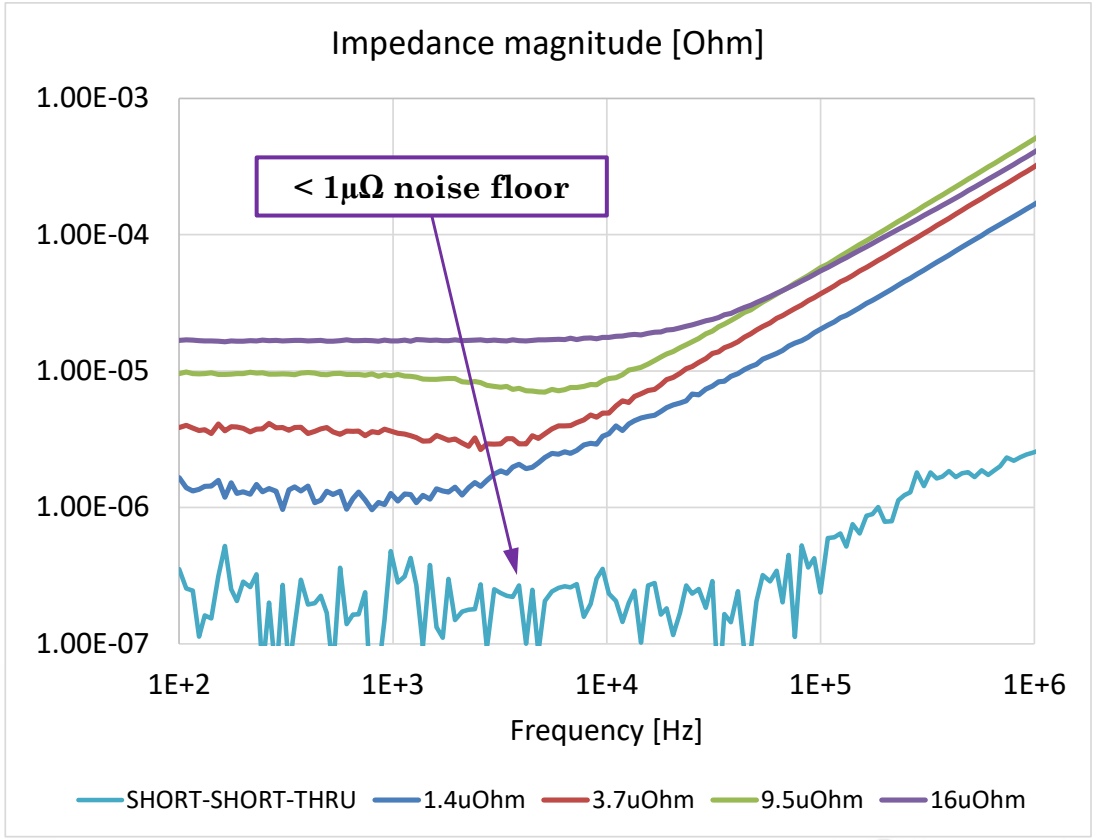




NOISE FLOOR INVESTIGATION

- 1Hz IFBW
- 0dBm source power
- No averaging
- SOLT calibration (including Isolation)
- 20dB 20dBm power booster on Port1
- 20dB low-noise pre-amplifier on Port2

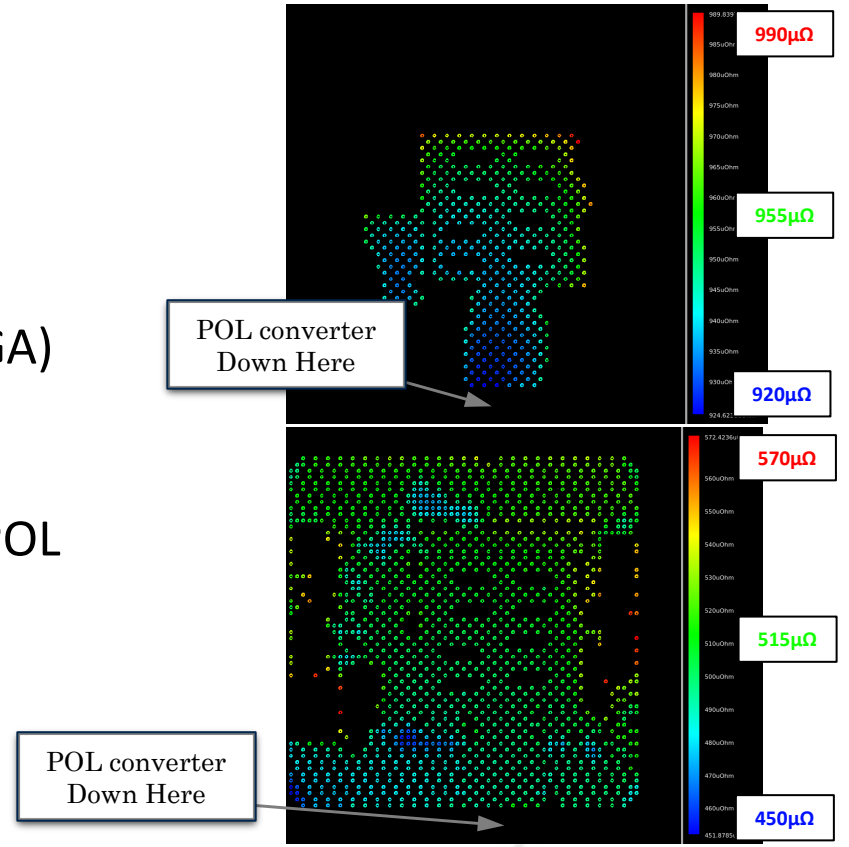




POWERDC® CONDUCTIVITY PER PIN PAIR

- DUT1: POL, 250A AI application
  - 30 layer stackup, 3layers power, half of layers GND
  - BGA: 430 pwr pins, 1400 GND pins
  - 500 decoupling caps, 5 different values
  - < 0.25nH net inductance seen by IC
  - < 1mOhm impedance 10kHz - 3MHz (seen looking into pcb BGA)

- DC Test 1: DC Resistance seen by pins
  - Top plot: Power domain pins see variable resistance path to POL due to variation in geometric distance to POL ranging from 920µΩ (blue) - 955µΩ (green) - 990µΩ (red)
  - Bottom plot: GND BGA pins' resistances vary similarly from 450µΩ (blue) - 515µΩ (green) - 570µΩ (red)

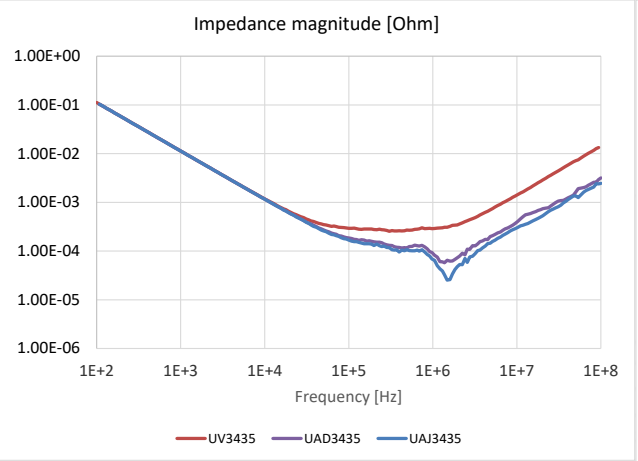


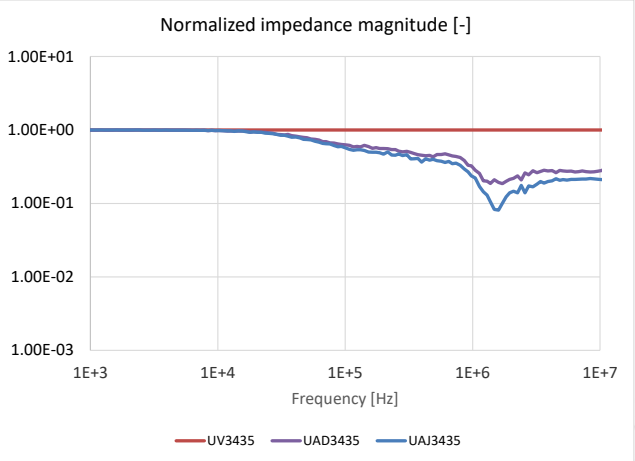
SPATIAL FILTERING EFFECT

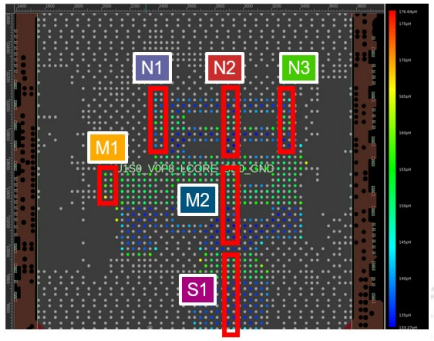
- Normalized transfer-impedance to self-impedance in order to estimate filtering transfer function:

$$\frac{Z_{21}}{Z_{11}} \sim \left(\frac{v_2}{i_1}\right) \cdot \left(\frac{i_1}{v_1}\right) = \frac{v_2}{v_1}$$

- Cutoff frequency ~30kHz for both BGA regions
  - <30kHz: little deviation showing effective "lumped" region. Filtering here due to DC resistance of planes
    - 30kHz – 800kHz: RC filtering region due to plane's DC and 'skin' resistances and net capacitance on plane
  - Transfer function slope ~10dB/dec, $\propto \sqrt{f}$, (skin resistance)



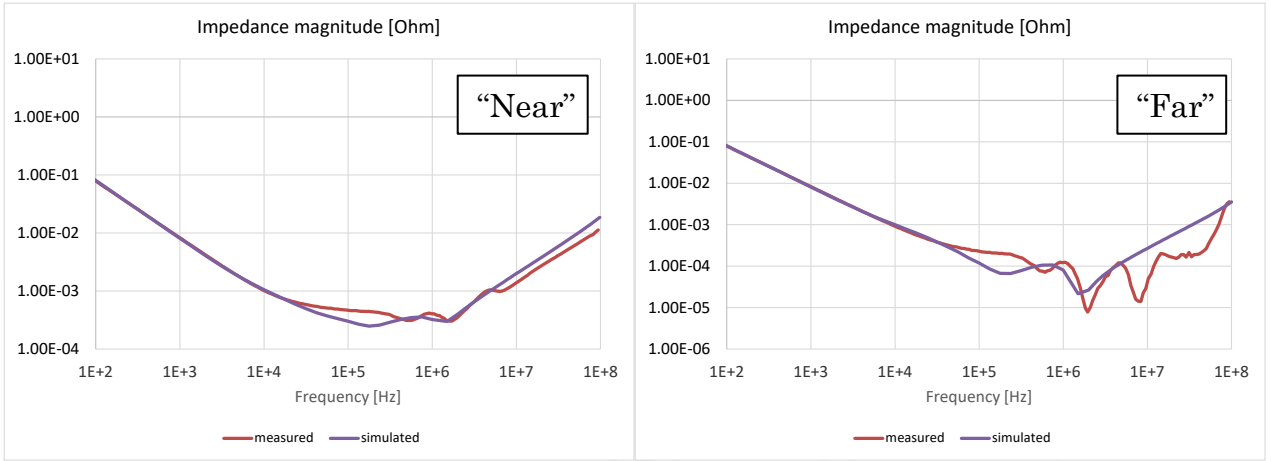


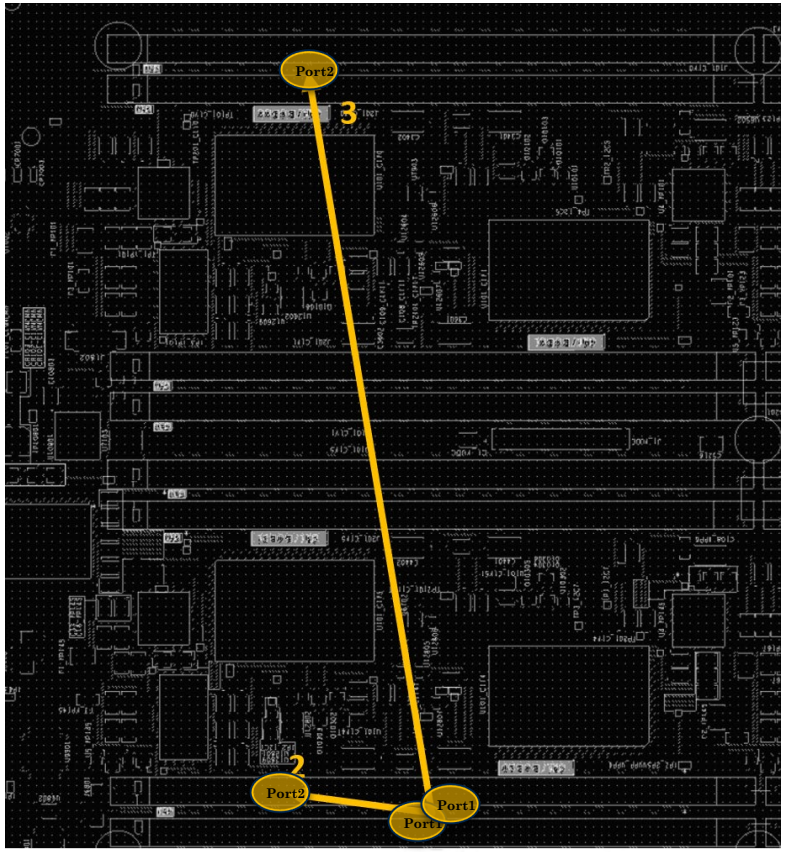


UV3435: N2 Region Self-Impedance
UAD3435: N2 Mid-Region Transfer Impedance
UAJ3435: N2 Cross-Region Transfer Impedance

DUT2: AC SIMULATION AND MEASUREMENTS

- Site 2/3: DIMM sites' transfer-impedances
  - "Near" transfer-impedance remains > 0.2mΩ
  - "Far" transfer-impedance bottoms out around 0.1mΩ
    - Dips to 10s of μΩ at SRF of MLCCs
  - Correlation good given simulation used RLC models
  - Measurement's 8MHz dip believed to be due to Memory Drivers' on-package decoupling (not modeled in simulation)





SUDDEN SERVICE®