PCB Design 007 *QuietPower* columns

Dynamic Models for Passive Components

Istvan Novak, Oracle, February 2016

A year ago the QuietPower column [1] described the possible large loss of capacitance in Multi-Layer Ceramic Capacitors (MLCC) when DC bias voltage is applied. However, DC bias effect is not the only way we can lose capacitance. Temperature, aging, and the magnitude of the AC voltage across the ceramic capacitor also can change its capacitance. Finally, the initial tolerance needs to be considered as well. In the worst case, we may lose up to 90% of the capacitance for an X5R capacitor, and even for an X7R capacitor. This column will show you the details and also how the most advanced manufacturers are helping the users with new simulation models to take these effects into account.

As an actual example, let us look at one of the capacitors that was extensively tested in [2], where 1uF 0603-size 16V capacitors were tested from various vendors. We further assume that we want to use the part on a 12V supply rail, where the AC noise is low (this will be important later when we take the AC bias dependence into account). Some of the samples were chosen with X5R, some with X7R temperature characteristics. As [2] showed with actual test data, X7R capacitors are sometimes worse for DC bias sensitivity than X5R parts.

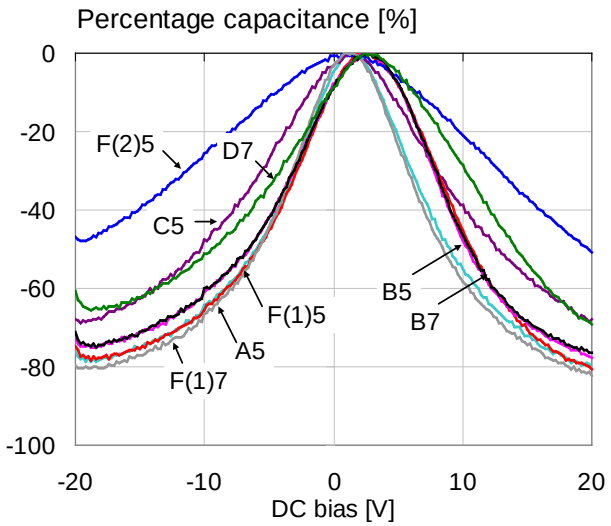

Figure 1: Percentage capacitance as a function of DC bias for all studied 1uF 0603 16V models, measured at 100 Hz and 10 mV AC bias.

If we take the part from Vendor B (labeled B7) on *Figure 1* (this was *Figure 5* in [2]), we see that at 12V DC bias we can lose 60% or 70% of the capacitance, dependent on which way the DC bias changes. But when we need to consider the worst-case capacitance loss, we have to consider the cumulative effect of all of the following factors:

- Initial tolerance
- Temperature effect
- DC bias effect
- AC bias effect
- Aging

The sample had +-10% initial tolerance. The X7R temperature characteristics comes with an additional +-15% tolerance window for the temperature variation.

When the part is used with low AC excitation across the part, the capacitance may be up to 20-30% less than what the standard test procedure provides. Since the vendors use the standard test methods, the AC bias dependence has only a negative range: 0 … -20%, sometimes up to -30%.

The aging in ceramic capacitors creates an exponential decay with a fixed percentage drop of capacitance for every decade of passed time. In case we take -2.5% per decade drop for X7R parts [3] and assume that the initial capacitance is measured 24 hours after manufacturing, within an expected life span of three years (26208 hours) this means approximately three decades of time, resulting in a -7.5% capacitance drop. If we consider the worst-case cumulative effect of all of the above contributors, we need to multiply all of the ratios corresponding to these percentage values. In the table below, we repeat the list of contributors together with their worst-case limits for the example part.

	Percentage range [%]	Relative multiplier
Initial tolerance	+-10	0.9 … 1.1
Temperature effect	+-15	0.85 … 1.15
DC bias effect	+0 -70	0.3 … 1
AC bias effect	+0 -30	0.7 … 1
Aging (over 3 years)	+0 -7.5	0.925 … 1

When we multiply the worst-case contributors, we get 0.9*0.85*0.3*0.7*0.925 = 0.15, which means instead of 1uF we have only 0.15uF capacitance. From the table we also see that with modern high density ceramic capacitors the biggest possible capacitance drop is due to the DC and AC bias effects. In some applications the loss of capacitance is important to know and therefore users want to simulate it. Until recently, however, simulation models were available only for no-bias conditions. This has changed with the emerging dynamic models [4], which use controlled sources inside encrypted models to create a true nonlinear response according to the instantaneous excitation across the part. Dynamic models are currently available for a number of popular simulators. The examples shown here were run on Linear Technologies LTSPICE. For the illustrations

below we use a GRM219R60G476ME44 part, which is 47uF +-20% X5R 4V capacitor in a 0805-size package. *Figure 2* shows the LTSPICE circuit to simulate the impedance of the capacitor with different bias conditions and *Figure 3* shows the impedance with 4V DC bias.

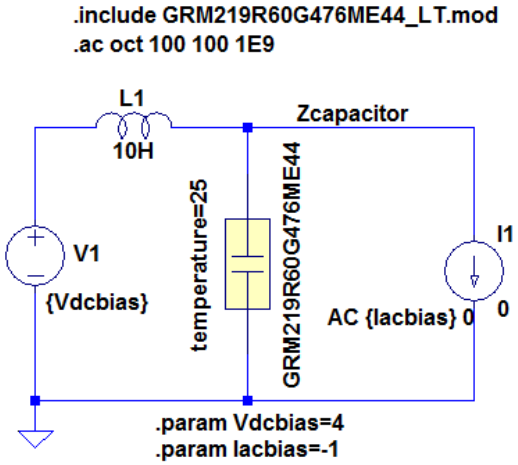

Figure 2: *LTSPICE simulation deck to calculate the linearized impedance at the 4V DC bias point.*

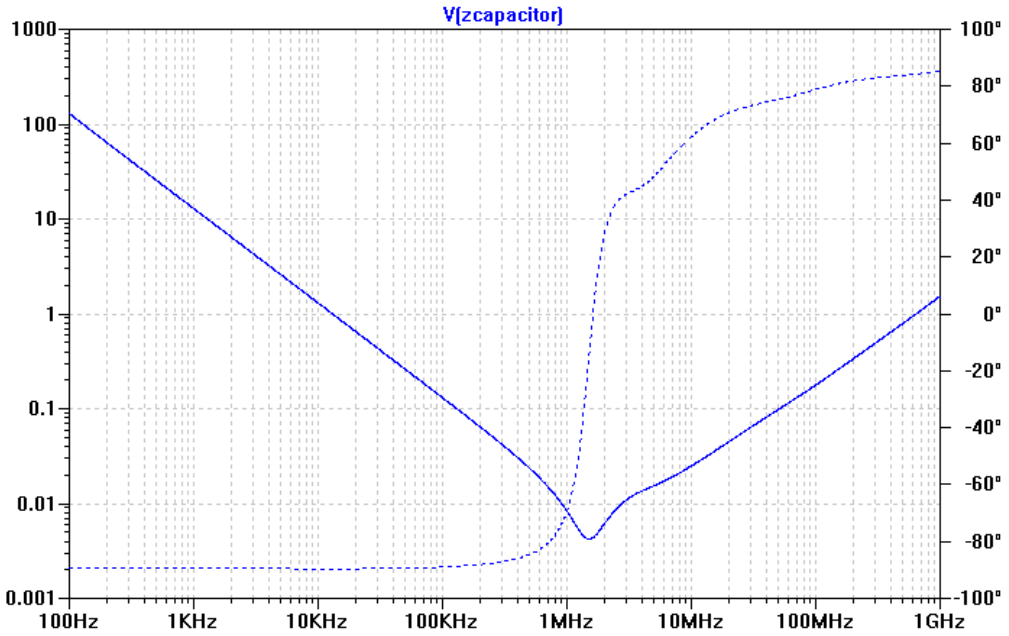

Figure 3: *Impedance versus frequency (magnitude, solid line, left axis and phase, dashed line, right axis) of the GRM219R60G476ME44 capacitor, simulated with its dynamic model.*

The data from *Figure 3* can be post processed and we can display impedance magnitude and real part, which is really the Effective Series Resistance (ESR), as shown in *Figure 4*,

and by further processing the imaginary part of the impedance, we can extract the equivalent capacitance and inductance, as shown in *Figure 5*.

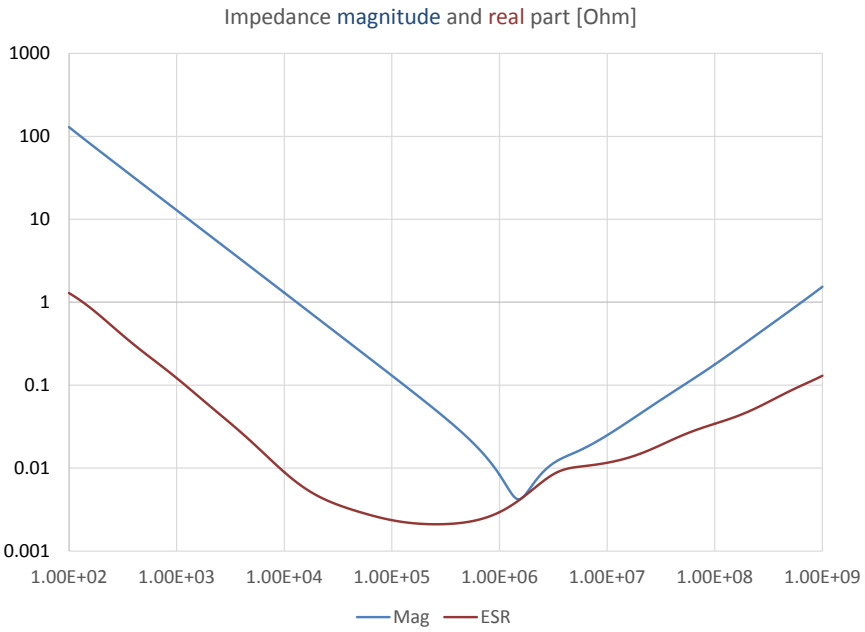

Figure 4: *Impedance magnitude and real part as a function of frequency, shown for the GRM219R60G476ME44 part with 4V DC bias.*

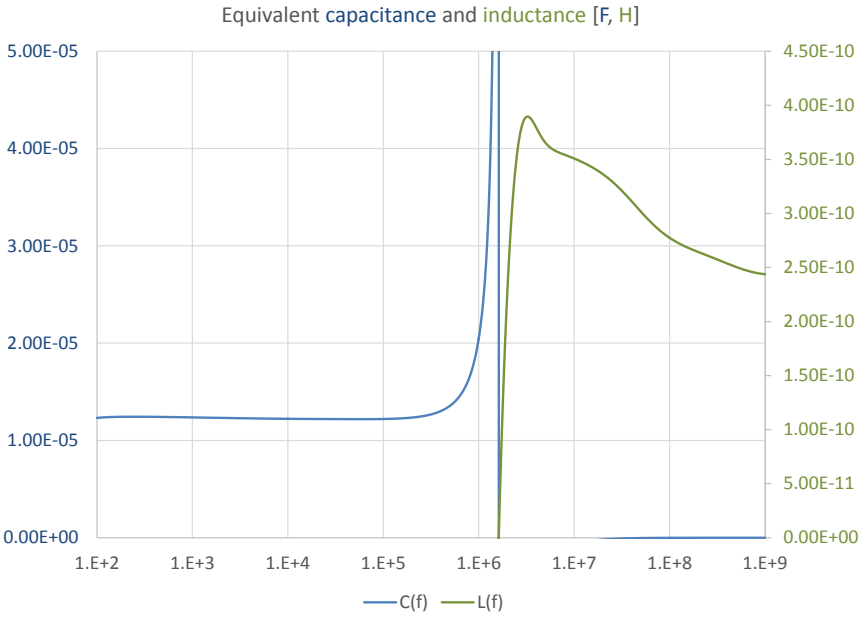

Figure 5: *Extracted capacitance (blue trace, left axis) and inductance (green trace, right axis) for the GRM219R60G476ME44 part with 4V DC bias.*

We can also run the simulation at different DC bias levels and show the equivalent capacitance at different DC bias voltages and we get a plot as shown in *Figure 6*. Note that even at 0V DC bias, the capacitance is just 35uF instead of the nominal 47uF. The reason for the difference is the AC bias dependence of the part. This dynamic model is based on measured data, where the excitation level is just a few millivolts, whereas the nominal capacitance is specified with a 0.5Vrms source voltage, and with the larger AC excitation the capacitance is bigger.

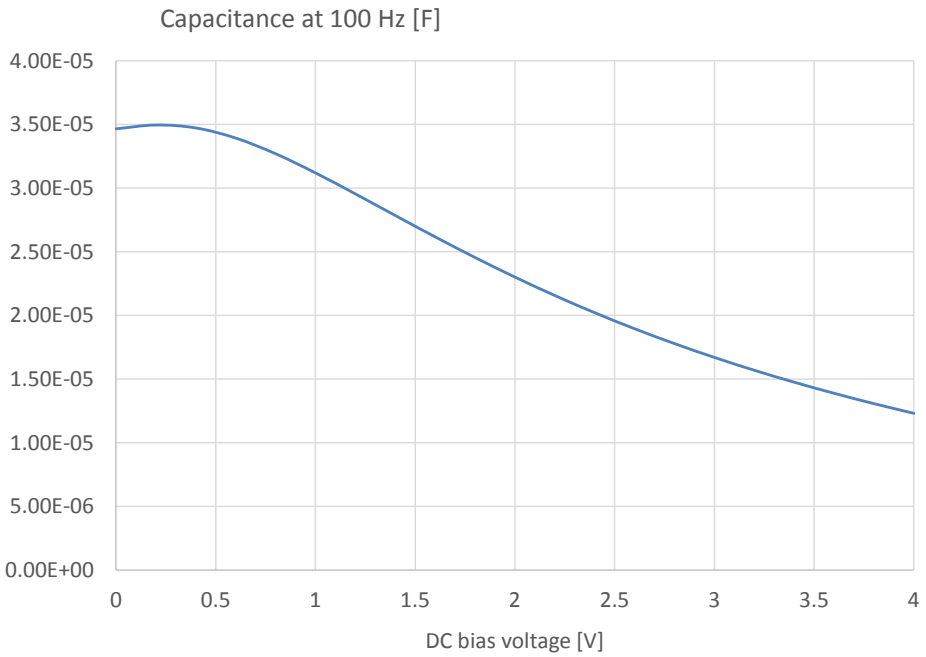

Figure 6: *Capacitance of the GRM219R60G476ME44 part at 100 Hz and different DC bias levels.*

The above simulation results used the AC SPICE simulation option, which linearizes the model at the given DC operating point. For this reason the capacitance extracted from the AC simulation result would not change if the test current value (I1 in *Figure 1*) changes. Of course we would need to scale the result, for instance with I1 = 0.1A, we would need to multiply the result by ten to get the correct impedance, but beyond this scaling we would get the same result for any value of I1. With time-domain simulations, however, we can expect the capacitor to show different capacitance values dependent on how the instantaneous voltage changes across the part. This best can be shown if we simulate the capacitor model with a linear voltage ramp across the part. The current through the capacitor will be proportional to its capacitance multiplied by the voltage slew rate. This means as the voltage across the capacitor changes as the ramp moves, the current through the capacitor also changes according to the change of capacitance with voltage bias. To make sure that we capture the DC bias dependence, we need to select a slow enough ramp. The ramp voltage in our simulation changes four volts in four millisecond. This voltage slew rate across the capacitor approximately corresponds to a bandwidth which matches the 100 or 120 Hz measurement frequency used by component vendors to test their parts.

Figure 7 shows the simulation deck, *Figure 8* shows the result. The current waveform in *Figure 8* shows sharp spikes at the beginning and the end of the ramp. We can ignore those spikes, since they are the result of the ideal piece-wise-linear voltage ramp with sharp corners at those time instances. For the duration of the voltage ramp, the current shows a voltage dependence that is very similar to that which we see in *Figure 6*. In fact from the current vs time function of *Figure 8* we can back calculate the capacitance and can show it on the same plot together with the AC simulation results, see *Figure 9*.

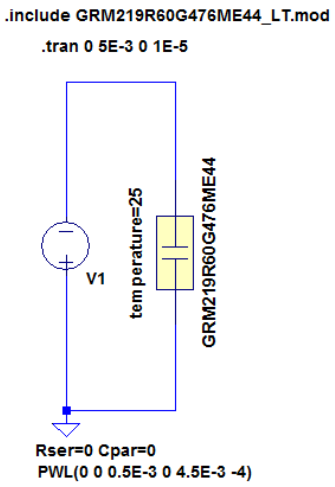

Figure 7: *Time-domain simulation deck to measure the voltage-dependent capacitance with a voltage ramp swinging from 0V to 4V.*

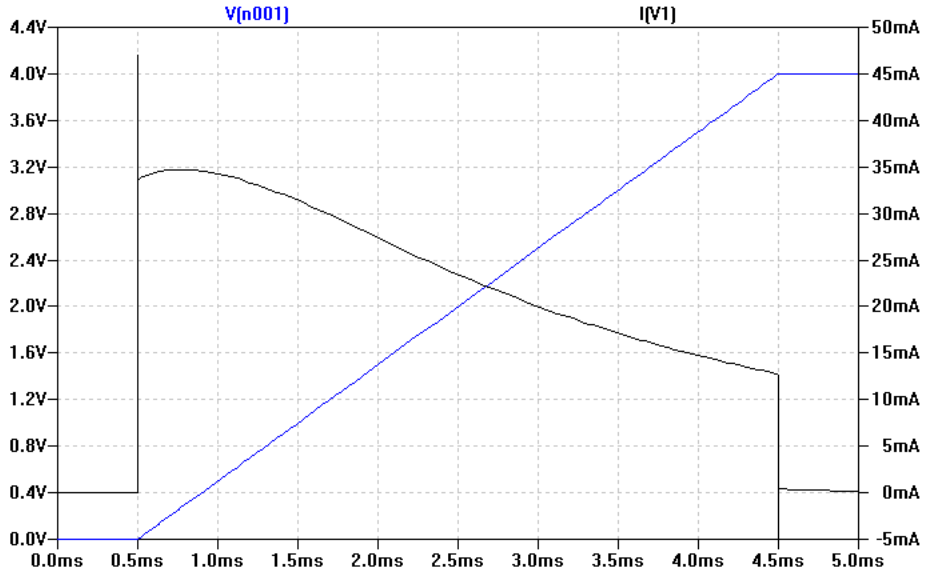

Figure 8: *Time-domain simulation results with the simulation deck shown in Figure 7. The blue trace with its axis on the left is the voltage ramp across the capacitor. The black trace with its axis on the right is the resulting current through the capacitor.*

The solid blue line is the same data we showed in *Figure 6*; this was the result of SPICE linearized AC analysis around the DC operating point. The red dots are the capacitance values calculated from the time-domain waveforms of *Figure 8*.

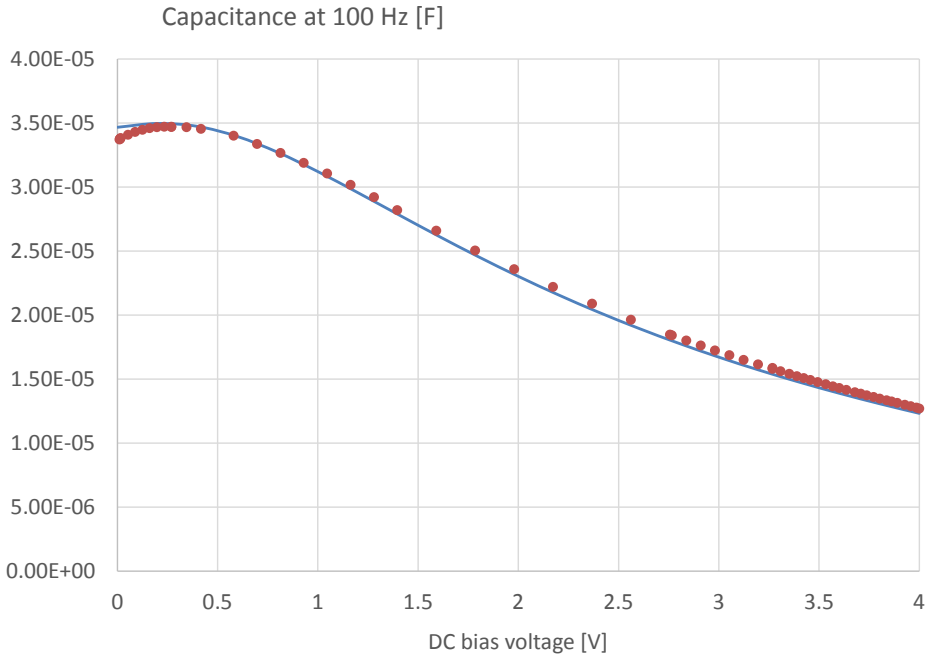

***Figure 9**: Comparison of capacitance vs DC bias voltage simulated with AC run versus time-domain ramp.*

The very good agreement between the two data series in *Figure 9* proves that these dynamic models are actually nonlinear and the capacitance changes instantaneously with the voltage. The dynamic models allow us to simulate the effect of DC bias dependence in LC filters, power circuits and in many other applications. Currently the dynamic models cover DC bias dependence; other parameters will be added in the future.

References:

[1] "DC Bias Effect in Ceramic Capacitors" Quietpower column, available at http://www.electrical-integrity.com/Quietpower_files/Quietpower-32.pdf

[2] "DC and AC Bias Dependence of Capacitors Including Temperature Dependence," DesignCon East 2011, September 27, 2011, Boston, MA. Available at http://www.electrical-integrity.com/Paper_download_files/DCE11_200.pdf

[3] http://www.johansondielectrics.com/ceramic-capacitor-aging-made-simple.html

[4] http://www.murata.com/en-us/about/newsroom/news/product/capacitor/2015/0727