

Why PI Design is More Difficult than SI

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Anyone practicing it can tell you that power integrity (PI) design for high-speed digital circuits is getting increasingly difficult in these days.

At first it was all about functionality. Lower-speed digital electronics only had to care about hooking up the components properly. Designs were schematics based, and the physical implantation, like PCB stackup, component placement and layout, mattered very little. At higher speeds signal-integrity (SI) issues emerge: we have to make sure that digital signals arrive on time and with low enough distortion. SI work means doing time of flight, skew and timing analysis and checking reflections, matching, crosstalk, attenuation and dispersion of signals.

With increasing speed and system density, power-integrity (PI) issues also become very challenging...

Exploding number of supply rails

Sometimes we hear the argument that PI is more difficult because we have an exploding number of independent supply rails to deal with. Ten or twenty years ago systems had one, maybe two or three different supply rails. Large computer boards today may have up to several dozens of independent supply rails. This is a big challenge, indeed. However, the number of supply rails is still many times lower than the number of high-speed interconnects, so this alone can not explain why PI is more difficult than SI.

2D and 3D problem instead of 1D

SI design is mostly a one dimensional problem. We know where the main signal goes: along narrow and long traces that we design. The traces determine the path of the signal. A major contributor to the PI challenge is the fact that a PDN is usually two, sometimes even three dimensional. Noise on planes can propagate anywhere in the X-Y directions and vias can carry the PDN noise in the Z direction as well. Also, we don't design the PDN to intentionally propagate the noise, just to the contrary: a well-behaved PDN should block the propagation of noise as much as possible. To figure out how noise spreads, we need 2D or 3D PDN models, which is harder to create and manage than a 1D SI model.

Unknown excitation and uncertain requirements

In SI, we usually know what the signal level and waveform are supposed to be. The 'main' signal for PI is the PDN noise excitation, but unfortunately its exact nature is mostly unknown to board designers. Noise excitation entering the PDN could come from a number of sources: power converter ripple and burst noise, shoot-through switching-

current spikes of active devices and last but not least, return currents of signals. Two of these four contributors, the converter burst noise and the shoot-through current spikes of active devices, are usually not – or just very vaguely - specified, so designers have very minimal input for a systematic PDN design. With the exception of the power-converter output ripple, which is typically fairly steady, all other noise components heavily depend on the system activity, creating a potentially huge parameter space to deal with. On top of all this, supply-rail noise tolerances of the various active devices are also very crudely specified: we usually have absolute limits only for the supply voltage, but very little knowledge about the different sensitivity of the device in different frequency ranges.

Lack of vendor support and standardization

SI work can get a lot of support today from component and tool vendors. Manufacturers of active and passive devices are increasingly willing to provide simulation models and characterization services, all the way to complete reference designs. There are also standard SI requirements for a number of signaling blocks to adhere to: eye masks, jitter specifications, attenuation, reflection and crosstalk limits. Instrument and tool vendors are eager to come up with solutions to simulate and measure our designs against the specification. Unfortunately PI design is mostly left without this kind of support: there is hardly any standard for PDN noise and PDN testing. This leaves instrument and tool vendors without guidance for their offerings. The lack of standards also leaves PI designers on their own to come up with a big part of the design requirements. There are application notes and a few reference designs available with PI content, but their applicability is usually limited to a narrow choice of parameters used for those particular examples.

SI had decades to figure out solutions. By now a big part of our SI work is better understood and bounded. In contrast, many today feel that PI design is ill determined and daunting. If you feel overwhelmed by the complexity of PI design, you are not alone. Many of us feel that way. Collective wisdom and experience over the coming years will surely help to alleviate the pain somewhat, but we should expect this challenge to stay with us for some time to come.