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How Much Signal Do We Lose Due to Reflections?

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We know that in the signal integrity world reflections are usually bad. In clock networks reflection glitches may cause multiple and false clock triggering, in medium-speed digital signaling reflections will reduce noise margin and in high-speed SerDes signaling reflections increase jitter and create vertical eye closure.

Reflections happen along an interconnect at any point where the impedance environment around the electromagnetic wave changes. *Figure 1* illustrates this with a simple example using a uniform stretch of transmission line with Z_{01} characteristic impedance between Z_0 reference impedance connections.

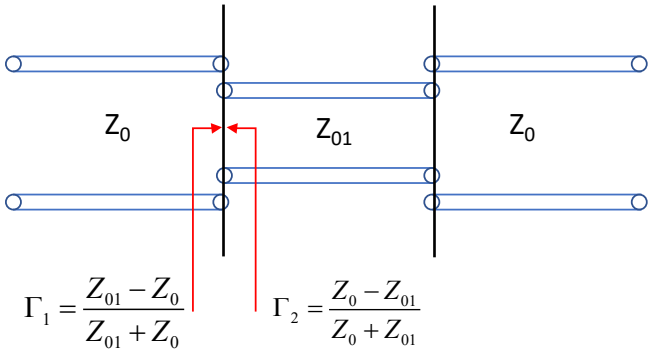

Figure 1: *Definition of voltage reflection coefficient.*

The formulas shown in the figure for the Γ voltage reflection coefficient are generic and they express the complex ratio of reflected and incident waves. We can apply the formula to steady-state impedances, something we could measure with a Vector Network Analyzer, or to transient impedances, which would be the case when we use Time Domain Reflectometry. In general, the impedances that go into the formula, and as a result, the voltage reflection coefficient itself as well, are complex numbers with magnitude and phase, or real and imaginary parts. Another generic characteristic is that the direction of the arrow at the end of the red line has a significance: in the nominator of the voltage reflection formula the first term is the impedance the wave will enter into by crossing the boundary and the second term is the impedance the wave is coming from. This means that if we calculate the voltage reflection coefficient at the same boundary, but going the opposite direction, the sign of the voltage reflection coefficient will change while the magnitude stays the same.

As a simple example, lets assume that we have a lossless transmission line with a Z_{01} = 45 Ohm characteristic impedance and we look at it between Z_0 = 50 Ohm reference impedances. This represents the lower bound of a +-10% impedance tolerance for a 50-Ohm trace. With all impedances being real numbers in this simple example, the voltage reflection coefficient is also real, with a value of Γ_1 = -1/19 and Γ_2 = 1/19, or approximately +/-5%. Based on the 5% reflection magnitude we may expect that 95% of the launched signal will continue after the reflection. To test this assumption, we can do a very simple simulation. *Figure 2* shows the circuit drawn in LTSPICE: a lossless 45-Ohm Tline section between a 50-Ohm source and load 50-Ohm termination. The resulting frequency response is shown in *Figure 3*.

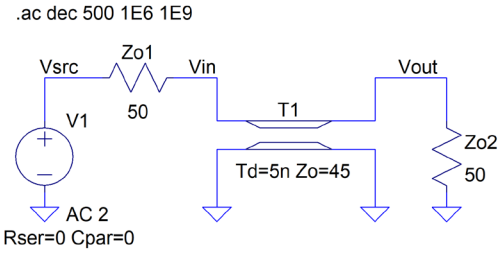

Figure 2: *LTSPICE simulation circuit with impedance mismatch.*

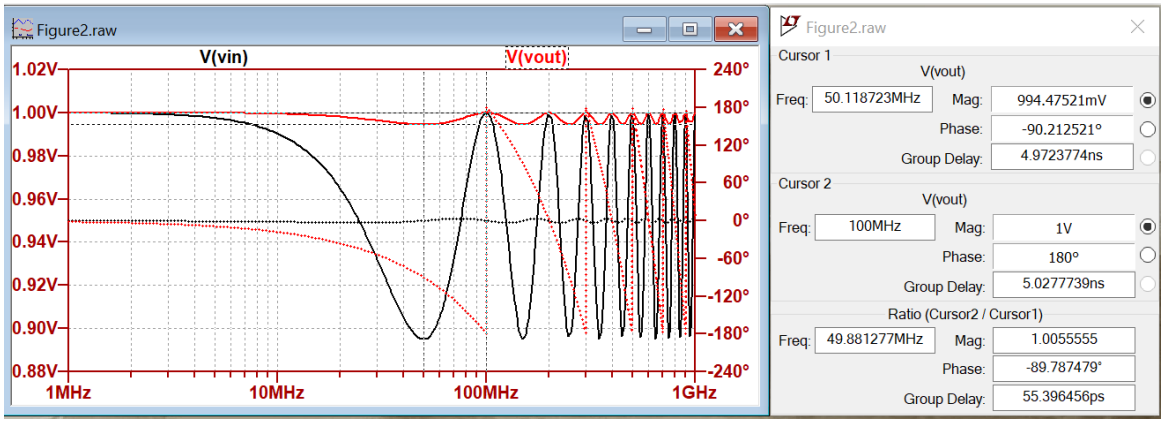

Figure 3: *Frequency response of circuit in Figure 2. Voltage magnitudes are solid lines referencing the left vertical axis, phase is dotted line, referencing the right vertical axis.*

With 2V source voltage, if we had all matched conditions, Z_0= Z_{01} = Z_{02} = 50 ohm, we would expect and in fact we would get 1V across the load regardless of frequency. That is actually the signal level we get at very low frequencies in our example, too. As frequency goes up, we notice that both the input voltage (the voltage across the input of the transmission line, after the source resistance) and the output voltage start to drop, but at a different rate. At 50 MHz both curves reach their minimum values: Vin voltage drops approximately 10%, but the Vout output voltage drops only 5.5 mV, much less than the 5% what we would expect from lumped-circuit assumptions. The variation continues

periodically with frequency: the traces reach a 1V maximum at 100 MHz and then the behavior repeats. With 5 ns delay through the transmission line, the first minimum at 50 MHz corresponds to the quarter-wave condition, at the maximum points of 100 MHz and its multiples we have the half-wavelength (and its multiples) condition.

Note the logarithmic frequency scale; it visually distorts the plots, making the linear phase lines looked curved, but at the same time it allows us to observe a several-decade wide frequency range with good resolution throughout the entire range. With linear frequency scale the phase curve would be a straight line sloping downwards following the simple formula:

$$\varphi = \omega\, t_{pd}$$

where φ is the phase angle in radians, ω is the radian frequency and t_{pd} is the propagation delay through the transmission line. Note also the delay readout in the cursor field: 4.97 ns at 50 MHz and 5.03 ns at 100 MHz. These numbers are close to the 5 ns delay we assigned to the transmission line, but we still may wonder: is this difference coming from numerical calculation errors or does this represent the real behavior of the circuit? As it was explained and illustrated in more detail in [1], what we see here is the manifestation of the fact that reflections can change the steady-state delay in a frequency-dependent manner.

Before we get back to why the output voltage drops only so surprisingly little, lets look at a different example. Instead of a direct impedance mismatch, we now use a Z_0 = 50 ohm transmission line and we use a series 5-ohm resistor, which may crudely represent its conductive losses. As opposed to regular printed circuit board traces, where the conductive losses are frequency dependent, the practical equivalent of this case could be for instance a thin-film transmission line. The schematics is shown in *Figure 4*, the frequency response is shown in *Figure 5*.

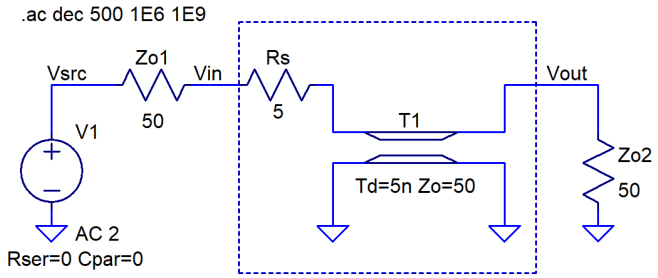

Figure 4: *LTSPICE simulation circuit with series loss resistance represented by a 5-ohm series resistor.*

In this case the result matches our simplistic expectation: regardless of frequency, we get an approximately 5% drop in the output voltage.

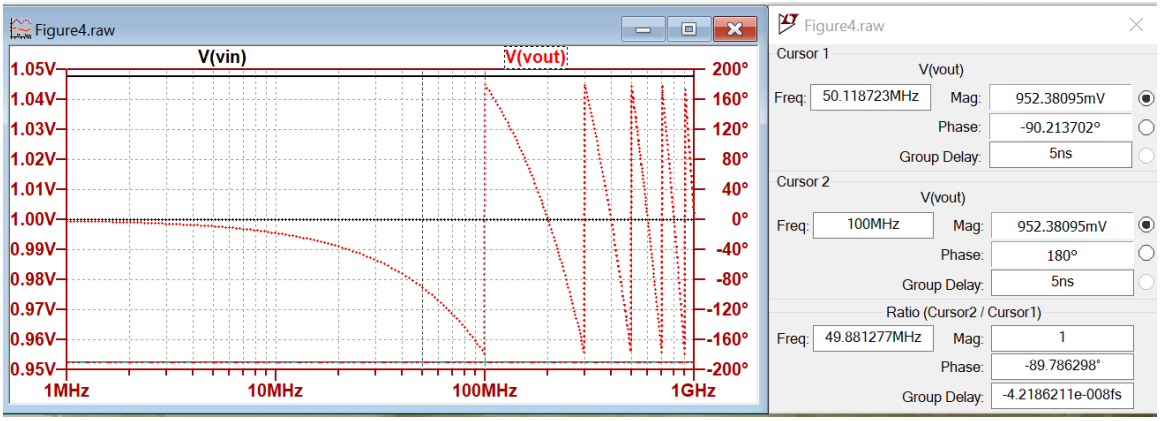

Figure 5: *Frequency response of circuit in Figure 4. Voltage magnitudes are solid lines referencing the left vertical axis, phase is dotted line, referencing the right vertical axis.*

To understand the reason for the two seemingly very different behaviors, we reach back to a fundamental principle, the conservation of energy. If we have a lossless (linear and time invariant) circuit that does not lose power due to losses, radiation or in any other way, we know that if we send a unity amount of power towards the circuit, the sum of the reflected and transmitted powers must equal unity. Expressed by the elements of the S matrix of the network, practically this means that the sum of the squares of the S-matrix elements in each row or column must add up to one. For instance, in case of a two-port lossless network and assuming that we launch the signal towards Port 1, this means

$$(S_{11})^2 + (S_{21})^2 = 1$$

This expression tells us that if we have $|\Gamma| = |S_{11}| = 0.1$ or 10% reflection from a lossless circuit, the magnitude of the transmitted wave will be sqrt(1-0.01) ~ 0.995, and this matches what we get from the simulated response.

Our second example is fundamentally different. The simple fact that we included a series resistor in the circuit, made the circuit lossy. Though the conservation of energy principle still applies, now in the power sum we would also need to include the power lost by dissipation across the series resistor. We could follow this approach to calculate the signal magnitude at the output, but we can also use some other simple tricks to get an answer. In *Figure 4*, looking into the T_1 transmission line on the left, its input impedance is 50 ohms, regardless of the frequency, because we deal the input impedance of a matched-terminated lossless transmission line. Based on this realization we can draw a simplified equivalent circuit, as shown in *Figure 6*. Looking into the circuit from the left, we see the sum of R_s and Z_{02}, or 55 ohms. From the 2V source voltage together with the 50-ohm source impedance this input impedance creates a 2*55/(55 + 50) = 1.0476 ~ 1.05 V signal, just as we see in *Figure 4*. From this input signal the 50/(55 + 50) voltage attenuator produces approximately 0.95 V, just as we see in *Figure 4*.

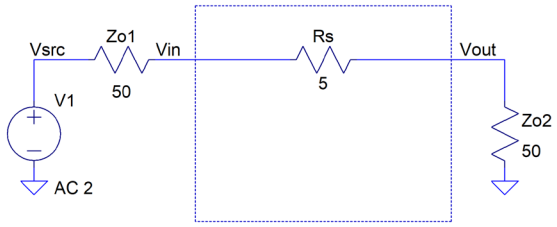

Figure 6: *Simplified equivalent circuit of the network shown in Figure 4.*

These above two examples represent the bounding limits we have to deal with in practice when we have lossy or lossless passive networks. These two extreme conditions can simply be plotted in spreadsheets in a normalized fashion. *Figure 7* can be applied to cases similar to *Figure 2*. The fact that the circuit does not dissipate power is represented here by a (lossless) reactance in series to the lossless transmission line. The plot on the left uses on the horizontal logarithmic scale the absolute value of the series reactive impedance; the plot on the right uses the same data with the reactive impedance normalized to the reference impedance. The plots show two lines: Return Loss (the dB value of the S_{11} input reflection coefficient) on the left axis and the Insertion Loss (the dB value of the S_{21} transmission coefficient) on the right axis.

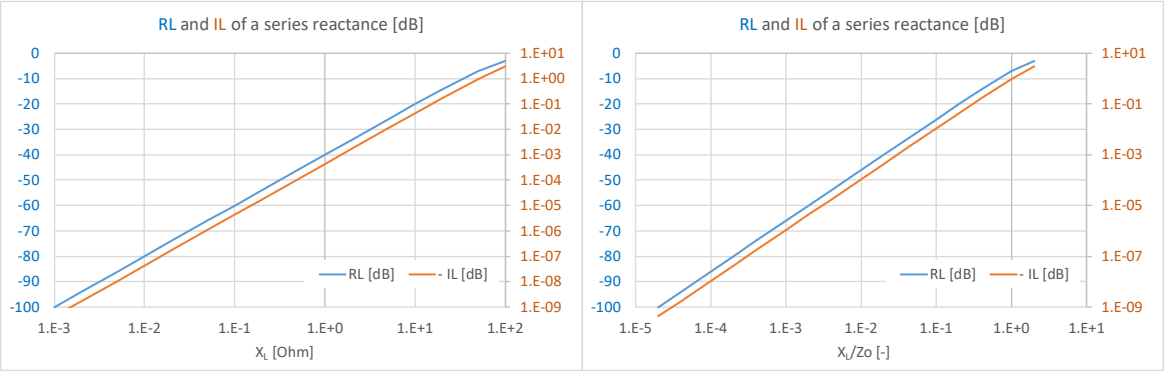

Figure 7: Calculated Return Loss (RL) and Insertion loss (IL) of circuits similar to shown in Figure 2.

Finally *Figure 8* shows similar plots when we use lossy circuits. We model it with a lossless transmission line and a series resistor. To allow easy comparison, the organization of the two plots is exactly the same that we had in *Figure 7*. The lines look very similar in the two figures, but we have to notice that the insertion loss lines in *Figure 7* are much steeper. This tells us numerically that when we deal with lossless, purely reactive circuits, or in other words when we have only reactive reflection loss, the loss of signal magnitude diminishes very sharply as we reduce the reflection magnitude and even

moderate or medium reflections will result in relatively small loss of signal strength at the output.

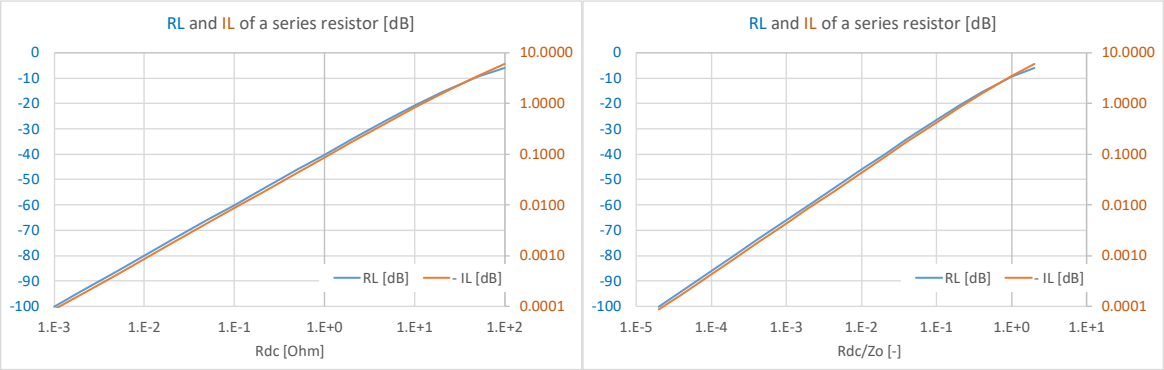

Figure 8: Calculated Return Loss (RL) and Insertion loss (IL) of circuits similar to shown in Figure 4.

In contrast, when we have dissipative losses, the signal strength on the output will be much less and even relatively small losses will result in noticeable loss of signal magnitude at the output.

As a final note, we need to keep in mind that while single reactive discontinuities (for instance connector launches, vias, antipads) will result in miniscule signal loss, when we have a periodic structure with evenly spaced multiple discontinuities, even small reflection will result in significant signal loss at frequencies where the small reflections all add up (see for instance [2] and [3]). On the flip side, though dissipative losses result in higher up-front signal loss, this loss of signal strength will be much less sensitive to the parameter variations of cascaded multiple segments.

References:

[1] "Sources and Compensation of Skew in Single-Ended and Differential Interconnects," DesignCon 2014, Santa Clara, CA, available at http://www.electrical-integrity.com/Paper_download_files/DC14_14_WE1Paper_SourcesAndCompensationOfSkew.pdf

[2] "Attenuation in PCB Traces due to Periodic Discontinuities," DesignCon 2006, Santa Clara, CA, available at http://www.electrical-integrity.com/Paper_download_files/DC06_SUN_AttenuationPeriodicalSiscontinuities.pdf

[3] "Additional Trace Losses due to Glass-Weave Periodic Loading," DesignCon 2010, Santa Clara, CA, available at http://www.electrical-integrity.com/Paper_download_files/DC10_7-WA1_Miller-Blando-Novak.pdf