QuietPower columns

Printed Circuit Board Fixtures for Power Integrity

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Power-integrity components, such as bypass capacitors, inductors or ferrite beads or other small discrete components can be characterized in fixtures. There is a wide range of fixtures available from the professional and very accurate [1] to the home-made and very crude [2]. In between these extremes you will find various printed-circuit board fixtures, for instance the Decoupling Test Board Kit shown in *Figure 1* [3], or the RF Experimenter board set shown in *Figure 2*.



Figure 1.: Picotest component characterization fixtures.

The Picotest boards come with Touchstone files for de-embedding the measured data. I particularly like this kit, because it has separate small boards with solder pads specifically for a wide range of surface-mount component sizes, including also reverse geometry capacitors and some medium-size bulk capacitors. The range starts with 0201 size and includes 0204 and 0612 reverse-geometry sizes. Large-size polymer capacitors can be tested on the D-size (7343) fixture, for surface-mount cylindrical capacitors we get 5mm and 8mm sites. To test filter structures, two of the smaller sizes (0402 and 0603) have also a generic T scheme: pads for two components in the series path and for one component in the shunt path. There is a dedicated site for single-body 0402-X2Y filter elements. This test board kit also has a single-piece open-short-load impedance reference board; you can find it in the oversized lower middle compartment in *Figure 1*.

You can also build fixtures straight out of small coaxial connectors, as it was shown in [4].

With all of these fixtures we need to keep in mind that the current path around the device we characterize does not necessarily match the current path that is created by the layout and stackup in our final application. In the solder-wick fixture the current path is highly uncertain; the shape of the flexible connections will vary dependent on how we achieve the pressure-mount connection. With the fixtures built entirely out of SMA connectors we have a fixed geometry for the connector pieces, but there are no dedicated pads to solder the parts down, so the actual current path depends on how we solder the DUT between the center pins and outer frame. This means that the extracted mounted inductance values will need to be used with some caution.

Generic PCB fixtures such as shown in *Figure 1* and *Figure 2* can be created from small co-planar 50-ohm traces that have exposed trace and ground next to each other on the same side of the fixture. The DUT can be connected between the trace and the ground shape, allowing us to use the Two-Port Shunt-Through measurement topology. Having a sufficiently large solder-mask free ground shape next to the trace, we can accommodate a large number of different case styles and sizes with the same board. Having connectors at the ends of the through trace will allow for quick connections and disconnections, though we could also use permanently attached (soldered) cables. Soldered connections would eliminate the need for separate cables with connectors at both ends, but would make the calibration a little bit more difficult. The photo in *Figure 2* shows an un-assembled panel of eight fixture boards that we can break away. Though the eight boards carry different labels, physically they are the same.



Figure 2.: Un-assembled panel of RF Experimenter Boards from SV1AFN [5].

If we solder SMA female connectors to both ends, the fixtures will conveniently take cables with male connectors.

The lines of the fixture are CPW (co-planar waveguide) over ground. The printed circuit material is FR4 and the board thickness is 0.8 mm. The gold-plated nickel over copper is 35 um (1 oz) and the line width is 1 mm with 0.254 mm separation to ground. As you can see from the measured TDR response of *Figure 3*, the coplanar traces are close to 50 ohms and have only 175 ps delay, which means for a lot of measurements up to 10 MHz a simple Response Through calibration is enough.

If we want to start the sweep anywhere below a few times ten kilohertz and at the same time we also want to measure components that have low impedance at low frequencies, such as low-ESR high-capacitance parts, we run up against the cable-braid loop error [6]. Dependent on how we want to reduce the cable-braid loop error, the chosen solution may

come with its own limitation at low or at high frequencies. For the photo on the right of *Figure 4* I used a home-made common-mode choke, with an upper bandwidth of approximately 50 MHz. With this setup data was collected in the 300 Hz to 30 MHz frequency range with a simple THRU calibration. Professional options for common-mode transformers for power-integrity measurement purposes are also available today [7]. The setup on the left of *Figure 4* uses flexible coaxial cables with low braid resistance [8], which eliminates the need for a common-mode transformer as long as the DUT impedance is not extremely low.



Figure 3.: TDR response of a matched-terminated fixture shown in Figure 2.



Figure 4.: Measurement setup with Keysight E5061B network analyzer. The commonmode toroid transformer on the right photo is encapsulated in a small black plastic box.

With these fixtures we also have the option of connecting the DUT in different ways. Mechanically and electrically we get the most robust and most reliable connection if we solder or firmly clip the part to the fixture. If we want to re-use the fixture and want to speed up the swapping of components, we can opt to use simple pressure mount and maybe we can reduce the contact resistance and improve consistency of our collected data by applying a dot of silver paste under the component terminals. If we decide to solder the component, we can improve the repeatability of the measurement by pushing down the parts on the pads during soldering. This way we can make sure that the thickness of solder layer between the component terminal and fixture pad is the possible minimum.



Figure 5.: 1210 size MLCC parts soldered on the PCB fixtures. 330uF 4V part on the left, 47uF 16V part on the right.

In *Figure 5* the two fixtures are shown with 1210-size ceramic capacitors soldered on them. The two setups in *Figure 4* use slightly different settings. Though the 330 uF ceramic capacitor has approximately 1 mOhm ESR, the impedance rises as we go towards lower frequencies. We also used cables with low braid resistance and therefore we did not need a common-mode transformer. This allowed us to set the upper sweep limit to 100 MHz. Full two-port SOLT calibration was done with a Keysight mechanical calibration standard.

The network analyzer gives us two-port S parameters. From the scattering matrix we use one of the transfer parameters, either S_{21} or S_{12} ; they should be the same or very close within minor measurement errors. During the through calibration, the 0 dB level of S_{21} is set when Port 1 and Port 2 are directly joined without a DUT. After calibration, from the measured S_{21} value we can calculate the Z_{DUT} unknown complex impedance:

$$Z_{DUT} = \left(\frac{50}{2}\right) \frac{S_{21}}{1 - S_{21}}$$

In the next step we take the imaginary part of the impedance and assume that it comes from capacitance or inductance. If the imaginary part of impedance comes from capacitance or inductance, we can use the following formulas, respectively:

$$Im\{Z_C\} = -1/(\omega C) \qquad Im\{Z_L\} = \omega L$$

Here ω is the radian frequency, or $2\pi f$. You can apply both formulas simultaneously over the entire frequency and rearrange them for *C* and *L*. They will give the correct (positive)

capacitance and inductance values in their respective portion of the frequency range and will give negative results in the frequency ranges where the assumption about the nature of impedance is incorrect.

Figure 6 shows the measurement result from the setups and DUT shown in *Figure 4* and *Figure 5*. We make use of the Impedance Analysis Option of the network analyzer and we can set up the screen to show four simultaneous traces: Impedance magnitude (upper left), Effective Series Resistance, Rs (upper right), Equivalent Series Capacitance, Cs (lower left) and Equivalent Series Inductance, Ls (lower right). The logarithmic horizontal scale starts at 300 Hz and ends at 30 MHz. For this DUT, the 70 Hz IFBW setting provides a good compromise between fast sweep and low noise floor.

The measurement result shows several familiar details. From 300 Hz to almost 1 MHz the impedance magnitude slopes downwards, indicating capacitive impedance. The trace bottoms out at 850 kHz with a 2 mOhm value at the series resonance frequency. Beyond 850 kHz the impedance magnitude slopes upwards, indicating that we are in the inductive region. There are smaller secondary resonances and inflection points between 1.5 and 3 MHz, beyond which the impedance stays clearly inductive. The effective series resistance plot (which is simply the real part of the measured complex impedance) on the upper right follows a similar pattern. At low frequencies it runs parallel to the impedance magnitude curve and their ratio is the dielectric loss tangent. You can read more about this in [9]. After a broad minimum near the series resonance frequency, the effective resistance also trends upward with a few secondary resonances. On the lower left and right plots you see the capacitance and inductance extracted from the imaginary part of the measured complex impedance.



Figure 6.: Measurement data of the 47uF 1210 size ceramic multi-layer capacitor taken in the co-planar fixture.

With the data shown in *Figure 6* we get positive extracted capacitance and negative inductance (that we just ignore) below 850 kHz. Above 850 kHz we get positive inductance and negative capacitance (which, again, you just ignore). Finally, if we look at the extracted capacitance and inductance curves, we can notice that both are sloping downwards slightly. The capacitance curve slopes downwards due to the dielectric losses: the higher the loss tangent, the more pronounced slope you see. The inductance curve slopes down because of the finite size and thickness of the DUT: at low frequencies the current path is determined by resistive losses and as a result the current spreads out utilizing a bigger part of the structure. At high frequencies the current path is dictated by the path inductance, and inductance is smaller in smaller loops, so if the current has the opportunity to rearrange itself as frequency changes, it will flow in smaller loops as frequency goes up.

Co-planar fixtures are very convenient and universal, but they come with some limitation. Similar to the solder-wick fixture, the co-planar trace represents not only a convenient way to attach a DUT, it also creates a 'sneaky path' between the two VNA ports, which limits the lowest impedance we can measure this way. Second, being generic, chances are that these fixtures will not match the geometry of our final usage of the component in our design. This latter, however, has an impact only on the inductance; the capacitance and ESR still can be assessed with high confidence.

References

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