AI Triggers the Next Paradigm Shift in PDN

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Artificial Intelligence (AI), together with Machine Learning (ML) created an unprecedented surge of computing and networking infrastructure needs. This in turn has dramatically increased the power consumption of computing and networking chips. Traditional design and validation methods no longer seem to be able to cope with the new challenges: a paradigm shift is under way how we design, optimize and validate our system power distribution.

During my career in electronics design, the first paradigm shift happened in the late 1990s, when the Central Processing Units (CPU) in computers grew in complexity and required 10s of ampere of core current. Very early computer boards did not need any specific power distribution design. This is illustrated on the left photo in Figure 1, which shows a Diode-Transistor Logic (DTL) card from a computing equipment made in the 1970s. It was on a two-sided board, with no ground plane and no bypass capacitor in sight. And we all remember the prevailing rule of thumb from the 1980s: place a 0.1uF ceramic capacitor across the power-ground pins of each logic chip, back then usually in Dual-in-Line (DIL) package. By the mid 1990s the current transients of CPU core rails required a new approach: power ground plane pairs replaced the power-ground traces, the number and values of bypass capacitors increased and a systematic frequency-domain design approach was developed. It was based on a calculated impedance target for the power distribution network [1]. Impedance target in the 1990s was tens of milliohms, which already created its challenge for validation: instrument setups previously used to measure impedance were not capable of measuring milliohms on working computer boards. To measure milliohms, the two-port shunt-through measurement setup was created [2], which has been in use ever since. In multi-layer printed circuit boards (PCB) using one or a couple of plane pairs to serve the low-impedance supply rails provided low enough series resistance that the horizontal power distribution lumped the entire power distribution network with tolerably low spatial variations. As a reminder: the sheet resistance of a one-ounce copper plane is around 0.7 milliohms, which is low compared to a 10 milliohm parallel target impedance. This was also the time before the wide-spread use of digital power converters. As a result, such PDNs could be treated as Linear and Time Invariant (LTI) networks, allowing us to use either time or frequency domain to measure or simulate our circuits, because getting the other domain was straightforward and easy with Fourier transform.

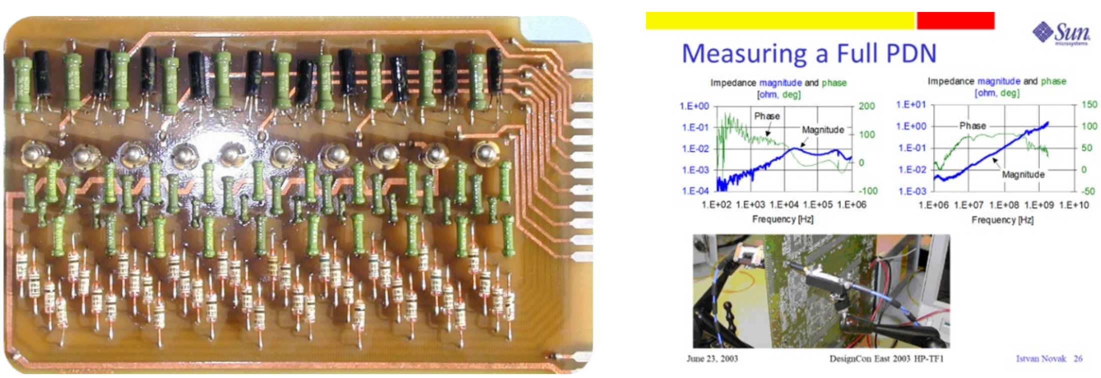

Figure 1: Two-layer DTL logic board from the late 1970s (on the left) and validation setup and PDN impedance on a server board from the 2000s (on the right)

Measuring PDN impedance at the milliohm level was readily doable with the two-port shunt-through scheme by probing the PDN at a dedicated power-ground plated through hole pair with probes connected to the top and bottom.

As the years passed, chips continued to become more power hungry: clock frequencies kept going up, supply voltage continued to drop and the maximum current draw and current transients were also on the constant rise. Lower supply voltages require us to set tighter absolute noise budget, which combined with rising current values results in a fast dropping target impedance. The recent boom of AI and ML accelerated this trend and in recent years we have arrived to another paradigm shift, which rapidly unfolds in front of our eyes. The largest chips now require tens of microohms PDN impedance to feed them, which creates significant new challenges. Validating microohm AC impedance is not trivial with the available instrumentation. But there are also bigger challenges: PDNs can not be considered lumped any more even at low frequencies, because the series plane impedance becomes comparable to or even bigger than the required parallel PDN impedance. This can create strong spatial variation of impedance and noise, regardless of whether we look at it in the frequency or time domain. The very low target impedance exposes three-dimensional (3D) interactions between probes and PDN that were previously masked by the higher target impedance [3]. Figure 2 on the left shows the probing of PDN in the footprint of a high current chip. PCBs which make use of blind vias to connect the surface pads to the power planes below lack through holes, so the probes for the two-port shunt-through testing must be placed on the pads on the same side of the board. Having wafer probes next to each other creates extra inductive loop coupling between the exposed probe tips, which may mask out the low DUT impedance we need to measure. Adding to the challenge, this probe tip coupling today can not be calibrated out with the available vector network analyzer (VNA) calibration methods. Adding to the list of challenges, the component density of our systems and subsystems puts potential noise sources and noise victims closer together, giving rise to increased in-system interference. Figure 2 on the right shows a multi-kW very compact power converter. To reduce distribution loss, we need to place the power converters close to the chips, where high-speed signals are concentrated, further increasing the chances for in-system interference.

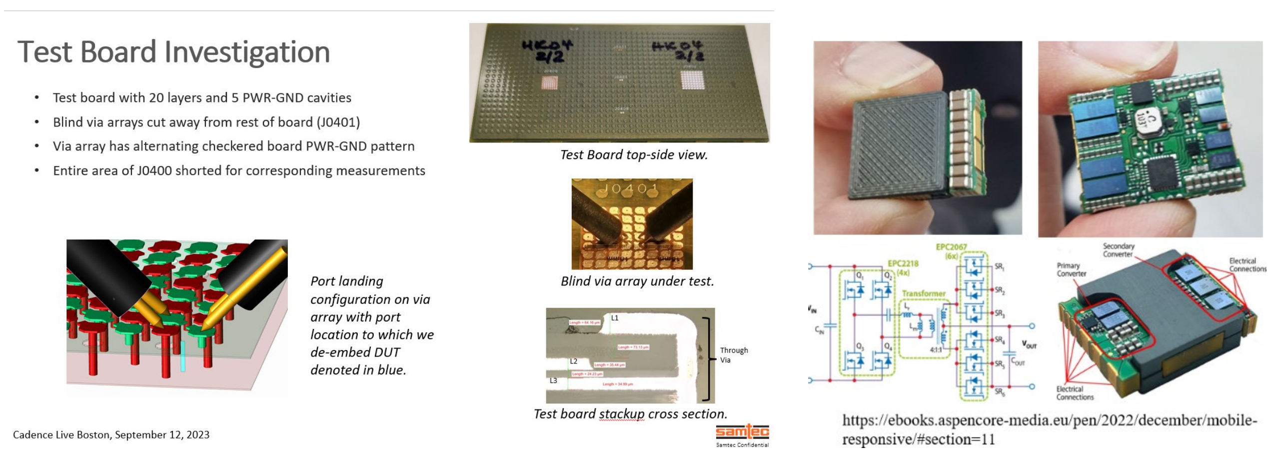

Figure 2: Illustration of 3D interaction between probe tip loops (on the left). High-power bus converter illustration on the right [4].

There are also additional challenges: the nonlinear functions of digital power converters make the PDN validation more complex and the easy conversion between time and frequency domain is valid only in the range of linear operation. The functionality under very large current transients have to be validated by a custom fixture, capable of creating large current transients.

The coming years will show what solutions the industry will settle on to solve these challenges. One emerging possibility is using vertical PDN, feeding the high-current supply rails of chips from below the main board, not relying on horizontal power planes in PCBs. In either horizontal or vertical PDN, validation of microohm impedance is very difficult. To enable and encourage cooperation among users, CAD and instrumentation companies, a new open-source PDN challenge has been suggested [5]. The entire CAD package has been made available for download at [6].

References

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